GARVIT VYAS

New York, NY | +1 (646) 210-4081 | gv2361@columbia.edu | https://www.linkedin.com/in/garvit-vyas/ | https://github.com/garvitvy18

EDUCATION

COLUMBIA UNIVERSITY New York, NY
Master of Science in Computer Engineering *Expected Dec 2025*
Coursework: System-On-Chip Platform, Computer Architecture, Formal Verification, Logic Design, Embedded Systems, Embedded AI

BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE (BITS), PILANI Hyderabad, IN
Bachelor of Engineering in Electronics & Communication Engineering *Jun 2024*
Coursework: Digital Design, Microprocessor Interfacing, Analog Electronics, Communication Networks

EXPERIENCE

ARM Chandler, AZ
SoC Engineer Intern *May 2025 - Present*
- Architect an automated register-block verification flow by parsing golden Markdown specs (via Jade Register Manager) into IP-XACT/JSON/XML, then develop custom C tests for various cases that run self-checking validations over the APB bus.
- Scale the framework with Python scripts and UVM/SystemVerilog wrappers to auto-generate signal-probe code for complex register behaviors and orchestrate an SoC-wide verification plan, automatically validating multiple register blocks in full-chip regression.

NVIDIA GRAPHICS Bangalore, IN
ASIC Intern *Jul 2023 - Dec 2023*
- Enhanced the UVM SystemVerilog USB2/3 TestBench by removing 10% of unwanted DUT dependencies in TB, improving modularity, streamlining the USB BFM agent, and isolating XHCI dependencies to separate host-controller to descriptor conversion flow.
- Led migration of USB BFM agents from USB unit TB to SOCv TB, replacing the C-based SoC-level test flow with a unified UVM environment and eliminating 16 weeks of SOC team's effort per chip required for separate SOC-level USB verification TestBench setup.
- Integrated Perl-based wrappers with Verilog TB code, boosting scalability and reusability across SOC and USB TestBenches, and pioneered release of the first verification component as CRR package in xUSB IP verification team.

SAMSUNG SEMICONDUCTOR INDIA RESEARCH Bangalore, IN
Summer Intern *Jun 2022 - Jul 2022*
- Optimized width-to-length (W/L) ratio of CMOS transistors using Cadence Virtuoso and HSPICE, to enhance switching speed and reduce power consumption, while ensuring noise margins and signal integrity were preserved.
- Implemented a two-stage operational amplifier design, achieving an optimal Gain-Bandwidth Product (GBW) for high-frequency performance with minimal distortion of less than 2% and a stable closed-loop gain.

PROJECTS

Extending ESP to Non-Mesh NoC Topologies, *Columbia System-Level Design Group x IBM Research* *Jan 2025 - May 2025*
- Implemented a SV ring-NoC router design with dynamic clockwise/anticlockwise path selection and developed a pseudo-random traffic generator TB, reducing area, simplifying routing and arbitration complexity, and lowering packet latency in small-scale deployments.
- Integrated ring-NoC into ESP's VHDL wrappers, replacing the legacy 2D mesh with a ring topology with a 3-port (Local/East/West) ring topology by removing North/South ports. Implemented a Hamiltonian-mapping to translate mesh grid coordinates into ring IDs.
- Prototyped on a FPGA with 4-tile (memory, I/O, Stratus-HLS FFT accelerator, Ariane CPU), exercised DMA transfers in various cache-coherency modes to validate against golden-reference FFT outputs—yielding 3% lower latency and 12% reduced resource utilization.

Performance Characterization of Vortex GPGPU Microarchitecture, *Columbia ICE Research Lab* *Jan 2025 - May 2025*
- Developed and integrated custom RTL performance counters in SystemVerilog to quantify SIMT (warp) efficiency and instruction-buffer backpressure stalls, enabling in-depth analysis of warp utilization and pipeline behavior in RISC-V based Vortex GPGPU rtlsim.
- Built a Python-based automation framework script to compile, execute, and extract performance counters (core, memory, SIMT) across different thread/warp configurations, input sizes, and OpenCL workloads, exporting CSVs for architectural bottleneck characterization.

Formal Verification of AHB2APB Bridge, *Columbia University* *Nov 2024 - Dec 2024*
- Verified all FSM states and transitions of the DUT, achieving 100% coverage of reset behavior, state changes, and protocol compliance for the ARM AMBA AHB-to-APB bridge leveraging Cadence JaseperGold formal verification tool for assertion based model checking.
- Identified and resolved a transition failure in the WENABLEP state, one of 18 possible transitions across 8 FSM states, using waveform analysis to ensure accurate state transitions and robust design functionality according to ARM AMBA specifications.

Digital FIR Filter Accelerator Design, *Columbia University* *Oct 2024 - Dec 2024*
- Designed a 64-tap FIR filter in Verilog by developing and integrating core components including FIFO, ALU, and CMEM (SRAM) for coefficient storage. Simulated and verified functionality using QSim and synthesized the RTL netlist using Synopsys DC.
- Performed static timing analysis and power estimation using Synopsys PrimeTime to meet timing and power goals. Validated the Verilog implementation against a MATLAB golden model to ensure functional correctness and performance alignment.

Network-On-Chip Verification, *BITS Pilani* *Jan 2024 - Apr 2024*
- Designed a SV-based UVM Testbench for NoC mesh topologies, scaling it from lower order sizes (2x2, 3x3) to larger meshes (9x9, 12x12, 14x14). Increased functional coverage from 73% to 97% using coverage bins, assertions, parameter tuning, and address settings.
- Benchmarked time and coverage of metaheuristic methods, including Particle Swarm Optimization (PSO), Genetic Algorithms (GA), and Differential Evolution (DE) against traditional UVM SystemVerilog TB for mesh topology, demonstrating faster convergence.

SKILLS

Programming Languages: SystemVerilog, Verilog, Perl, Python, C, SystemC, Tcl, VHDL
Tools and Frameworks: UVM, Vivado, JasperGold, Cadence Virtuoso, AWR Microwave, SPICE, Synopsys VCS/Verdi, Modelsim
General: Git, Vim, Linux Terminal, UNIX, SSH, Microsoft Office Suite, Confluence, Bash, Makefile, OOP, APR scripts

LEADERSHIP AND ACHIEVEMENTS

Merit Scholarship at BITS Pilani, Elected EE Department Rep at Columbia EGSC, Published 2 first-author papers on IEEE Xplore Library