Laird™
CONNECTIVITY

User Guide

BL5340 Development Kit

Part # 453-00052-K1 and 453-00053-K1

Version 1.0

REVISION HISTORY

Version	Date	Notes	Contributor(s)	Approver
1.0	1 Sept 2021	Initial version	Raj Khatri	Jonathan Kaye

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1 Overview

The Laird Connectivity DVK for the BL5340 modules series provides a platform for rapid wireless connectivity prototyping, providing multiple options for the development of Bluetooth Low Energy (BLE), 802.15.4 and Near Field Communication (NFC) applications.

The development kit is designed to enable customers to test and validate all the hardware interfaces of the BL5340 module and support the rapid development of application software using either Zephyr RTOS or Nordic Semiconductor nRFConnect SDK.

The BLE Gateway out-of-box demo firmware for the DVK-BL5340 development board comes pre-loaded with GA1 (v5.1.9) of the BLE Gateway Firmware. See the following links for more information:

- Firmware details: https://github.com/LairdCP/BL5340_Firmware_Manifest/
- Download releases: https://github.com/LairdCP/BL5340_Firmware_Manifest/releases
- Out-of-box demo documentation: https://github.com/LairdCP/BLE_Gateway_Firmware

This document is applicable to the version of development board which has PCB silk screen text DVK-BL5340-**2.0**. This document should be read in association with the DVK-BL5340 Schematics available on the BL5340 product page, Documentation section: https://www.lairdconnect.com/bl5340-series

2 Laird Connectivity BL5340 Development Kit Part Numbers

Part Number	Product Description
453-00052-K1	Development kit for BL5340 Multi-Core / Protocol - Bluetooth® + 802.15.4 + NFC Module (Nordic nRF5340) – Integrated antenna
453-00053-K1	Development kit for BL5340 Multi-Core / Protocol - Bluetooth® + 802.15.4 + NFC Module (Nordic nRF5340) - Trace pin (Ext antenna)

Applicable to the following BL5340 module part numbers:

Part Number	Product Description
453-00052	BL5340 series - Multi-Core / Protocol - Bluetooth® + 802.15.4 + NFC Module (Nordic nRF5340) – Integrated antenna
453-00053	BL5340 series - Multi-Core / Protocol - Bluetooth® + 802.15.4 + NFC Module (Nordic nRF5340) – Trace pin

3 Package Contents

All kits contain the following items:

Development Board	The development board has the required BL5340 module soldered onto it and exposes all available hardware interfaces.
Power Options	▪ USB cable (x2) – Type A to micro type B. The cable also provides serial communications via the FTDI USB – RS232 converter chip on the board. ▪ DC barrel plug for connection to external power supply (5.5 VDC max)
Two-pin jumpers for pin headers (5)	Five jumpers for 2.54 mm pitch headers used on BL5340 development board.
Fly leads (6)	Supplied (1 by 1 female to female jumper cable) to allow simple connection of any BL5340 module pins (available on plated though holes or headers on J44, J47, J48, J41, J29, J1, J12, J1, J5, J17, J21, J6 and J36).
External BLE	Supplied with development kit part # 453-00053 only.

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dipole antenna	External antenna, 2 dBi, FlexPIFA (Laird Connectivity part #001-0022) with integral RF coaxial cable with 100 mm length and IPEX-MHF4 compatible RF connector.
External NFC antenna	Laird Connectivity NFC flexi-PCB antenna – Part # 0600-00061
TFT LCD display	Mounted LCD display MPN created by selecting below options: 2.8"TFT Touch Shield for Arduino w/Capacitive Touch Screen Module (buydisplay.com) ▪ **2.8"TFT Touch Shield for Arduino w/Capacitive Touch Screen Module** ▪ **Interface:** Pin Header Connection-4-wire SPI +USD0.33 ▪ **Power Supply (Typ.):** VDD=3.3V ▪ **Touch Panel(attached by default):** 2.8" Capacitive Touch Panel +USD5.36 ▪ **Font Chip (refer to Font Chip Datasheet):** ER3300-1 +USD1.30
BLE sensor	Sentrius BT510 (Laird Connectivity part # 455-00083), http://www.lairdconnect.com/bt510
DVK 'Legs'	4 x stand-off and 4 x associated nuts

4 BL5340 Development Kit – Main Development Board

This section describes the BL5340 development board hardware.

The BL5340 development board is a universal development tool that highlights the capabilities of the BL5340 module. The development kit is supplied in a default configuration which should be suitable for multiple experimentation options. It also offers several header connectors that help isolate on-board sensors and UART from the BL5340 module to create different configurations. This allows you to test different operating scenarios.

The board allows the BL5340 series module to physically connect to a PC via the supplied USB cable for development purposes. The development board provides USB1-to-Virtual COM port (UART0 on BL5340) conversion through a FTDI chip (U27) – part number FT232R. Any Windows PC (XP or later) should auto-install the necessary drivers; if your PC cannot locate the drivers, you can download them from http://www.ftdichip.com/Drivers/VCP.htm The development board also provides second USB2-to-Virtual COM port (UART1 on BL5340) conversion through the Atmel chip (U14).

4.1 Key Features

The BL5340 development board has the following features:

- BL5340 series module soldered onto the development board
- The following power supply options for powering the development board:
  - USB (micro-USB, type B), either USB1, USB2, USB3 connectors
  - External DC supply CON1(3.5-5.5V) or battery connector (P2)
  - USB3 (micro-USB, type B) –for direct use of BL5340 USB nRF5230 interface as well
- Powering the BL5340 module in Normal Voltage mode (OPTION1) via selection switch (SW7). Regulated 3.3V or Regulated 1.8V via selection switch (SW5).
- Powering the BL5340 module in High Voltage mode (OPTION2) via selection switch (SW7). Regulated 2.5V or optional external voltage (from J28 or P2) anywhere between 2.5V to 5.5V for the High Voltage mode (via J28) via selection switch (SW8).
- USB1 to UART bridge (FTDI chip, U27)
- BL5340 can have multiple UARTS, on DVK-BL5340 we have 2 UARTs that can be interfaced to:
  - USB1 (PC) using the USB-UART0 bridge (U27 FTDI chip)
  - External UART source (using IO break-out connectors J1 – No-Pop, Plated Through Holes) when the development board is powered from a DC jack (CON1) or from USB1 (when jumper fitted in J35).
  - USB2 (PC) using the Atmel MCU (U14) provided USB2-UART1 bridge (from code running in Atmel U14 chip)

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  - Atmel MCU by use of an analog switch to route the BL5340 UART1. USB2 (into Atmel MCU U14) to UART1 to connect to the UART1 of the BL6340 (via closed DIP switch S7).
- Current measuring options (BL5340 module only):
  - Pin header J7, J9 (Ammeter). Cut closed solder bridge SB1 to use J7, cut closed solder bridge SB13 to use J9.
  - 10R Series resistor for differential measurement (oscilloscope) via open solder bridges.
- IO break-out 2.54 mm pitch pin header connectors (plated through-holes) that bring out all GPIO of the BL5340 module – on which various interfaces UART0, UART1, SPI, SPIM4, QSPI, I2C, GPIO, AIN, NFC – and allow for plugging in external modules/sensors.
- Pin headers jumpers or DIP switches that allow the on-board sensors to be disconnected from BL5340 module (by removing jumpers or DIP switches).
- Multiple on-board sensors:
  - I2C devices
    - 3-axis accelerometer chip (U16) via DIP switch (DIP switch S12 closed by default)
    - Temperature/Pressure/Humidity chip (U5) via 2-pin headers (jumper fitted by default in J3 and J4)
    - EEPROM chip (U2) via 2-pin headers (jumper fitted by default in J11 and J6)
    - RTC chip (U16) via 2-pin headers (jumper fitted by default in J17 and J21)
    - DAC chip (U17) via 2-pin headers (jumper fitted by default in J5 and J10)
    - Port Expander chip (U31) via 2-pin headers (jumper fitted by default in J16 and J18, J22) on which are connected:
      - Four buttons (S1, S2, S9, S10) and
      - Four LEDs (LED1, LED2, LED3, LED4)
    - LCD display assembly (on CON4) I2C interface 2-pin headers (jumper fitted by default in J24, J26)
  - SPI devices and High-Speed SPI (SPIM4) device
    - SD card SPI connector (CON9) via 4-pin DIP switch (DIP switch S6 closed by default)
    - Ethernet to SPI chip (U4) via 4-pin DIP switch (DIP switch S5 closed by default)
    - LCD display assembly (plugged into CON4) SPIM4 (High speed SPIM4) interface level shifted and via DIP switches (DIP switches S8, S11 closed by default)
  - QSPI device (Flash) chip (U1) via closed solder bridges (by default)
- One reset button S3 (via U25 level shifter)
- One BOOT button S4 (connected to P1.11 of BL5340)
- NFC antenna connector (CON2) on-board development board for use with supplied flexi-PCB NFC antenna (0600-00061, see datasheet)
- *Optional* external 32.768 kHz crystal (Y3) circuit (Not required for operation of the BL5340). The 32.768 kHz crystal oscillator circuit requires load capacitor inside the nRF5340 chipset to be enabled in software (and for Y3 32.768kHz part, nRF5340 provided load capacitance of 7pF should be used). The Y3 crystal is connected by default BL5340 by closed solder bridges.
- *Optional* external serial (QSPI) flash chip (U1). Not required for operation of the BL5340; is connected by closed solder bridges by default.
- Access to BL5340 Serial Wire Debug (SWD) 2-wire interface (JTAG) on P1 or J46 via analog switch U24
- On-board SWD (JTAG) programmer circuitry formed by Atmel MCU (U14) that transforms USB2 to SWD interface (which then connects to BL5340 module SWD interface)
- FW upgrade or application loading HW capability:
  - Via SWD (USB2 to BL5340 SWD) using on-board SWD (JTAG) programmer circuitry (U14 Atmel MCU) on the BL5340 Development Kit
  - Via UART0 (using the U27 FTDI USB1-UART0)
  - Via UART1 (using the U14 Atmel MCH USB2-UART1)

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5 Understanding the Development Board

Development board 453-00053-K1 (fitted with 453-00052 BL5340 series - Multi-Core / Protocol - Bluetooth® + 802.15.4 + NFC Module (Nordic nRF5340) – Integrated antenna)

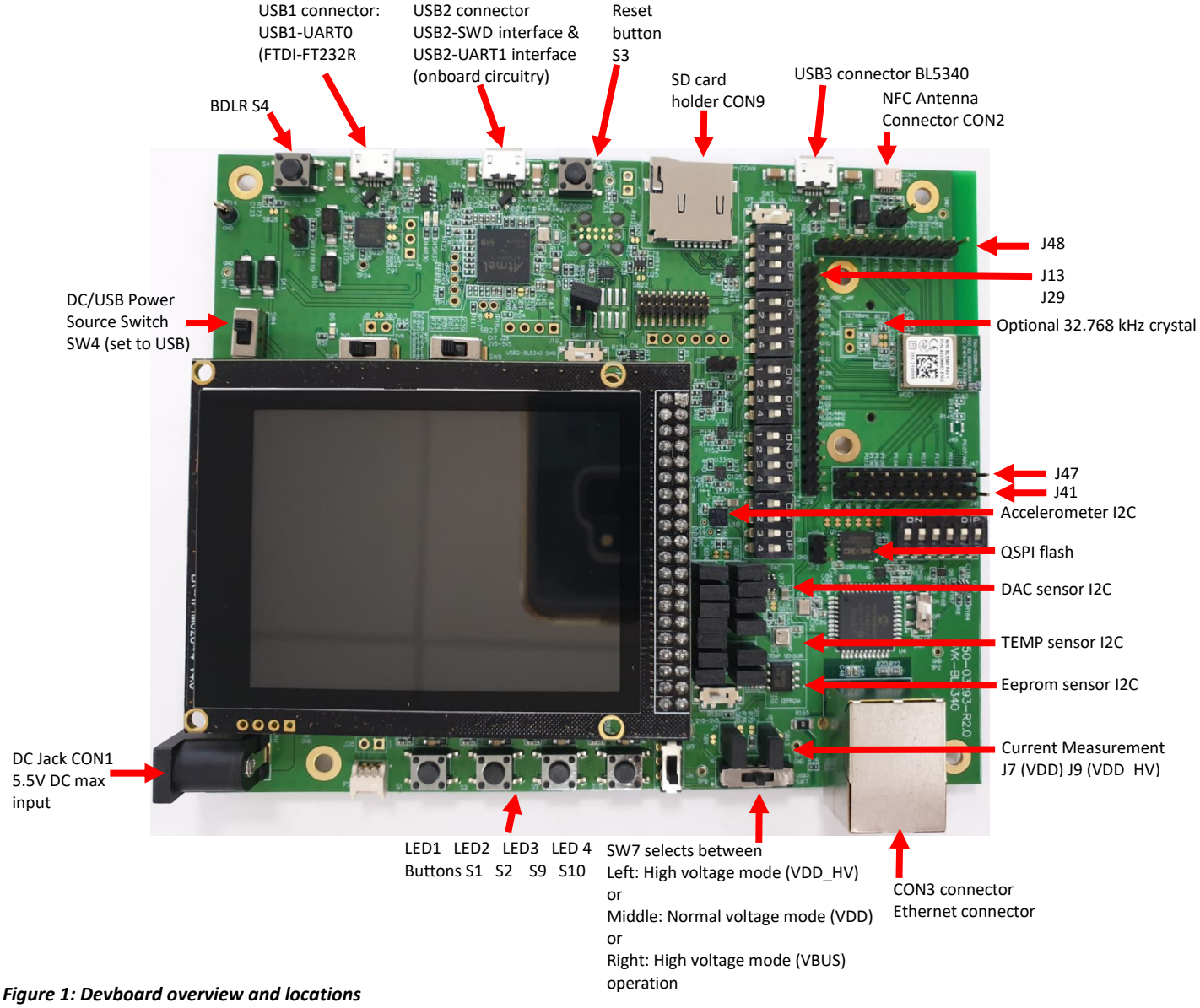

Figure 1: Devboard overview and locations

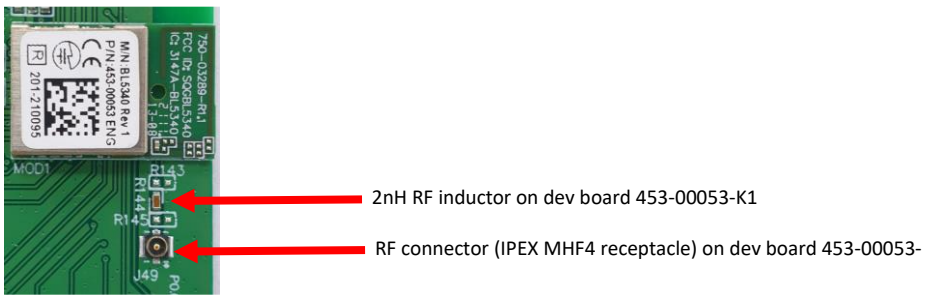

Figure 2: Zoomed area of development board 453-00053-K1 (fitted with 453-00052 BL5340 series -– RF Trace pad variant) with mandatory RF GCPW RF 50 Ohms track and series 2nH RF inductor (R144)

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5.1 BL5340 Default Configuration and Jumper Settings

Important! To ensure correct out-of-the-box configuration, the **BL5340** development board switches, DIP switches and jumpers must be configured as shown in Figure 3.

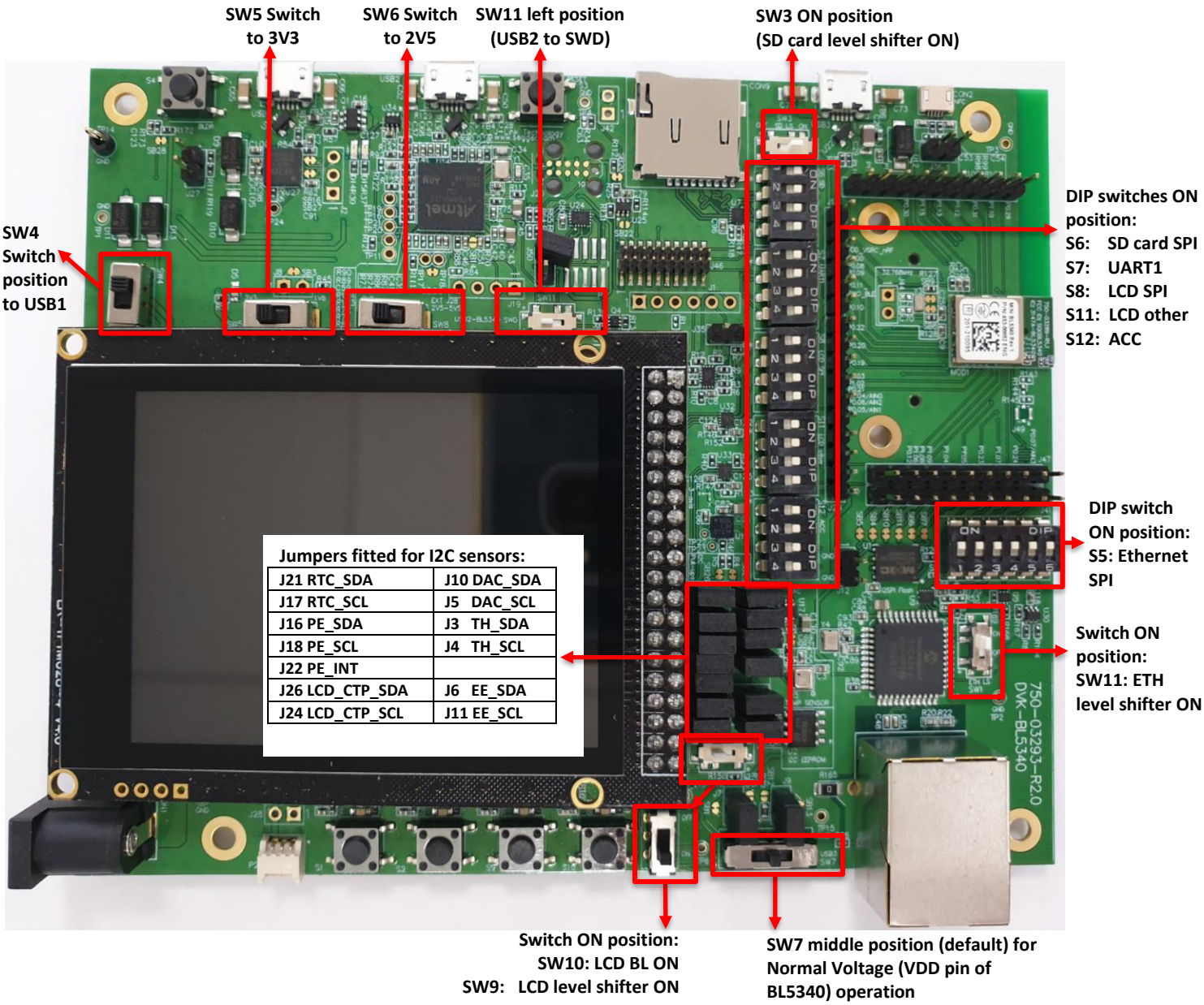

Figure 3: Correct BL5340 development board 453-00052-K1 or 453-00053-K1 jumper and switch settings (image for 453-00052)

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6 Functional Blocks

6.1 Power Supply

Figure 4 shows the BL5340 development board Power Supply block.

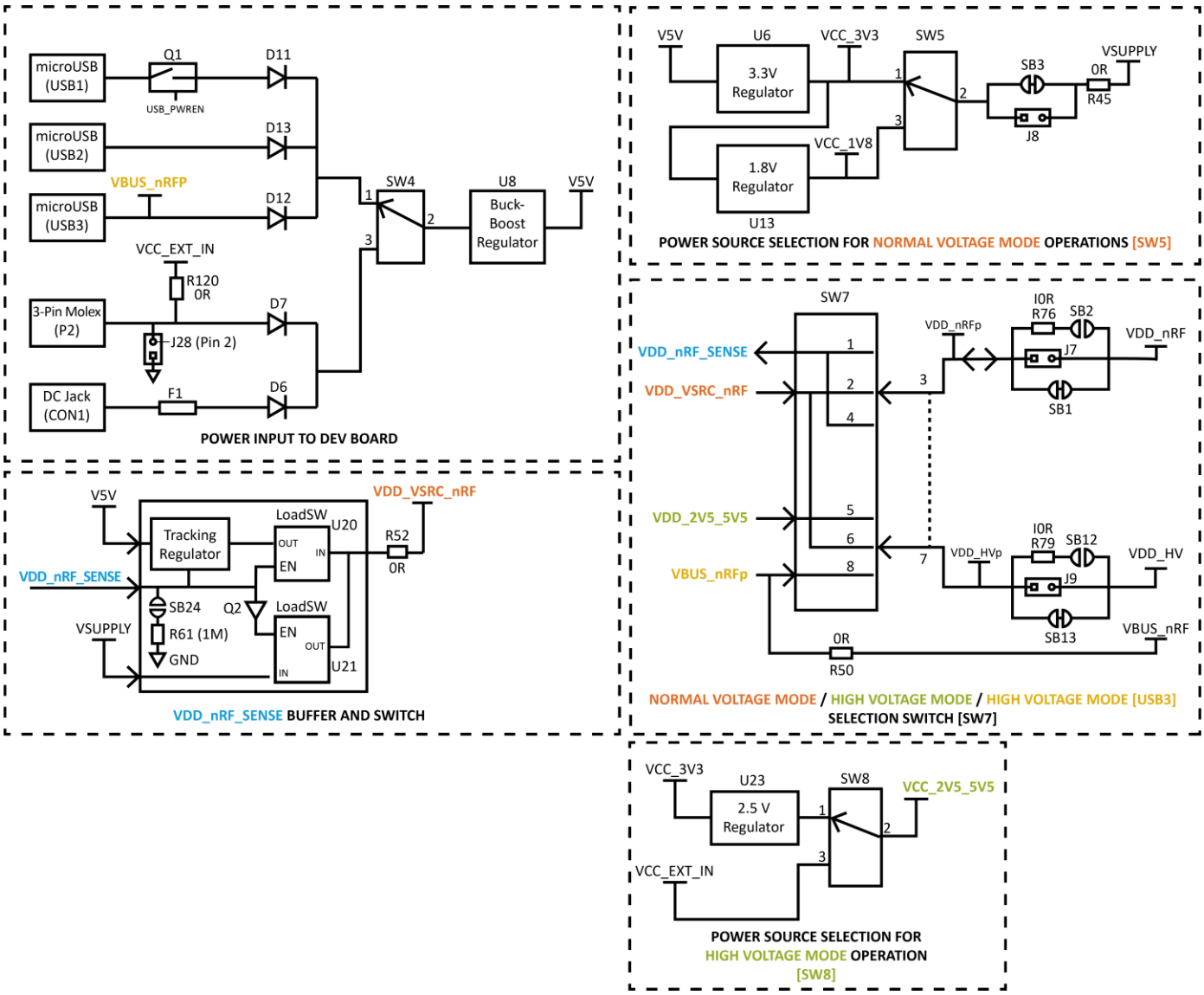

Figure 4: BL5340 development Kit power supply

There are five options for powering the development board:

- USB1 USB type micro-B connector – If it requires the FTDI USB1-UART (of BL5340) path
- USB2 USB type micro-B connector – If it requires the Atmel USB2-SWD (of BL5340) path
- USB3 USB type micro-B connector – If it requires the USB3 to USB (of BL5340) path
- External DC supply (2.5V-5.5V), into DC jack connector (CON1),

The external power sources are fed into selection switch SW4 which allows a selection between either USB sources or the DC jack/J28.

All the external power sources listed above are buck-boost regulated to a fixed 5V on the development board.

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The BL5340 module has the following power supply pins:

- VDD pin (operating range of 1.7V to 3.6V) – Used for Normal Voltage mode
- VDD_HV pin (operating range of 2.5V to 5.5V) – Used for High Voltage mode
- VBUS pin (operating range of 4.35V to 5.5V) – Used for BL5340 USB mode

It can be powered in the following ways:

- **Normal Voltage mode operation**

  Option 1 – Normal voltage power supply mode entered when the external supply voltage is connected to both the VDD and VDD_HV pins (so that VDD equals VDD_HV). Connect external supply within a 1.7V to 3.6V range to the BL5340 VDD and VDD_HV pins.

  For Normal Voltage mode operation, the BL5340 Development Board power supply section generates the following:

  - Regulated 3.3V
  - Regulated 1.8V

  Via selection switch SW5 (default is 3.3V position), you can select whether to use 3.3V or 1.8V.

- **High Voltage mode operation**

  Option 2 – High voltage mode power supply mode (using BL5340 VDD_HV pin) entered when the external supply voltage in ONLY connected to the VDD_HV pin and the VDD pin is not connected to any external voltage supply. Connect external supply within a 2.5V to 5.5V range to the BL5340 VDD_HV pin. Leave the BL5340 VDD pin unconnected.

  For High Voltage mode operation, the BL5340 Development Board power supply section generates the following:

  - Regulated 2.5V
  - (or inject external voltage into J28pin1 up to 5.5V)

  Via selection switch SW8 (default is 2.5V position), you can select whether to use 2.5V or 4.5V.

  Option 3 – High voltage mode with voltage via USB3

  - For either option, if you use the BL5340 USB interface, the BL5340 VBUS pin must be connected to an external supply within the range of 4.35V to 5.5V.

The BL5340 development board power supply section is designed to cater to the above. Follow the following steps:

1. Set SW7 – Select one of the following three positions:
   - High Voltage mode operation and BL5340 USB (connect USB cable to USB3 connector) – Top position. Source from USB3.
   - Normal Voltage mode operation – Middle position (default). Source from SW5.
   - High Voltage mode operation – Bottom position. Source from SW8.
2. Depending on chosen SW7 position, select one of the following three positions:
   - Plug in USB cable into USB3 – If SW7 is set to Top position.
   - SW5 (either 3.3V or 1.8V) – Default SW5 on 3.3V position. If SW7 set to Middle position.
   - SW8 (either 2.5V or 5.5 (from J28) – Default SW8 on 2.5V position. If SW7 set to Bottom position.

Table 1 summarises the dev-board on-board power sources and switch positions.

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Table 1: Dev board power sources and switch positions

Selection Switch SW7 positions (silk screen) / Source / Voltage Operating mode		Dev Board Power Supply Switch Positions		
		SW5 Selects between 3.3V or 1.8V 	SW8 Selects between 2.5V or 5.5V (J28) 	Connect USB cable into USB3
		Present selected voltage to the BL5340 pin		
		BL5340 VDD pin	**BL5340 VDD_HV pin**	**BL5340 VBUS pin**
SW7 Right position Silkscreen: "USB3" (source from USB3) High Voltage Mode with BL5340 USB used (USB3)		Note 1:	USB3 voltage	USB3 voltage
SW7 Middle position – Silkscreen: "SW5" (Source from SW5, **Error! Reference source not found.**) Normal Voltage Mode		Decided by SW5 (default SW5 on 3.3V position)	N/A	N/A
SW7 Left position – Silkscreen: "J28 (SW8)" (Source from SW8) High Voltage Mode		Note 1	Decided by SW8 (default SW8 on 2V5 position)	N/A

Power Source and Switch Location Notes:

Note 1: No voltage is presented to VDD pin, as in High voltage mode, the VDD pin becomes an output voltage pin. It can be used to supply external circuitry from the VDD pin. Before any current can be taken from the BL5340 VDD pin, this feature must be enabled in the BL5340. Additionally, the VDD output voltage is configurable from 1.8V to 3.3V with possible settings of 1.8V, 2.1V, 2.4V, 2.7V, 3.0V, and 3.3V. The default voltage is 1.8V.

Note: The development board for BL5340 has on-board circuitry to allow access to BL5340 SWD interface (via USB connector USB2). Use USB2 only to power the development board when BL5340 SWD interface is needed. Refer to SWD Interface. When USB2 is used, USB1 does not need to be used for DC power.

One special feature of the development board's power supply is it resolves whether the BL5340 VDD pin is an input supply pin (in Normal Voltage mode) or becomes an output supply voltage pin (in High Voltage mode).

Power circuitry net names

On the development board, the power circuity net names are as follows:

- VCC_3V3 – Supplies regulated 3.3V power to the FTDI chip as well as temperature sensor (U1).
- VSUPPLY – Supplies regulated 3.3V or 1.8V via selection switch SW5 to net VSUPPLY which is connected to input of Load switch U21.

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- VCC_2V5_5V5 – Selection switch SW8 supplies either regulated 2.5V or externally injected 5.5V (J28) can be used for when BL5340 is powered in High Voltage mode (using the VDD_HV pin).
- V5V – The main development board power supply's buck-boosted output (that is 5V) supplies a discrete regulator made up of Q3 and U19
- U19 OpAmp drives Q3 to generate regulated voltage (that then is connected to input of load switch U20) that tracks control signal VDD_nRF_SENSE.
- VDD_VSRC_nRF – Supplies the FTDI chip IO and all other sensors and circuitry. VDD_VSRC_nRF is generated from load switches U20 or U19.
- VDD_nRF_SENSE – Used as control signal to drive control pin of load switches U20 and U19. The source of VDD_nRF_SENSE is the BL5340 VDD pin. When BL5340 is powered in High Voltage mode (using the VDD_HV pin), the BL5340 VDD pin becomes an output voltage supply.
- VDD_nRFp – Supplies the BL5340 series module only. Current measuring block on the development board only measures the current into power domain VDD_nRFp (that is current going into header J7 pin 1).
- VDD_nRF – Supplies the BL5340 series module only and is to the current that has come out of the current measuring block on the development board on header connector J7 pin 2.
- VDD_HVp – Supplies the BL5340 series module only. Current measuring block on the development board only measures the current into power domain VDD_nRFp (that is current going into header J9 pin1).
- VDD_HV – Supplies the BL5340 series module only and is to the current that has come out of the current measuring block on the development board on header connector J9pin2.
- VBUS_nRFp – This voltage from USB cable plugged into connector USB3, that is directly fed to BL5340 VBUS pin (via 0R resistor R50) on net VBUS_nRF.

TIP: If operating the development board at temperature of 75°C or above there is an issue related to Q2 (it starts turning on) which results in VDD_VSRC_nRF supplying heading towards 0V or turning off. To overcome this issue 75°C or above issue, bridge with solder the open-solderbridge SB24 which connects 1MOhms resistor to ground onto the gate of Q2. The 1-MOhm resistor results in extra current consumption of (= VDD_nRF_SENSE/1Mohms) added to any current measurements made when operating the BL5340 module on devboard in High voltage mode (VDD_HV pin) ONLY which is when SW7 in Top position or Bottom position (and in that case by default VDD_nRF_SENSE is 1.8V). Figure 5 shows PCB location of SB24 and schematic showing SB24.

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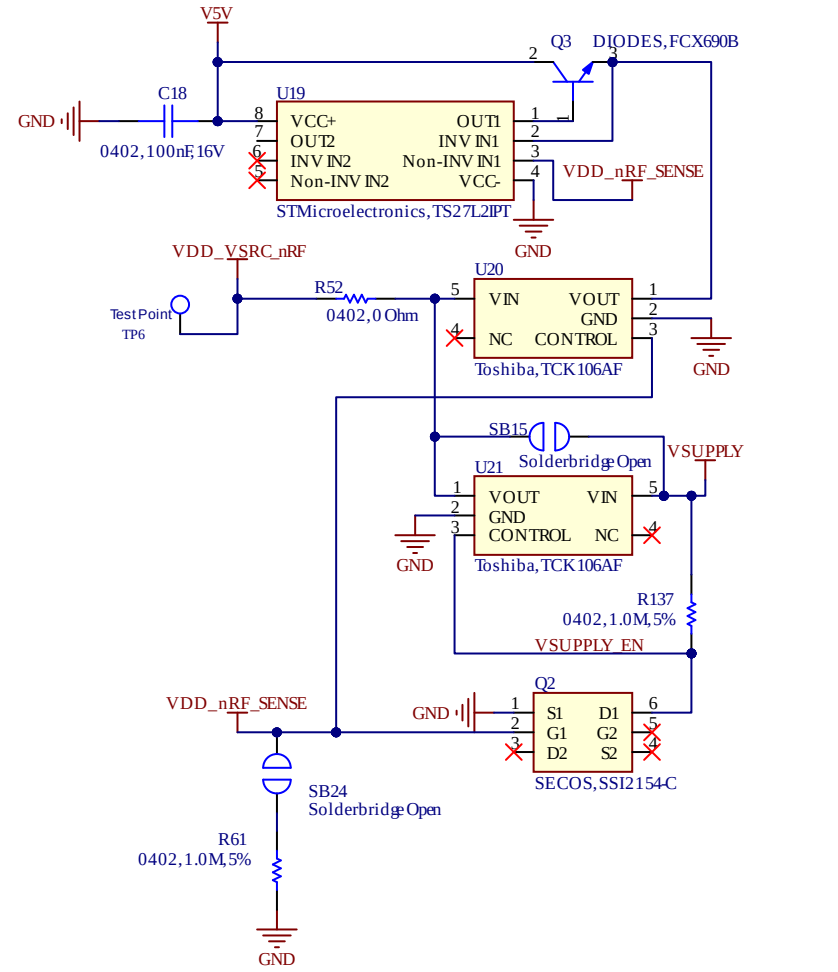

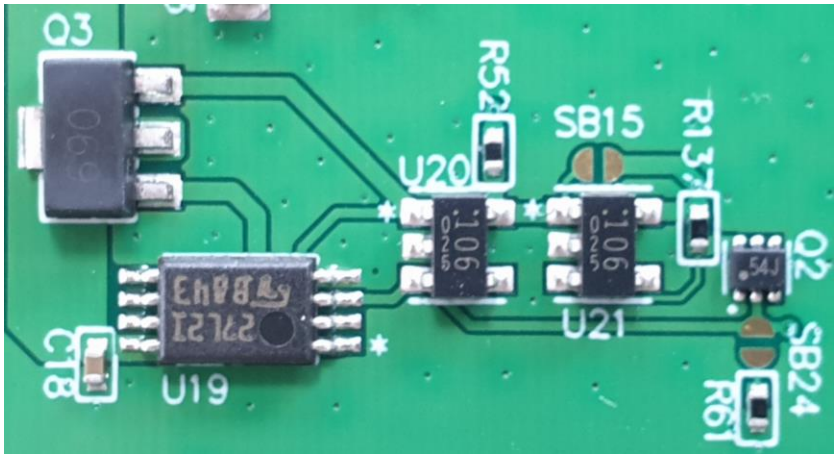

Figure 5: Schematic and PCB location of SB24

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6.2 Reset Button

The development board has a reset button (S3) with the net name RESET_BLE_BUTTON. The RESET_BLE_BUTTON (is active low when S3 pushed down) is routed to the BL5340 module nRESET_BLE pin via an AND gate (U25) which also acts as a buffer and level shifter U25. The placement of the S3 reset button and circuitry is shown in Figure 6.

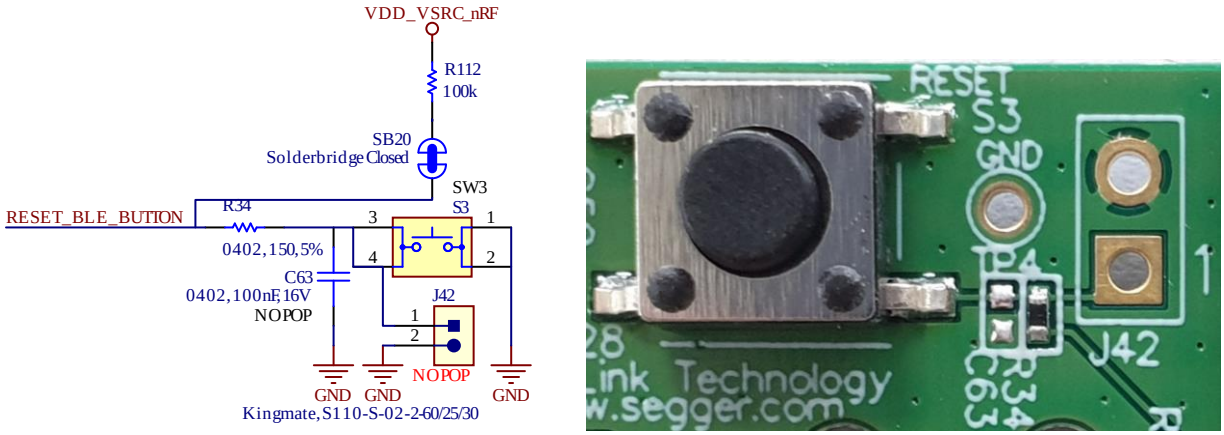

Figure 6: Reset button placement

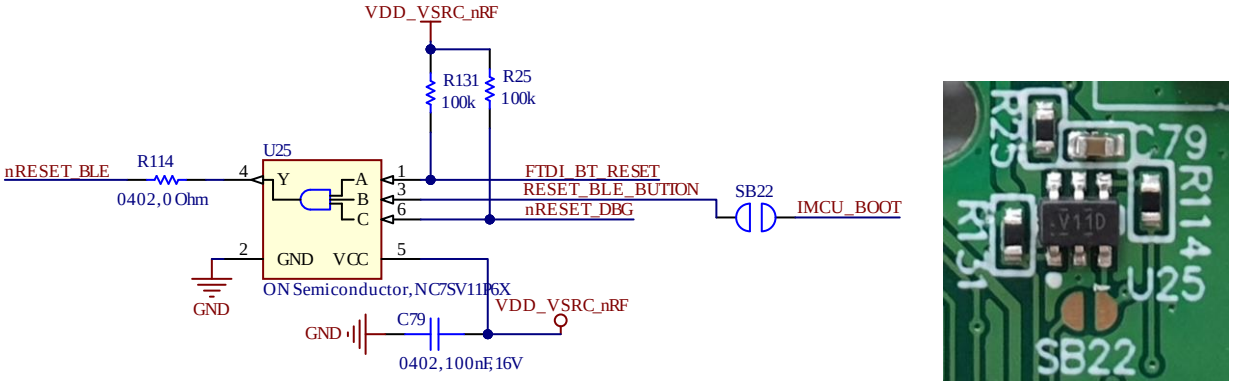

Figure 7: Reset button schematic and routing through U25 AND gate buffer PCB placement

BL5340 module reset (nRESET_BLE) can be driven 3 sources (via AND gate U25):-

- reset button S3 (net name RESET_BLE_BUTTON)
- FTDI chip U27 DCD pin (net name FTDI_BT_RESET)
- either Atmel MCU USB2-SWD circuitry U14 (OB_RESET) or P1 (and J46) connector (nRESTE_EXT) via analog switch U24 (net name nRESET_DBG), see section 6.3 SWD (JTAG) Interface

6.3 SWD (JTAG) Interface

The development board provides access to the BL5340 module two-wire SWD interface on P1 via analog switch U24. This SWD interface is REQUIRED for customer use for FW programming.

Note: We recommend SWD two-wire interface used for FW loading. Customer MUST wire out the SWD two-wire interface (namely SWDIO, SWDCLK, nReset, GND, and VCC).

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For those customers that require access to BL5340 SWD (JTAG) interface, the BL5340 development board (see Figure 1) has on-board circuitry to allow access to BL5340 module SWD interface (via USB connector USB2). The USB2 to SWD interface conversion circuitry is formed by Atmel MCU (U14).

Figure 9 shows the schematic for SWD on-board circuitry routing via analog switch U24.

When the USB cable is plugged into connector USB2 (the USB cable detection output generates a HIGH for USB_DETECT and USB_DETECTp when switch SW11 is in position 2-1 – the default) and Atmel MCU (U14) SWD (JTAG) signals are routed to the BL5340 SWD interface. This is required to connect the two-wire SWD (JTAG) interface from U14 to the BL5340 SWD (JTAG) interface.

When the USB cable is plugged into connector USB2 and the SW11 is in position 2-3 (Low), there is a LOW on U24 control line USB_DETECTp and the Atmel MCU (U14) SWD (JTAG) signals are routed to connector P1 (which is not populated).

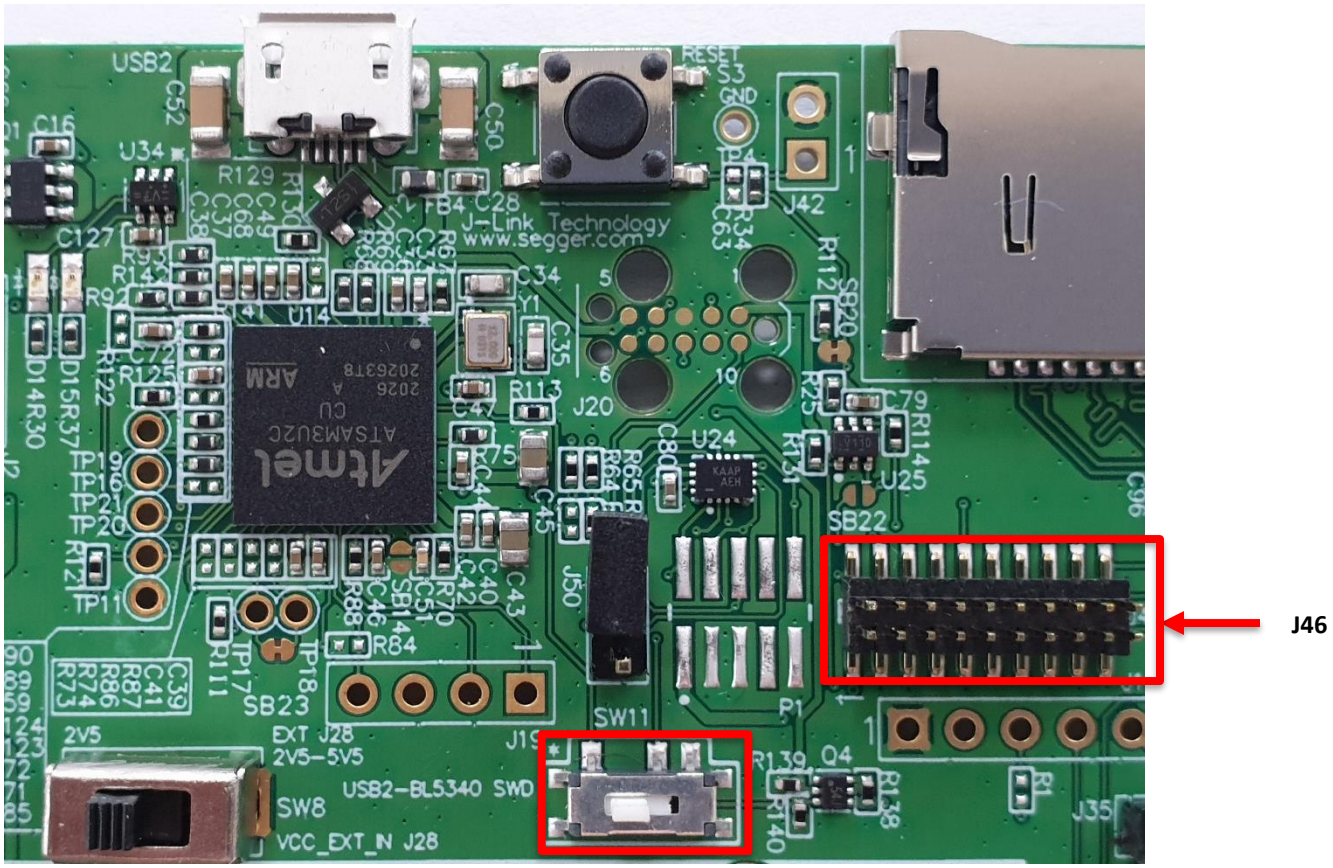

Figure 8: SW11 on development board (showing default SW11 position (left))

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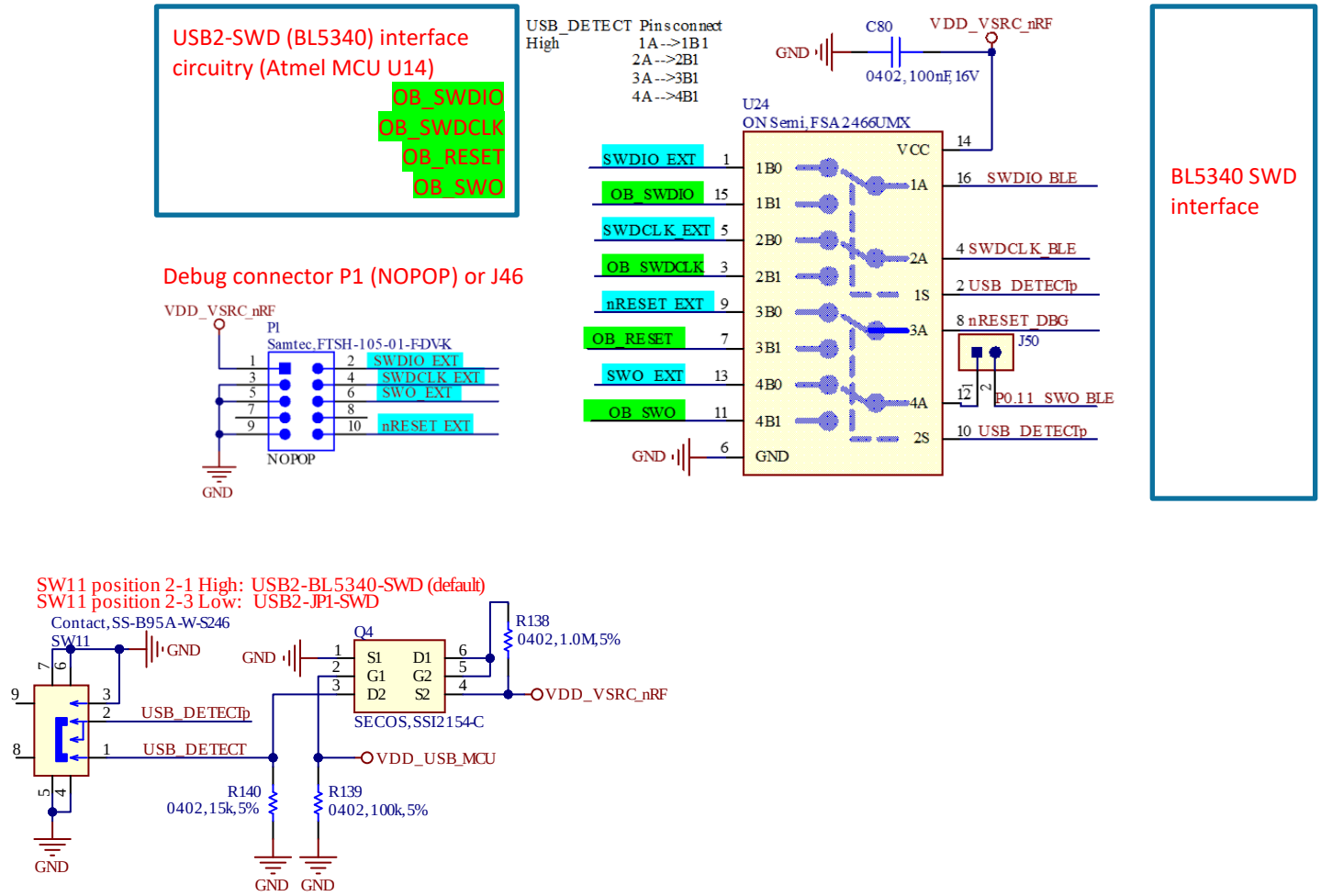

Figure 9: BL5340 SWDS interface via analog selection switch (U24) to either Atmel (U14) SWD to USB2 convertor or to SWD debug connector P1 (and J46)

Table 2 displays the four signals running from BL5340 SWD interface (plus P0.11_SWO and nReset_BLE) via analog selection switch (U24) to either Atmel SWD-USB2 convertor or routing SWD interface to debug connector P1 (and J46).

Table 2: USB U4 USB-SWD to BL5340 SWD signal routing connections

BL5340 (MOD1) pin Net name	**USB cable plugged into USB2 (USB_DETECTp HIGH) and SW11 in position 2-1 HIGH (default)**	**No USB cable plugged into USB2 (USB_DETECTp LOW), by putting SW11 in position2-3 LOW**	**Comments**
	Route SWD Interface BL5340 module to Atmel MCU (U14) to USB2 Net Name	**Route SWD Interface BL5340 module to External debug connector P1 (and J46)**	
SWDCLK_BLE (pin 56)	OB_SWDCLK	SWDCLK_EXT (P1 pin4)	
SWDIO_BLE (pin 55)	OB_SWDIO	SWDIO_EXT (P1 pin2)	
nRESET_BLE (pin 54) via U25 AND gate	OB_RESET	nRESET_EXT (P1 pin10)	
P0.11_SWO_BLE (pin 23) via J50 2pin header	OB_SWO	SWO_EXT (P1 pin6)	No jumper in J50 (default). Must fit jumper into J50 to route out SWO from module.

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P0.11_SWO_BLE is a trace output (called SWO, Serial Wire Output) and is not necessary for programming BL5340 over the SWD interface.
nReset_BLE is necessary for programming BL5340 over the SWD interface.

6.4 Four-wire UART Serial Interfaces

The BL5340 can have multiple four-wire UART's (TX, RX, CTS, RTS). On the DVK-BL5340 development board, 2 UARTs can be interfaced.

Note: The BL5340 module can provide multiple four-wire UART interfaces on the HW and the other four signals (DTR, DSR, DCD, RI), which are low bandwidth signals, can be implemented in FW (if required using any spare digital GPIO pins.

6.4.1 UART0 Interface (on BL5340) Driven by USB1 connector (USB1 to UART0 FTDI bridge chip)

- **USB1 Connector:** The development kit provides a USB Type Micro-B connector (USB1) which allows connection to any USB host device. The connector optionally supplies power to the development kit and the USB1 signals are connected to a USB1-to-UART0 serial converter device (FT232R) when SW4 is set to the USB position.
- **USB1 – UART0:** The development kit is fitted with a (U27) FTDI FT232R USB-to-UART converter which provides USB0-to-Virtual COM port (UART0 on BL5340) on any Windows PC (XP or later). Upon connection, Windows auto-installs the required drivers. For more details and driver downloads, visit the following website: http://www.ftdichip.com/Products/FT232R.htm.
- **UART0 Interface driven by USB1 FTDI Chip:** In normal operation, the BL5340 UART0 interface is driven by the FTDI FT232R USB1-to-UART0 converter (U27).

Note: External UART0 source (using IO break-out connectors J1 – No-Pop, Plated Through Holes) when the development board is powered from a DC jack or from USB1 (when jumper fitted in J35).

The UART0 connection on the DVK-BL5340 and the FTDI IC (U27) are shown in Table 3. Figure 11 explains how the BL5340 series module UART0 is mapped to the breakout header connector J1.

Table 3: UART0 connections on DVK-BL5340

BL5340 (MOD1) pin and available on J1 connector	BL5340 module UART0 assigned	FTDI (U27) IC UART0 via analog switch U15	Comments (no jumper in J35),
P0.20 (pin14)	UART0_TX (output)	USB1_RX0	Analog switch U15 routes to FTDI chip (default)
P0.22 (pin12)	UART0_RX (input)	USB1_TX0	Analog switch U15 routes to FTDI chip (default)
P0.19 (pin15)	UART0_RTS (output)	USB1_CTS0	Analog switch U15 routes to FTDI chip (default)
P0. 21(pin11)	UART0_CTS (input)	USB1_RTS0	Analog switch U15 routes to FTDI chip (default)

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6.4.2 UART1 Interface (on BL5340) Driven by USB2 connector (USB2 to UART1 Atmel MCU bridge chip)

- **USB2 Connector:** The development kit provides a USB Type Micro-B connector (USB2) which allows connection to any USB host device. The connector optionally supplies power to the development kit and the USB2 signals are connected to Atmel MCU (U14) USB2-to-serial converter device when SW4 is set to the USB position.
- **USB2 – UART1:** The development kit is fitted with a (U14) Atmel MCU (U14) USB2-to-UART1 converter (from code running in Atmel U14 chip) which provides USB2-to-Virtual COM port on any Windows PC (XP or later). Upon connection, Windows auto-installs the required drivers (Segger drivers).
- **UART1 Interface Driven by USB2 Atmel chip (U14):** In normal operation, the BL5340 UART1 interface is driven by the Atmel MCU (U14) USB2-to-UART1 converter via DIP switch S7.

Table 4: UART1 connections on DVK-BL5340

BL5340 (MOD1) pin	BL5340 module UART1 assigned	Atmel (U14) IC UART 1	Comments
P1.08 (pin7)	UART1_TX (output)	USB2_RX1	DIP switch S7 position closed to route (default)
P1.10 (pin57)	UART1_RX (input)	USB2_TX1	DIP switch S7 position closed to route (default)
P1.07 (pin8)	UART1_RTS (output)	USB2_CTS1	DIP switch S7 position closed to route (default)
P1.09(pin5)	UART1_CTS (input)	USB2_RTS1	DIP switch S7 position closed to route (default)

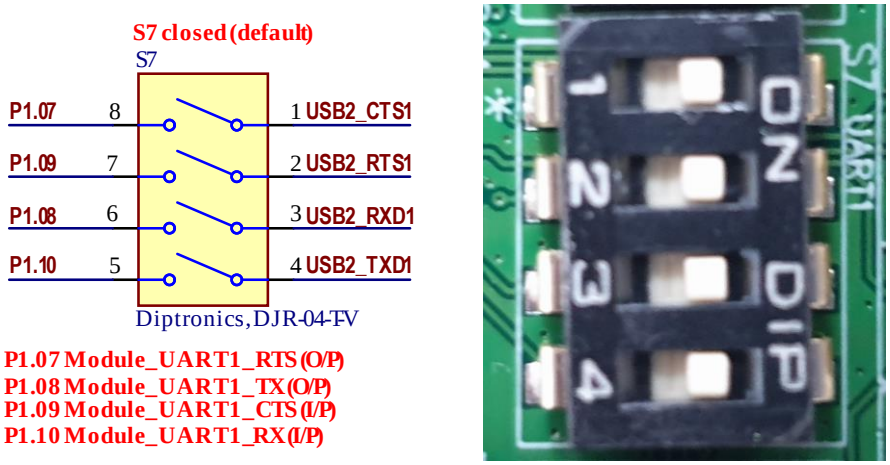

Figure 10: DIP switch S7 schematic and PCB (from USB2 (Atmel U14 USB2 to UART1 convertor) to UART1 (to BL5340))

6.4.3 UART0 Interface (on BL5340) Driven by External Source (J1 connector)

- **UART0 Interface Driven by External UART Source:** The BL5340 module UART0 interface (TX, RX, CTS, RTS) is presented at a 2.54 mm (0.1”) pitch header (J1). To allow the BL5340 UART0 interface to be driven from the breakout header connector (J1), the following must be configured:
  - The development board must be powered from a DC jack (CON1) or inject external supply (J28) and with switch SW4 in DC position.
  - The FTDI device (U27) must be held in reset. This is achieved automatically by removal of the USB cable (from connector USB1), placing SW4 in the DC position or fitting a jumper on J27.
  - Fit a jumper on J35 (to switch the Analog switch U15 and route BL5340 UART0 to J1) when connecting an external UART0 source (for example FTDI USB-UART TTL (3.3V) converter cable) using J1. This isolates the BL5340 UART0 from the on-board USB1-UART0 FTDI device (U27). By default, the jumper on J35 is not fitted, so by default BL5340 UART0 is routed to U27 FTDI FT232R USB1 –UART0 converter (U27).

Note: The BL5340 UART signal levels must always match the supply voltage net VDD_VSRC_nRF of the BL5340.

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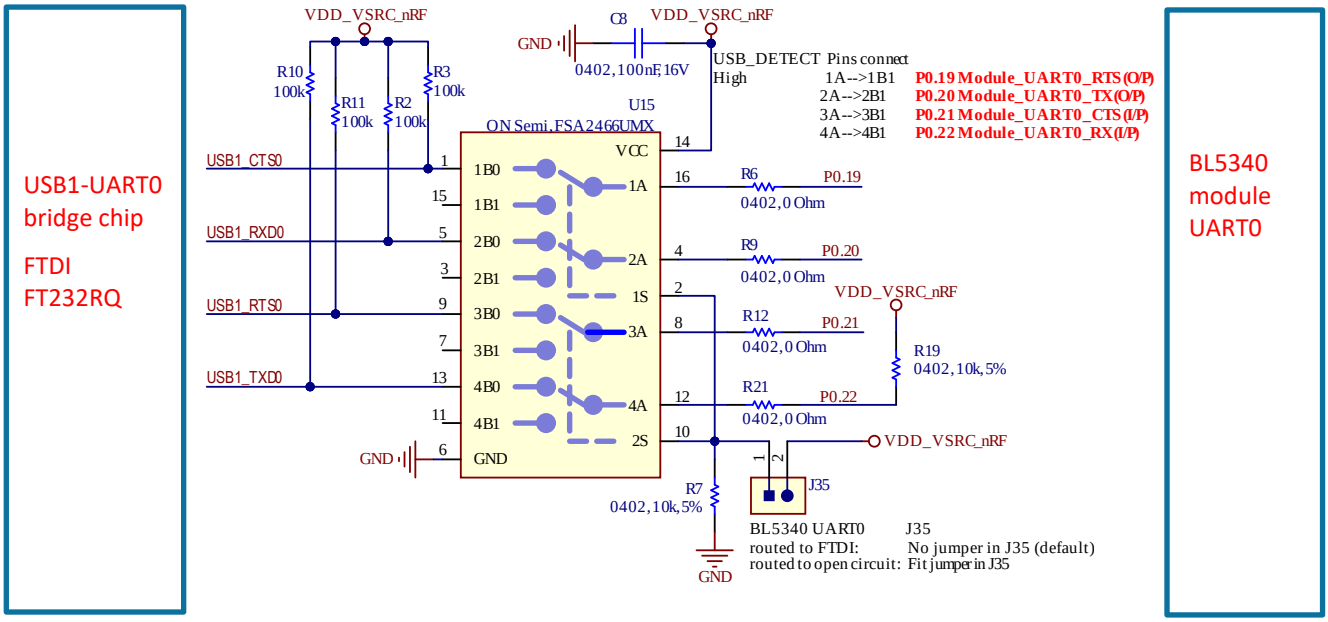
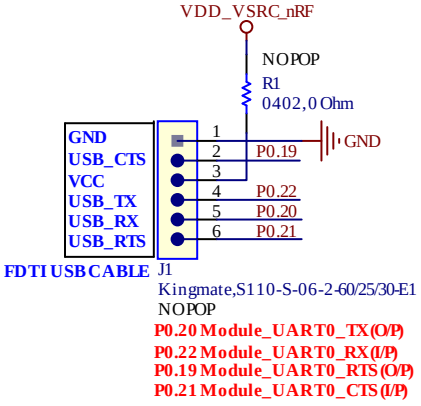


Figure 11: USB1 to UART0 (via FTDI chip U27 on devboard) interface via analog switch U15

J1 pinout is designed to be used with FTDI USB1-UART0 TTL (3.3V) converter cables (found at http://www.ftdichip.com/Products/Cables/USBTTLSerial.htm). One example is FTDI part TTL-232R-3V3.

If the BL5340 on the development board is powered from 1.8V supply, then you must use the 1.8V version of the FTDI USB1-UART0 cable. UART0 signal levels always need to match the supply voltage net VDD_VSRC_nRF of the BL5340 development board.



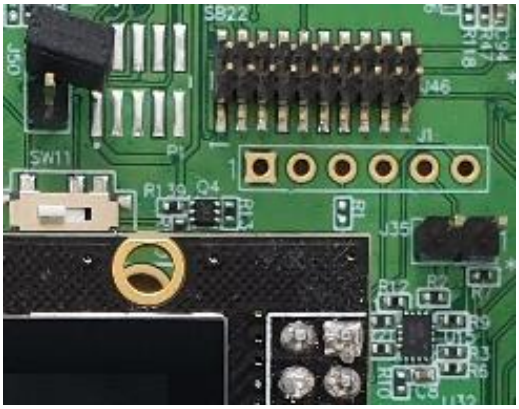


Figure 12: J1 wiring to match FTDI USB-UART0 cable (TTL-232R-3V3 cable)

Fit a jumper in J35 (to switch the Analog switch U15 and route BL5340 UART0 to J1) when connecting an external FTDI USB1-UART0 TTL (3.3V) converter cable using J1.

Fitting a jumper in J35 also allows the BL5340 UART0 to be routed to open circuit.

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7 Software for Communicating to BL5340 UART0 and UART1

The development board connects the BL5340 module to a virtual COM port (UART0 or UART1) of a PC or other device. From a PC, you can communicate with the module using a terminal emulator like PuTTY https://www.chiark.greenend.org.uk/~sgtatham/putty/

This utility allows connections to serial devices using any combination of the communications parameters listed in Table 5. If you want to send commands via UART PuTTY settings can be seen https://developer.nordicsemi.com/nRF_Connect_SDK/doc/latest/nrf/gs_testing.html

Table 5: PuTTY communication parameters for BL5340

Port (Windows)	1 to 255
Port (Mac/Linux)	Any /dev/tty device
Baud Rate	1200 to 1000000 **Note:** Baud rate default is 115200 for BL5340.
Parity	None
Data Bits	8
Stop Bits	1
Handshaking	None or CTS/RTS

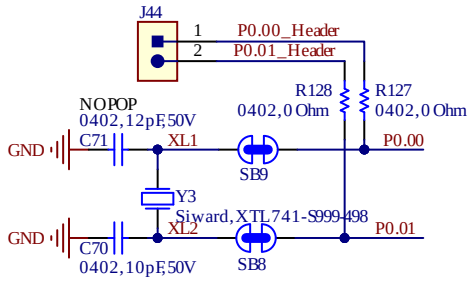
7.1 GPIO Breakout Connectors

Access to all 48 x BL5340 series module signal pins (GPIO = General Purpose Input /Output) is available on 2.54mm pitch header connectors on J41, J47, J29, J13, J48, J36 and plated through hole (for 2.54mm header connector) J44, J1. J12 header is for access to GND.

These breakout connectors can interface to a wide array of sensors via customer developed FW, and the DVK incorporates additional fly-lead cables inside the box to enable simple, hassle-free testing of these multiple interfaces.

Table 6 shows the BL5340 module pins that are brought out to 2.54mm pitch header connectors and plated through holes (suitable for 2.54 mm pitch headers).

Table 6: Module pins exposed by plated through holes

Plated Through Holes or Header Connector	BL5340 Module Signals Exposed
J44 	BL5340 pin plated holes for access: ▪ P0.00 ▪ P0.01 J44 connects to P0.00 and P0.01 via 0R resistors R127 and R128. By default, the optional external 32.768 kHz crystal circuit is connected to BL5340 as SB8 and SB9 are closed. To use J44 to bring out BL5350 GPIO P0.00 and P01.01, cut SB9, SB8 to disconnect Y3.

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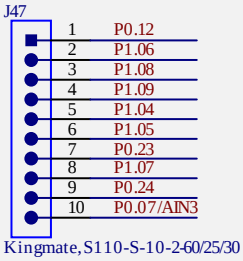
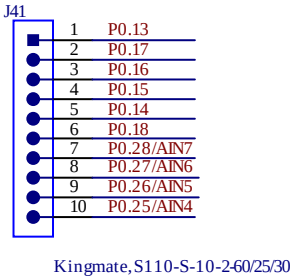
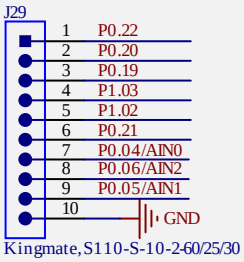
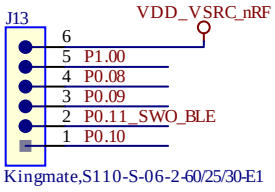
	Plated Through Holes or Header Connector	BL5340 Module Signals Exposed
J47		BL5340 pin header for access: ▪ P0.12 ▪ P1.06 ▪ P1.08 ▪ P1.09 ▪ P1.04 ▪ P1.05 ▪ P0.23 ▪ P1.07 ▪ P0.24 ▪ P0.07/AIN3
J41		BL5340 pin header for access: ▪ P0.13 ▪ P0.17 ▪ P0.16 ▪ P0.15 ▪ P0.14 ▪ P0.18 ▪ P0.28/AIN7 ▪ P0.27/AIN6 ▪ P0.26/AIN5 ▪ P0.25/AIN4
J29		BL5340 pin header for access: ▪ P0.22 ▪ P0.20 ▪ P0.19 ▪ P1.03 ▪ P1.02 ▪ P0.21 ▪ P0.04/AIN0 ▪ P0.06/AIN2 ▪ P0.05/AIN1 ▪ GND
J13		BL5340 pin header for access: ▪ VDD_VSRC_nRF ▪ P1.00 ▪ P0.08 ▪ P0.09 ▪ P0.11_SWO_BLE ▪ P0.10

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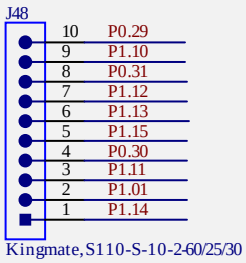
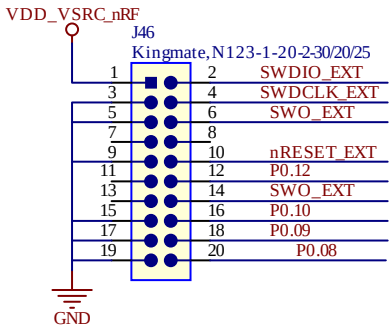
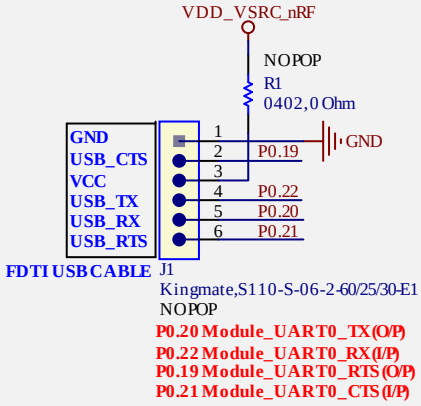
	Plated Through Holes or Header Connector	BL5340 Module Signals Exposed
J48		BL5340 pin header for access: ▪ P0.29 ▪ P1.10 ▪ P0.31 ▪ P1.12 ▪ P1.13 ▪ P1.15 ▪ P0.30 ▪ P1.11 ▪ P1.01 ▪ P1.14
J46		J46 is compatible to same connector on Nordic development board and brings out same signals. To bring the below signals from BL5340 module (via analog switch U24) to J46 (and P1), selection SW11 switch must be in position 2-1 (LOW) and jumper must be fitted in J50. ▪ SWDIO_EXT ▪ SWDCLK_EXT ▪ SWO_EXT ▪ nRESET_EXT
J1		Serial Port plated holes for access UART0 DVK-BL5340:
J35	BL5340 UART0 routed to FTDI: J35 No jumper in J35 (default) routed to open circuit: Fit jumper in J35	Jumper in J35 selects between DVK-BL5340 UART0 routed to FTDI chip or not (open circuit): **No Jumper on J35 (default)** • Routes P0.19 (RTS) to FTDI CTS • Routes P0.22 (TX) to FTDI RX • Routes P0.20 (CTS) to FTDI RTS • Routes P0.21 (RX) to FTDI TX **Jumper on J35 (Route to open circuit)** • Routes P0.19 (RTS) to open circuit

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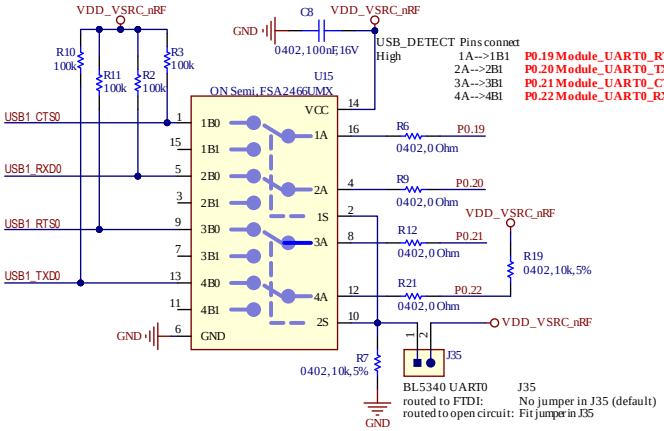
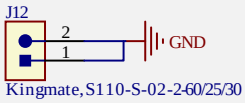
Plated Through Holes or Header Connector	BL5340 Module Signals Exposed
	• Routes P0.22 (TX) to open circuit • Routes P0.20 (CTS) to open circuit • Routes P0.21 (RX) to open circuit

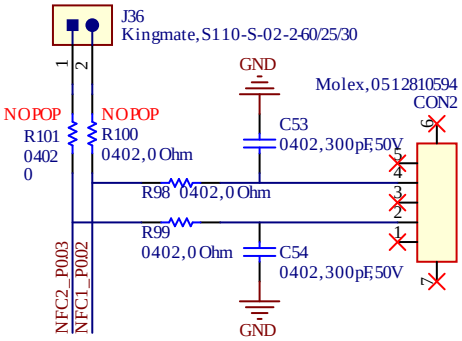
J12



BL5340 pin header for access:

- Connects to GND

J36



BL5340 pin header for access:

- P0.02 via R100 0R (default NOPOP)
- P0.03 via R101 0R (default NOPOP)

To use NFC1 pin as P0.02 fit R100 0R and NOPOP R98.

To use NFC2 pin as P0.03 fit R101 0R and NOPOP R99.

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7.2 Additional Peripherals/Sensors

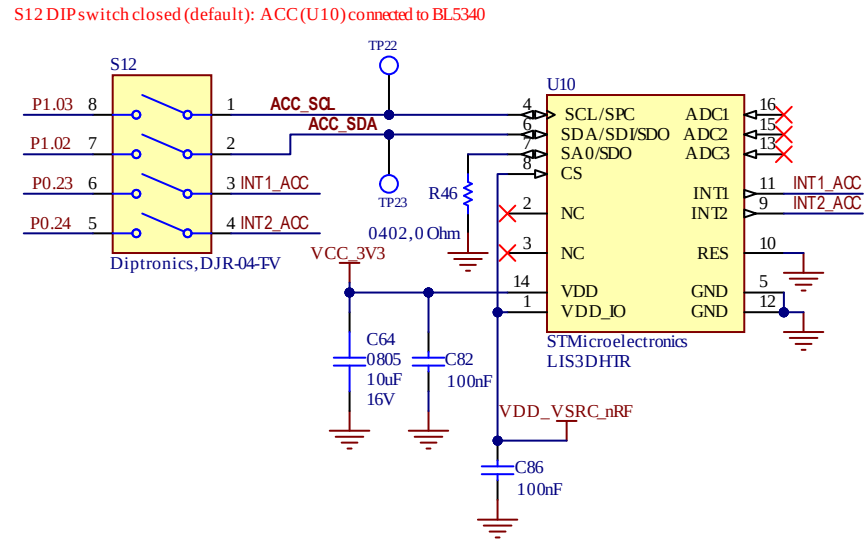
The BL5340 development board provides for simple and hassle-free connectivity to a wide range of sensors, but also includes several on-board sensors and options to enable a developer to test functionality straight out of the box.

7.2.1 I2C Sensors (3-axis accelerometer chip)

The I2C 3-axis accelerometer device (U10) is connected to the BL5340 I2C pins via DIP swich S12. Table 7**Error! Reference source not found.** lists signal mappings of how the I2C EEPROM (U2) is wired to BL5340 I2C pins.

Table 7: I2C 3-axis accelerometer chip U10 on DVK-BL5340 to BL5340 module I2C signal mappings

I2C 3-axis accelerometer (U10)	BL5340 (MOD1) pin	Comments
(U10pin4) TH_SCL	(MOD1 pin38) P1.03	DIP switch S12 position closed to route (default)
(U10pin3) TH_SDA	(MOD1 pin37) P1.02	DIP switch S12 position closed to route (default)



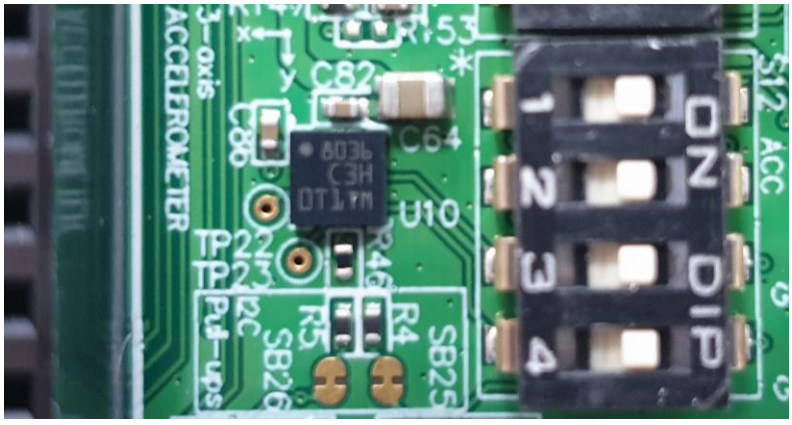


Figure 13: I2C 3-axis accelerometer (U10), DIP switch (S12) schematic and PCB (shows closed DIP switch S12)

Link to datasheet for 3-axis accelerometer IC (U10), https://www.st.com/resource/en/datasheet/lis3dh.pdf
Manufacturer: STMicoelectronics
Manufacturer part number: LIS3DHTR

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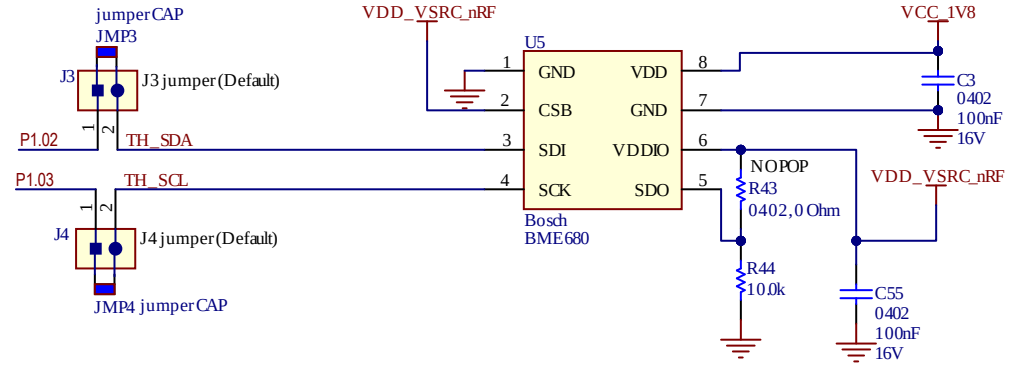
7.2.2 I2C Sensors (Temperature/Pressure/Humidity chip)

The I2C Temperature/pressure/humidity device (U5) is connected to the BL5340 I2C pins via pin headers. Table 8 lists signal mappings of how the I2C Temperature/pressure/humidity device (U5) is wired to BL5340 I2C pins.

Table 8: I2C Temperature /Pressure /Humidity chip U5 on DVK-BL5340 to BL5340 module I2C signal mappings

I2C Temperature/Pressure/Humidity (U5)	BL5340 (MOD1) pin	Comments
(U5pin4) TH_SCL	(MOD1 pin38) P1.03	Fitted jumper on J4 to route (default)
(U5pin3) TH_SDA	(MOD1 pin37) P1.02	Fitted jumper on J3 to route (default)



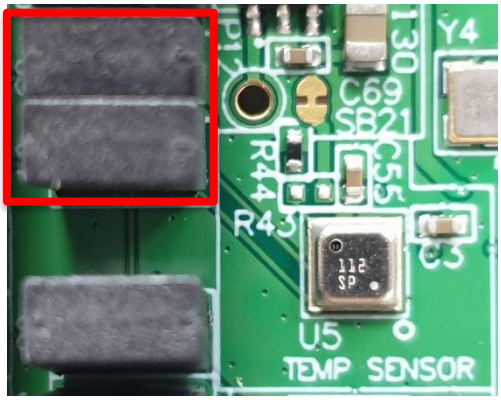


Figure 14: I2C Temperature/Pressure/Humidity chip (U5) and jumpers (shown in red) schematic and PCB

Link to datasheet for Temperature/Pressure/Humidity IC (U5), https://ae-bst.resource.bosch.com/media/_tech/media/datasheets/BST-BME680-DS001.pdf
Manufacturer: Bosch
Manufacturer part number: BME680

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7.2.3 I2C Sensors (Eeprom chip)

The I2C EEPROM device (U2) is connected to the BL5340 I2C pins via pin headers. Table 9 lists signal mappings of how the I2C EEPROM (U2) is wired to BL5340 I2C pins.

Table 9: I2C EEPROM chip U2 on DVK-BL5340 to BL5340 module I2C signal mappings

I2C EEPROM (U2)	BL5340 (MOD1) pin	Comments
(U2pin6) EE_SCL	(MOD1 pin38) P1.03	Fitted jumper on J11 to route (default)
(U2pin5) EE_SDA	(MOD1 pin37) P1.02	Fitted jumper on J6 to route (default)

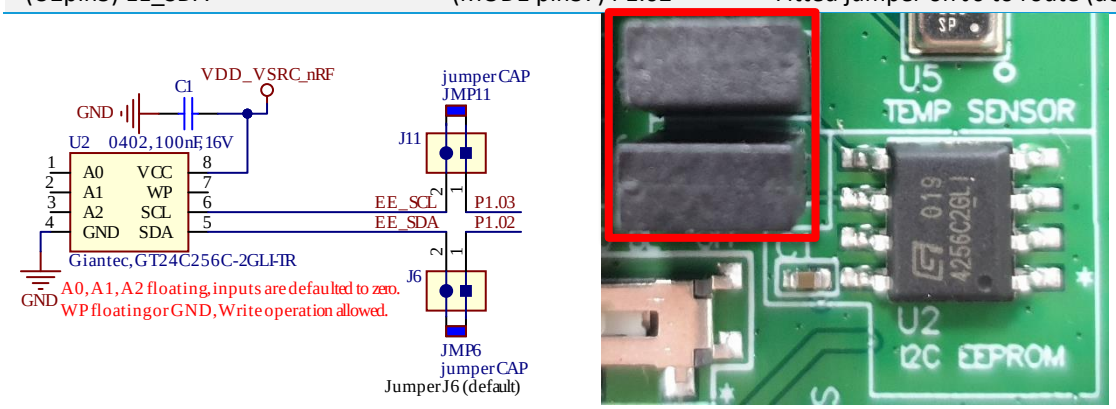


Figure 15: I2C EEPROM (U2), jumpers (shown in red) schematic and PCB

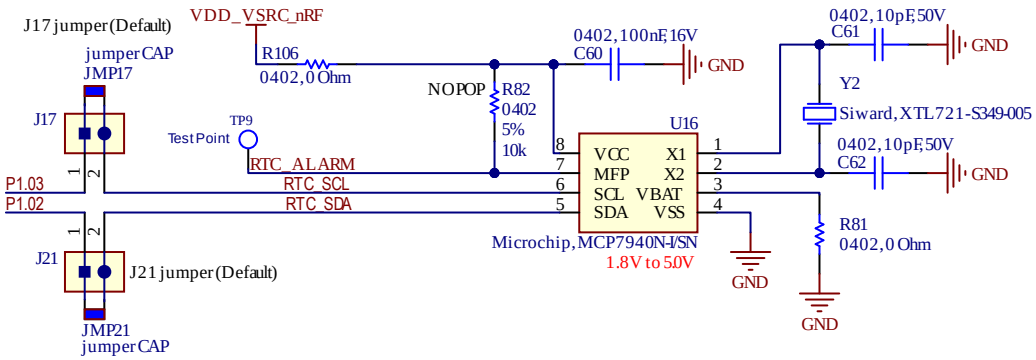
Link to datasheet for EEprom IC (U2), http://www.giantec-semi.com/Upload/datasheet/CU/GT24C256C_DS_Cu.pdf
Manufacturer: Giantec
Manufacturer part number: GT24C256C-2GLI-TR

7.2.4 I2C Sensors (RTC chip)

The I2C RTC chip (U16) is connected to the BL5340 I2C pins via pin headers. Table 10 lists signal mappings of how the I2C RTC (U16) is wired to BL5340 I2C pins.

Table 10: I2C RTC chip U16 on DVK-BL5340 to BL5340 module I2C signal mappings

I2C RTC chip (U16)	BL5340 module (MOD1) pin	Comments
(U16 pin6) RTC_SCL	(MOD1 pin38) P1.03	Fitted jumper on J17 to route (default)
(U16 pin5) RTC_SDA	(MOD1 pin37) P1.02	Fitted jumper on J21 to route (default)
(U16 pin7) RTC_ALARM	-	Brought out on TP9



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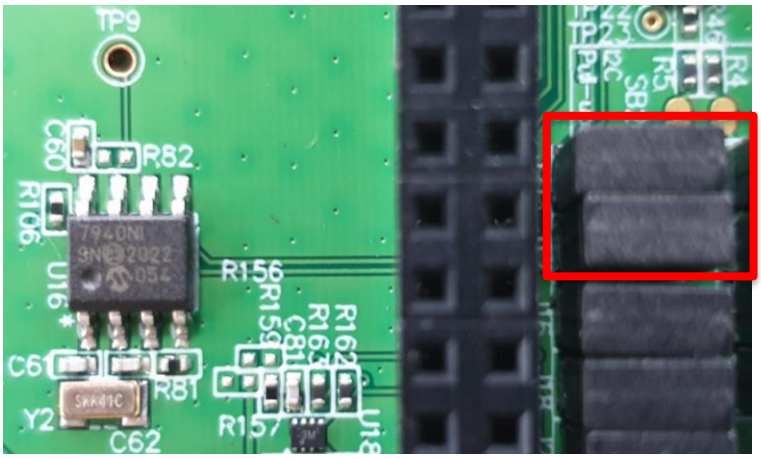

Figure 16: I2C device RTC chip (U16), jumpers (shown in red) schematic and PCB

Link to datasheet for RTC chip (U2), http://ww1.microchip.com/downloads/en/DeviceDoc/MCP7940N-Battery-Backed-I2C-RTCC-with-SRAM-20005010G.pdf

Manufacturer: Microchip
Manufacturer part number: MCP7940N-I/SN

7.2.5 I2C Sensors (DAC chip)

The I2C DAC device (U17) is connected to the BL5340 I2C pins via pin headers. Table 11 lists signal mappings of how the I2C DAC device (U17) is wired to BL5340 I2C pins.

Table 11: I2C DAC chip U17 on DVK-BL5340 to BL5340 module I2C signal mappings

I2C RTC chip (U16)	BL5340 module (MOD1) pin	Comments
(U17 pin5) DAC_SCL	(MOD1 pin38) P1.03	Fitted jumper on J5 to route (default)
(U17 pin5) DAC_SDA	(MOD1 pin37) P1.02	Fitted jumper on J10 to route (default)

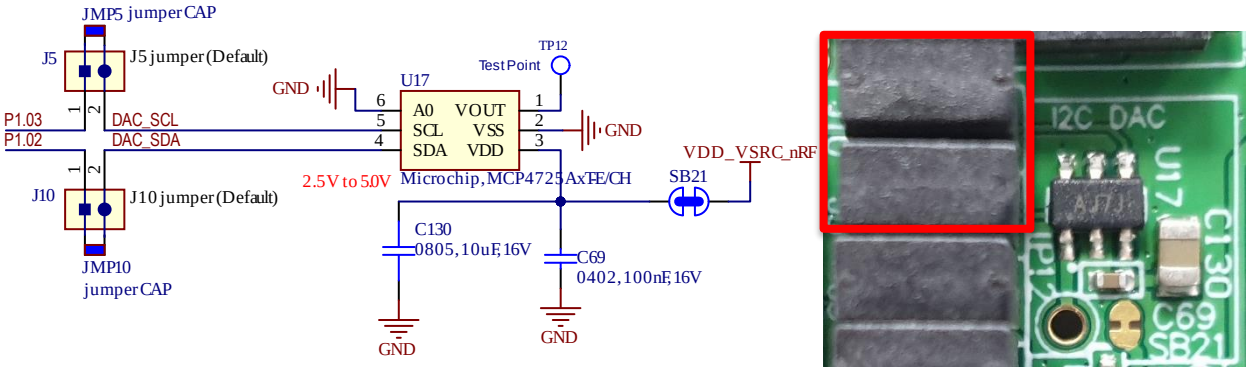

Figure 17: I2C device DAC chip (U17), jumpers (highlighted in red) schematic and PCB

Link to datasheet for DAC chip (U17), https://ww1.microchip.com/downloads/en/DeviceDoc/22039d.pdf
Manufacturer: Microchip
Manufacturer part number: MCP4725AxT-E/CH

The DAC chip does NOT operate down to 1.7V (VDD_VSRD_nRF), so only valid position for power supply switch SW5 is “3V3” position for Normal voltage mode operation (SW7 middle position).

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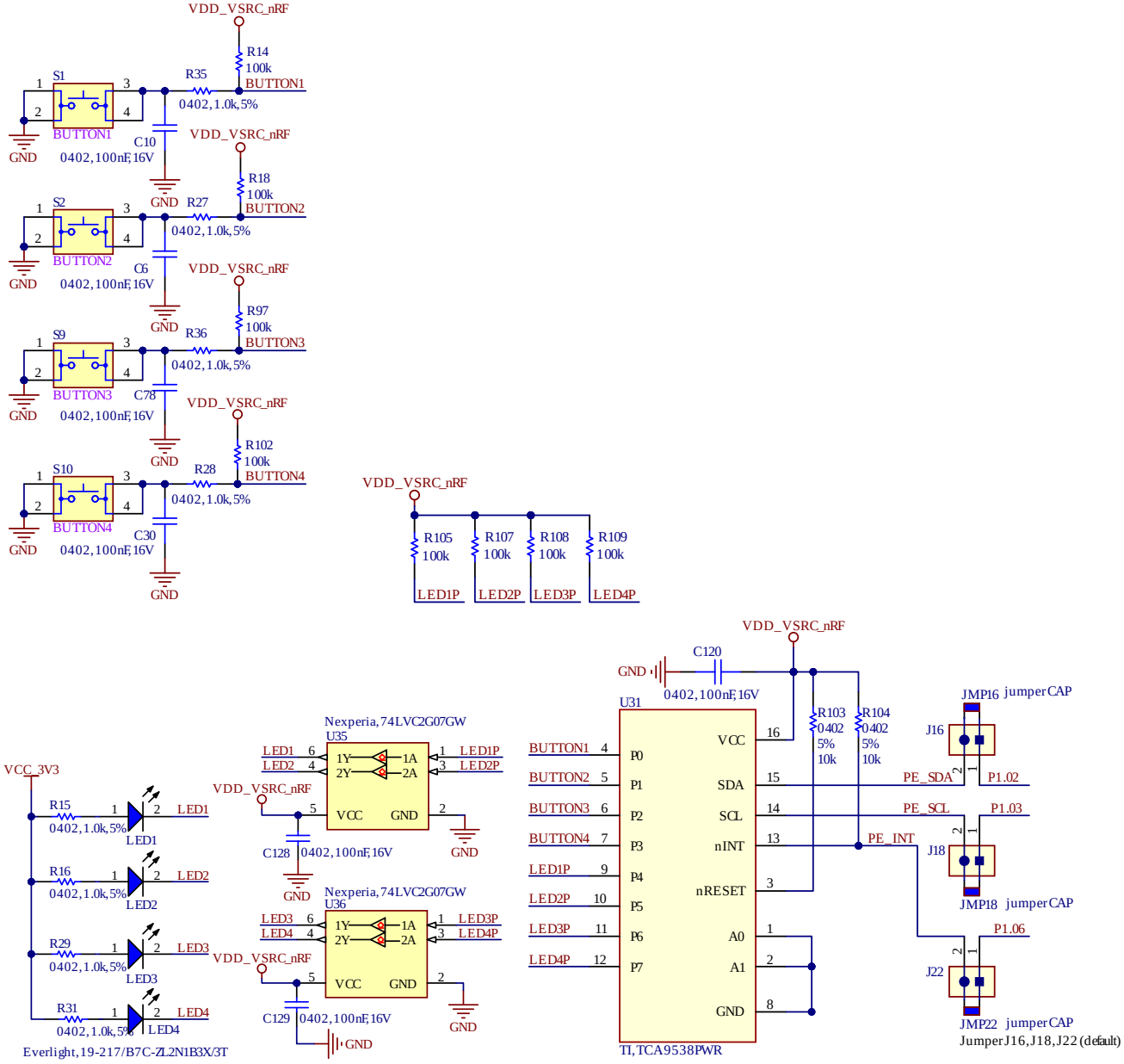
7.2.6 I2C Sensor (Port Expander chip connecting 4 LED's and 4 BUTTONs)

The I2C Port Expander device (U31) is connected to the BL5340 I2C pins via pin headers. Table 12 lists signal mappings of how the I2C DAC device (U17) is wired to BL5340 I2C pins.

Table 12: I2C Port Expander chip U31 on DVK-BL5340 to BL5340 module I2C signal mappings

I2C RTC chip (U16)	BL5340 module (MOD1) pin	Comments
(U31 pin14) PE_SCL	(MOD1 pin38) P1.03	Fitted jumper on J18 to route (default)
(U31 pin15) PE_SDA	(MOD1 pin37) P1.02	Fitted jumper on J16 to route (default)
(U31 pin13) PE_INT	(MOD1 pin37) P1.06	Fitted jumper on J22 to route (default)



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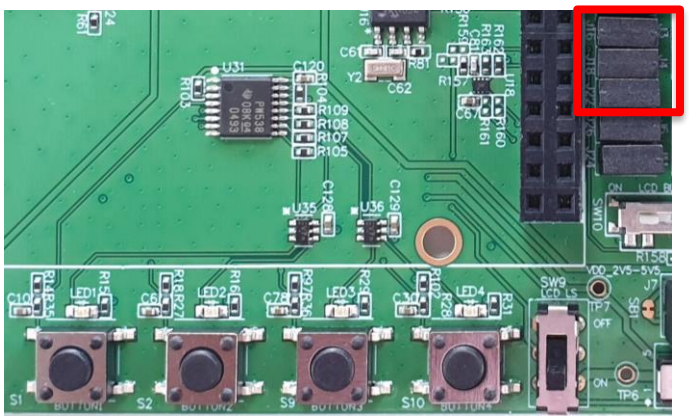

Figure 18: I2C device port expander chip (U31), LEDs, Buttons, jumpers (highlighted in red) schematic and PCB

Link to datasheet for I2C device GPIO Port expander chip (U31),
http://www.ti.com/general/docs/suppproductinfo.tsp?distId=10&gotoUrl=http%3A%2F%2Fwww.ti.com%2Flit%2Fgpn%2Ftca9538
Manufacturer: TI
Manufacturer part number: TCA9538PWR

The four LEDs are active low, meaning that writing a logical one (“0”) to the output pin (of U35 and U36) illuminates the LED.

Link to LED open drain buffer driver (U35, U36) https://assets.nexperia.com/documents/data-sheet/74LVC2G07.pdf
Manufacturer: Nexperia
Manufacturer part number: 74LVC2G07GW

7.2.7 I2C Sensors (LCD assembly and level shifter)

See section 7.2.10 High Speed SPI (SPIM4) Device (LCD assembly and level shifter) for full LCD assembly circuit which includes the I2C interface part of the LCD display assembly, level shifter and pins header schematic and PCB.

The I2C interface on LCD assembly (plugged into CON4) is connected to the BL5340 I2C via level shifter U18 and jumpers on header connectors J24, J26. Table 13 lists signal mappings of how the I2C of LCD assembly is wired to BL5340 I2C pins. Level shifter (U18) is needed as the LCD display assembly operates at 3.3V only, but the BL6340 can operate down to 1.7V. Level shifter (U18) is enabled (by default) by switch SW9.

Table 13: I2C LCD assembly level shifter chip (U18) on DVK-BL5340 to BL5340 module I2C signal mappings

I2C level shifter chip (U18)	BL5340 module (MOD1) pin	Comments
(U18 pin3) LCD_CTP_SCL1	(MOD1 pin38) P1.03	Fitted jumper on J24 to route (default)
(U18 pin4) LCD_CTP_SDA1	(MOD1 pin37) P1.02	Fitted jumper on J26 to route (default)

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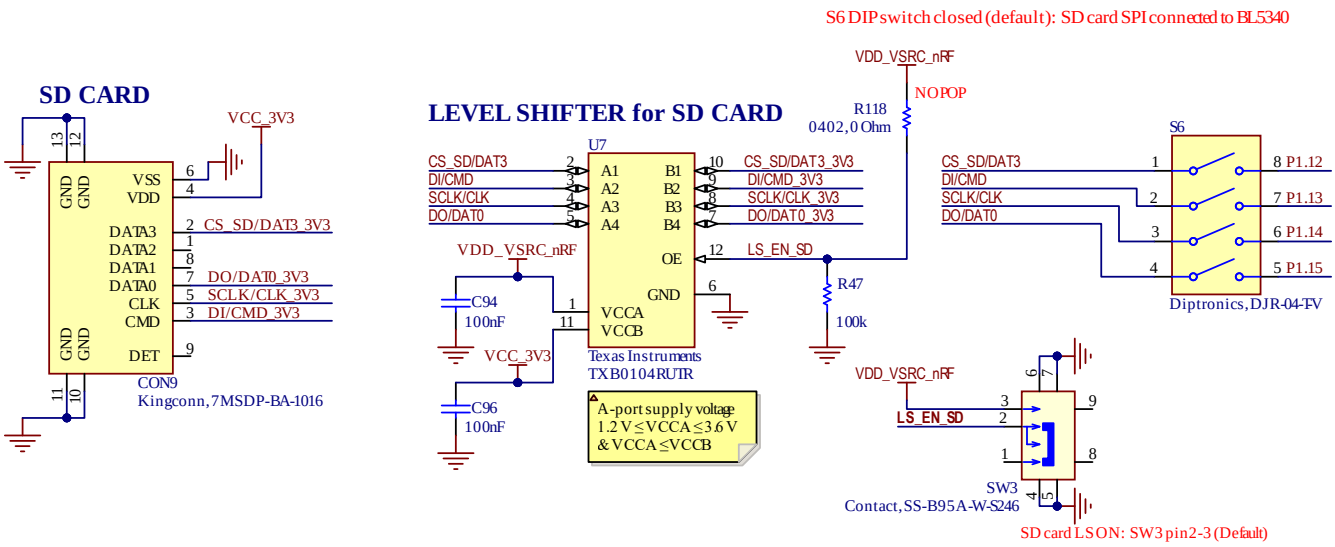
7.2.8 SPI Device (SD card)

The SD card SPI interface level shifter device (U7) is connected to the BL5340 SPI pins via DIP switch S6, see Table 14.

Table 14: SD card SPI interface level shifter chip (U7) on DVK-BL5340 to BL5340 module SPI signal mappings

SPI level shifter chip (U7)	BL5340 module (MOD1) pin	Comments
(U7 pin2) CS_SD/DAT3	(MOD1 pin49) P1.12	DIP switch S6 position closed to route (default)
(U7 pin3) DI/CMD	(MOD1 pin47) P1.13	DIP switch S6 position closed to route (default)
(U7 pin4) SCLK/CLK	(MOD1 pin48) P1.14	DIP switch S6 position closed to route (default)
(U7 pin5) DO/DAT0	(MOD1 pin45) P1.15	DIP switch S6 position closed to route (default)



Level shifter (U7) is needed as the SD card operates at 3.3V only, but the BL6340 can operate down to 1.7V. Level shifter (U7) is enabled (by default) by switch SW3.

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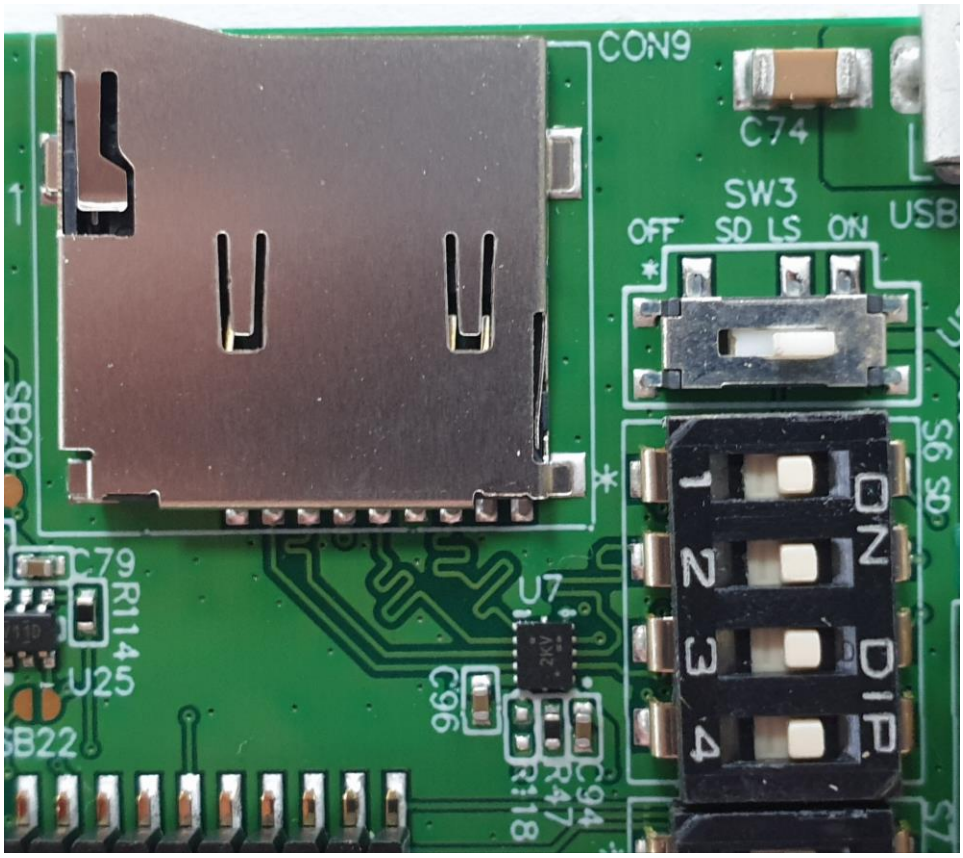

Figure 19: SPI device SD card holder (CON9), level shifter (U7), closed DIP switch schematic and PCB

Link to level shifter (U7) http://www.ti.com/lit/gpn/txb0104
Manufacturer: TI
Manufacturer part number: TXB0104RUTR

7.2.9 SPI Device (Ethernet chip)

The Ethernet chip SPI interface level shifter device (U7) is connected to the BL5340 SPI pins via DIP switch S5, see Table 15.

Table 15: Ethernet chip SPI interface level shifter chip (U9, Q6, U30) on DVK-BL5340 to BL5340 module SPI signal mappings

SPI level shifter chip (U9) SPI_CS_ETH discrete level shifter Q5 ETH_INT discrete level shifter U30 and	BL5340 module (MOD1) pin	Comments
(U9 pin5) SPI_SCK_ETH	(MOD1 pin53) P0.28/AIN7	DIP switch S5 position closed to route (default)
(U9 pin3) SPI_MOSI_ETH	(MOD1 pin4) P0.27/AIN6	DIP switch S5 position closed to route (default)
(U9 pin4) SPI_MISO_ETH	(MOD1 pin2) P0.26/AIN5	DIP switch S5 position closed to route (default)
(Q6 pin2) SPI_CS_ETH	(MOD1 pin6) P0.25/AIN4	DIP switch S5 position closed to route (default)
(U30 pin4) INT_ETH	(MOD1 pin65) P0.07/AIN3	DIP switch S5 position closed to route (default)

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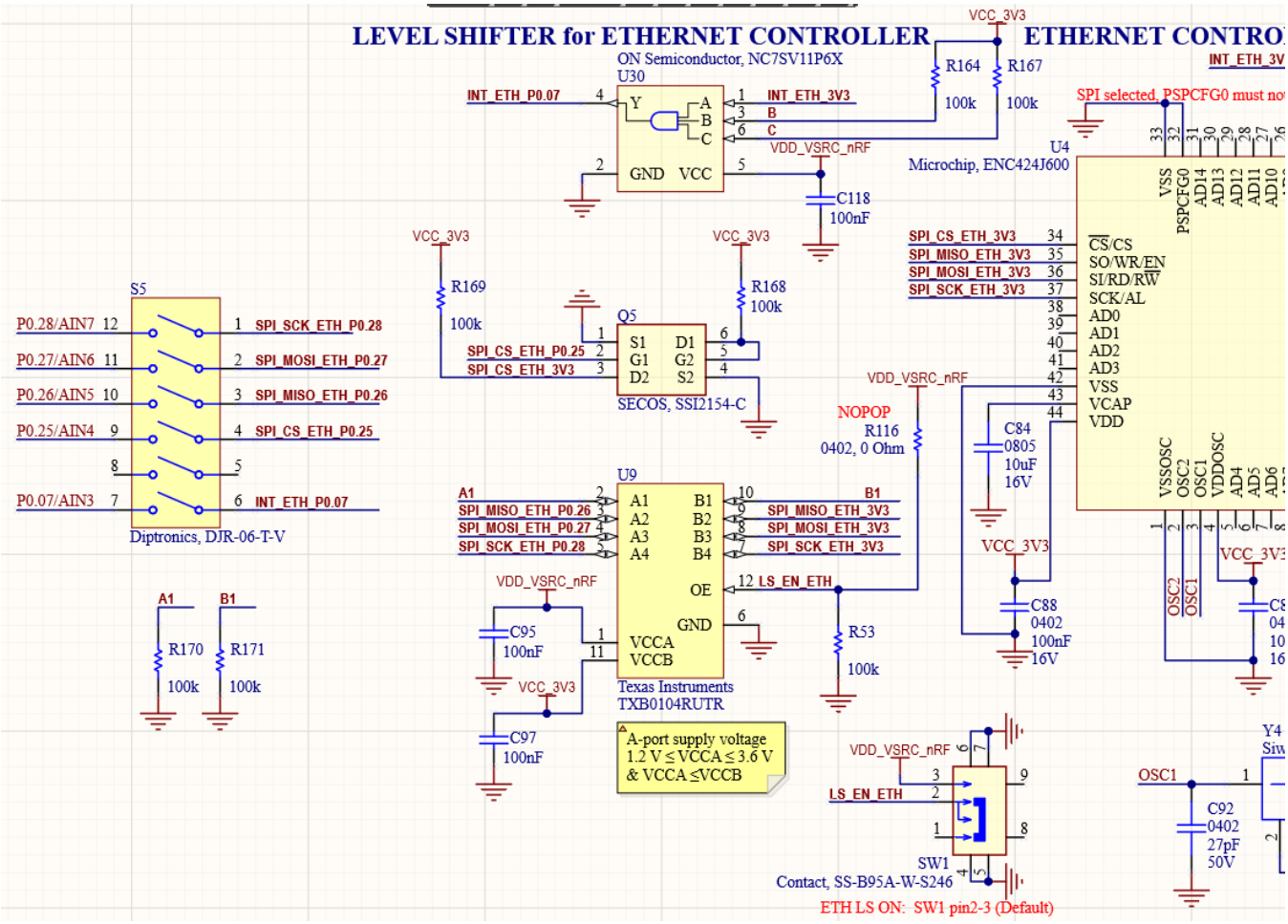
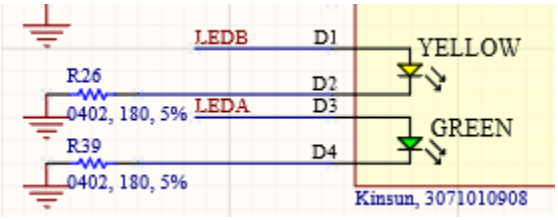


RJ45 ethernet connector (CON3) has integral LEDs as shown in Figure 20.



Level shifters (U9) is needed as the Ethernet chip (U4) operates at 3.3V only, but the BL6340 can operate down to 1.7V. Level shifter (U9) is enabled (by default) by switch SW1. Similarly, discrete level shifter circuits Q5, U30 for same purpose.

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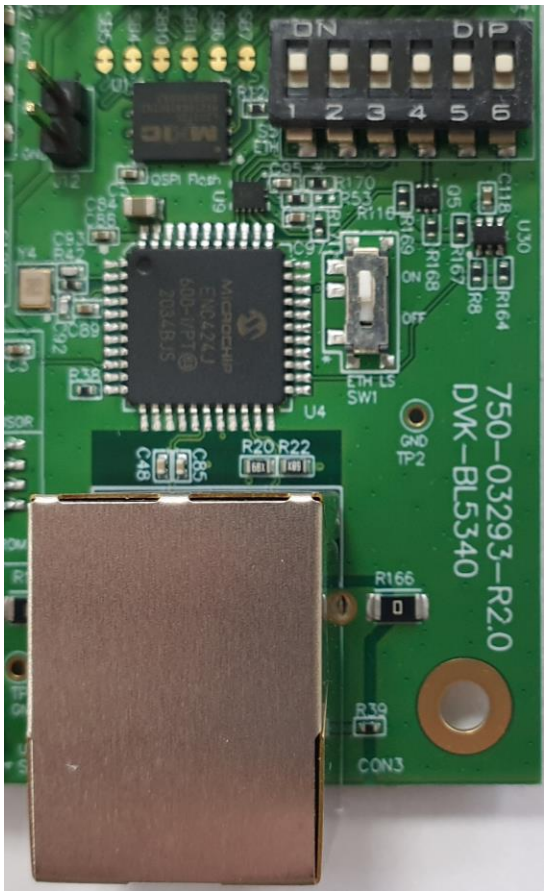

Figure 20: SPI device Ethernet chip (U4), level shifters (U30, Q5, U9), closed DIP switch (S5) schematic and PCB

Link to datasheet for SPI device Ethernet chip (U4), https://www.microchip.com/wwwproducts/en/en542414
Manufacturer: Microchip
Manufacturer part number: ENC424J600

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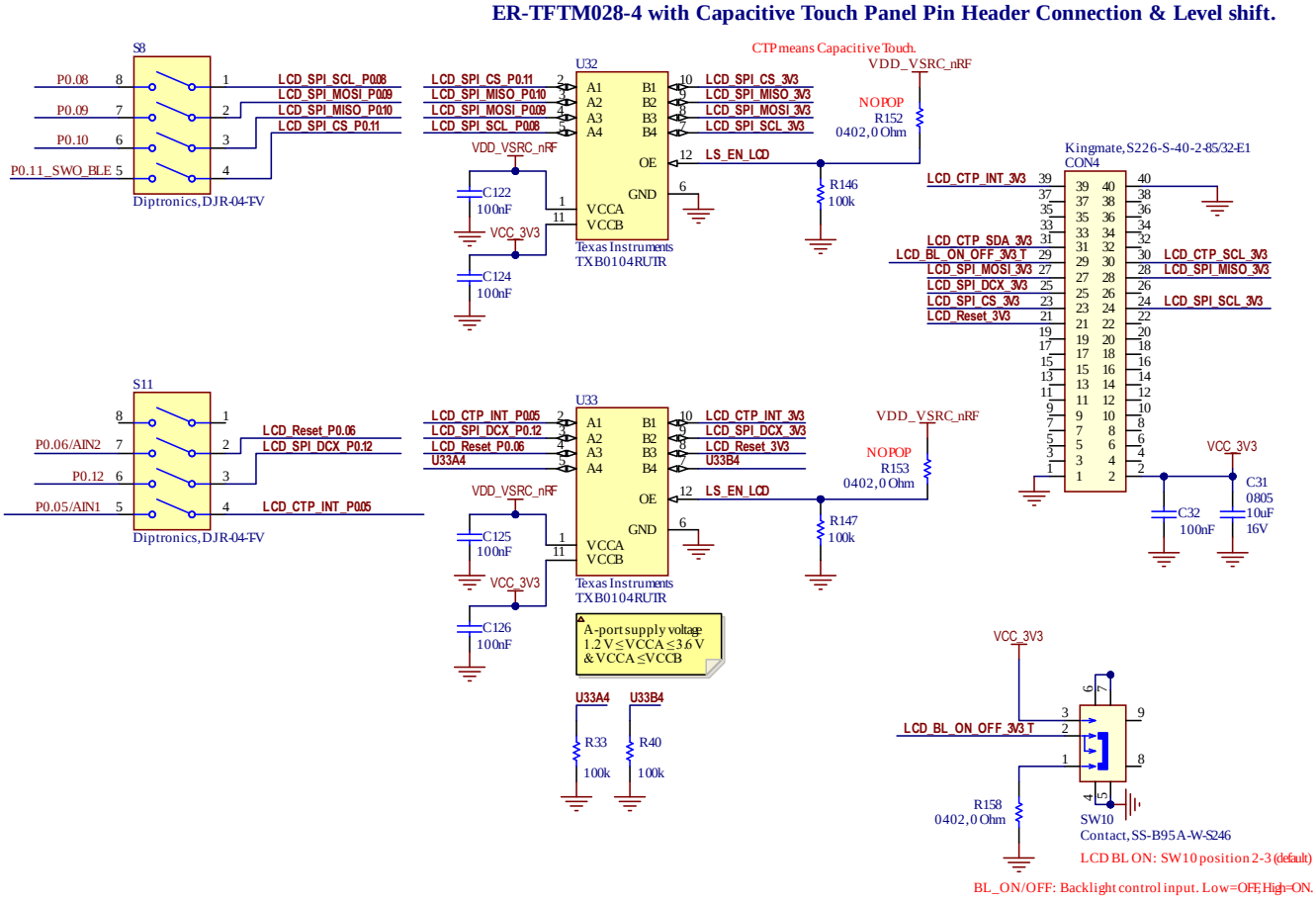
7.2.10 High Speed SPI (SPIM4) Device (LCD assembly and level shifter)

The SPI interface on LCD display assembly (plugged into CON4) is connected to the BL5340 SPI via DIP switches S8 and S11, see Table 16.

Table 16: LCD assembly High speed SPI interface (SPIM4) level shifter chip (U32, U33) on DVK-BL5340 to BL5340 module SPI signal mappings

SPI level shifter chip (U32, U33)	BL5340 module (MOD1) pin	Comments
(U32 pin5) LCD_SPI_SCL	(MOD1 pin27) P0.08/TRACEDATA3/SPIM4_SCK	DIP switch S8 position closed to route (default)
(U32 pin4) LCD_SPI_MOSI	(MOD1 pin25) P0.09/TRACEDATA2/SPIM4_MOSI	DIP switch S8 position closed to route (default)
(U32 pin3) LCD_SPI_MISO	(MOD1 pin22) P0.10/ TRACEDATA1/SPIM4_MISO	DIP switch S8 position closed to route (default)
(U32 pin3) LCD_SPI_CS	(MOD1 pin23) P0.11/TRACEDATA2/SPIM4_CSN	DIP switch S8 position closed to route (default)
(U33 pin4) LCD_Reset	(MOD1 pin64) P0.06/AIN2	DIP switch S11 position closed to route (default)
(U33 pin3) LCD_SPI_DCX	(MOD1 pin20) P0.12//TRACECLK/SPIM4_DCX	DIP switch S11 position closed to route (default)
(U33 pin2) LCD_CTP_INT	(MOD1 pin46) P0.05/AIN1	DIP switch S11 position closed to route (default)



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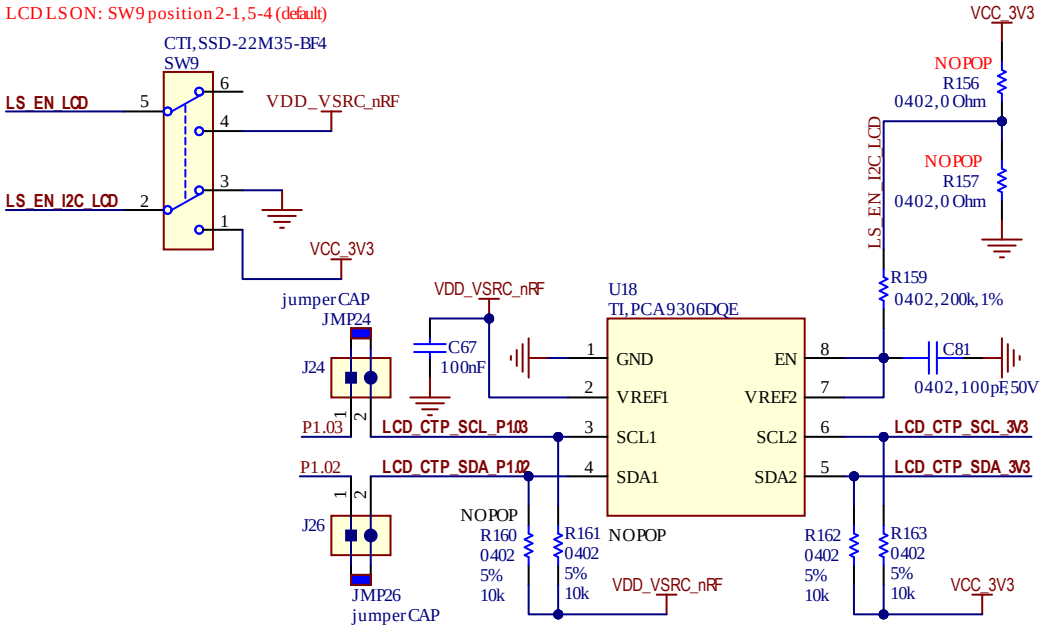

Level shifters (U32, U33) are needed as the LCD display assembly operates at 3.3V only, but the BL6340 can operate down to 1.7V. Level shifters (U32, U33) for LCD SPIM interface is enabled (by default) by switch SW9.

Level shifter (U18) is needed as the LCD display assembly operates at 3.3V only, but the BL6340 can operate down to 1.7V. Level shifters (U18) for LCD I2C interface is enabled (by default) by switch SW9.

Switch SW9 is for turning on or off the LCD assembly backlight, by default the SW9 is in ON position.

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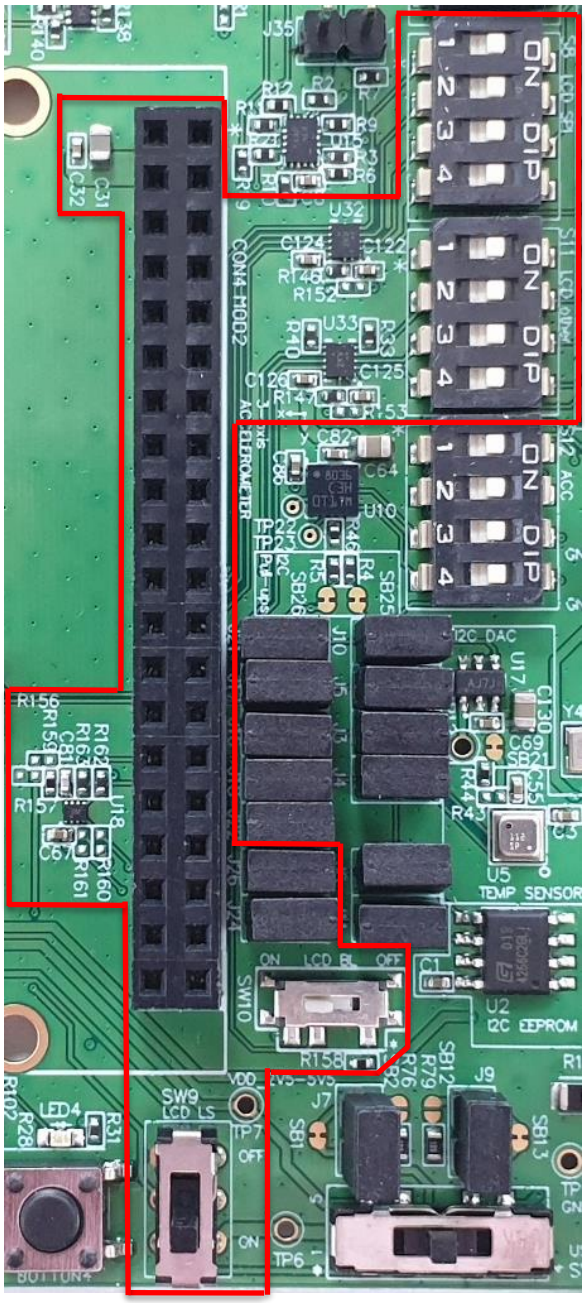

Figure 21: SPI and I2C device LCD assembly schematic and PCB

Link to datasheet for SPI and I2C device LCD display assembly (plugged into CON4), https://www.buydisplay.com/2-8-inch-tft-touch-shield-for-arduino-w-capacitive-touch-screen-module
Manufacturer: BuyDisplay
Manufacturer part number: to get MPN, choose below options
2.8"TFT Touch Shield for Arduino w/Capacitive Touch Screen Module
Interface: Pin Header Connection-4-wire SPI +USD0.33.
Power Supply (Typ.): VDD=3.3V
Touch Panel(attached by default): 2.8” Capacitive Touch Panel +USD5.36
Font Chip (refer to Font Chip Datasheet): ER3300-1 +USD1.30

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7.2.11 NFC External Antenna Connector and NFC Antenna RF Matching Circuit

The NFC antenna input connector (CON2) allows the Laird Connectivity-supplied flex-PCB NFC antenna to be plugged in. The BL5340 module NFC circuit uses two pins, pin 28 (**NFC1/P0.02**) and pin 26 (**NFC2/P0.03**) to connect the antenna. These pins are shared with GPIOs (**P0.02** and **P0.03).** Pin 28 (**NFC1/P0.02**) and pin 26 (**NFC2/P0.03**) are configured by default on the development board schematic to use NFC antenna, but if pin 28 (**NFC1/P0.02**) and pin 26 (**NFC2/P0.03**) are needed as normal GPIOs, R98 and R99 must be removed and R100 and R101 must be shorted by 0R.

C53 (300pF) and C54 (300pF) are RF tuning elements for the flexi-PCB NFC antenna (see datasheet).

Table 17: NFC input BL5340 signal mappings

BL5340 (MOD1) pin	Bring out P0.02 and P0.03 to NFC antenna connector (CON2)	Bring out P0.02 and P0.03 to Header connector (J36)
(MOD1 pin28) **P0.02/NFC1**	Fit R98 0R (default) Remove R100 0R (default)	Remove R98 0R Fit R100 0R
(MOD1 pin26) **P0.03/NFC2**	Fit R99 0R (default) Remove R101 0R (default)	Remove R99 0R Fit R101 with 0R

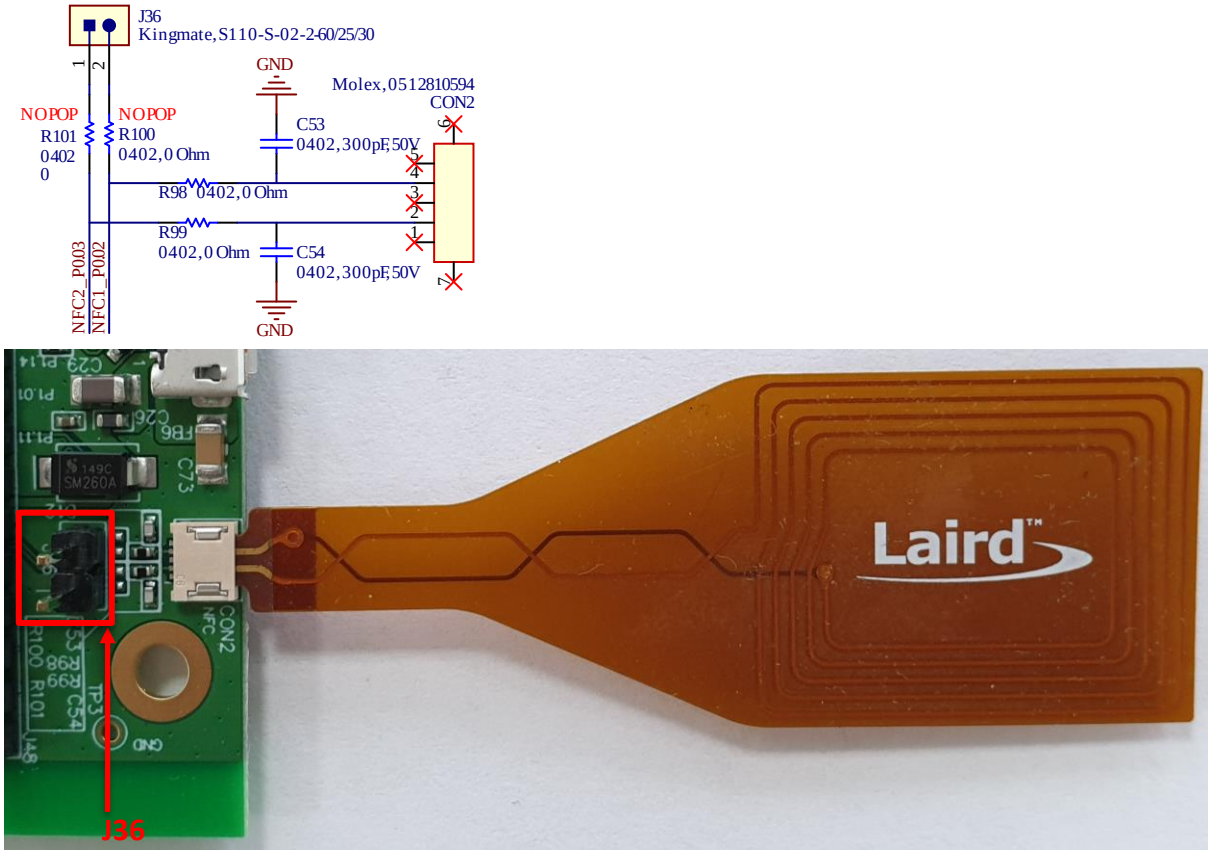

Figure 22: NFC antenna RF matching circuit, NFC antenna connector schematic and NFC plugged in to connector CON2

7.2.12 Optional External Serial QSPI Flash IC

There is an optional external serial QSPI flash IC (U1) that may be used, for example, for data logging purposes. U1 can also be capable of SPI mode.

Closed solder bridges SB4, SB5, SB6, SB7, SB10 and SB11 by default connects this optional external serial (QSPI) flash (U1 to the BL5340 module).

By default, these BL5340 pins are GPIO pins.

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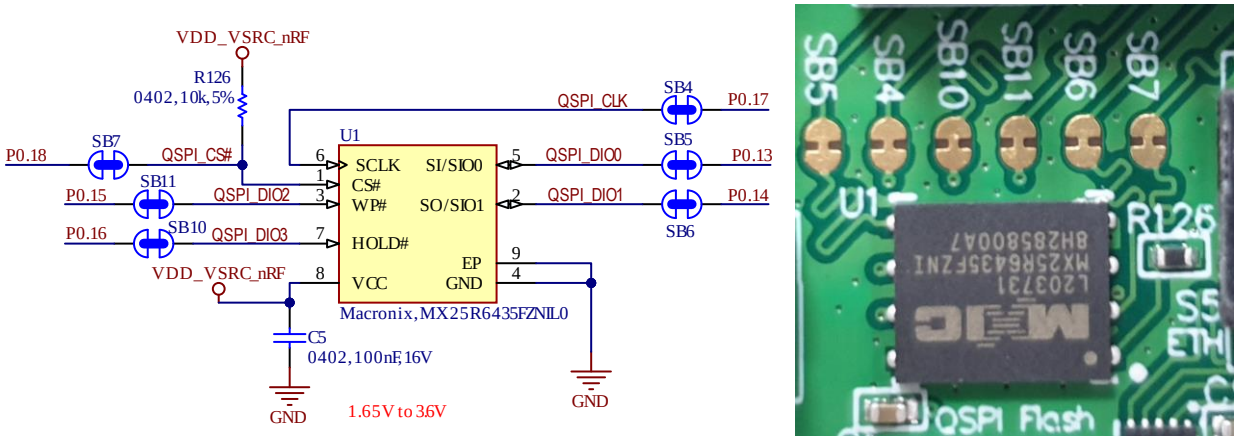

Figure 23: Optional external serial QSPI flash IC (U1) schematic and PCB

Table 18 shows the U1 pin mapping to BL5340 GPIO pin mapping (via closed solder bridges).

Table 18: U1 QSPI (or SPI) flash IC pin mapping to BL5340 GPIO mappings

BL5340 (MOD1) pin	U1 Pin (QSPI flash IC) and Pin Name	Via Closed Solder bridge
(MOD1 pin61) P0.18/QSPI_CSN	Pin 1 CS#	SB7 BL5340 Dev board R126 10K pull-up on, therefore by default, device not selected. Drive from BL5340 line low to select.
(MOD1 pin16) P0.17/QSPI_CLK	Pin 6 SCLK	SB4
(MOD1 pin24) P0.13/QSPI_IO0	Pin 5 SIO0/SI	SB5
(MOD1 pin62) P0.14/QSPI_IO1	Pin 2 SIO1/SO	SB6
(MOD1 pin18) P0.15/QSPI_IO2	Pin 3 SIO2/WP#	SB11
(MOD1 pin17) P0.16/QSPI_IO3	Pin 7 SIO3/HOLD#	SB10

Link to datasheet for QSPI device flash chip (U1),
http://www.macronix.com/Lists/Datasheet/Attachments/7428/MX25R6435F,%20Wide%20Range,%2064Mb,%20v1.4.pdf
Manufacturer: Macronix
Manufacturer part number: MX25R6435FZNIL0

7.2.13 Optional 32.768 kHz Crystal

The BL5340 on-chip 32.768kHz RC oscillator provides the standard accuracy of ±250 ppm, with calibration required every 8 seconds (default) to stay within ±250 ppm.

The BL5340 also allows, as an option, to connect an external higher accuracy (±20 ppm) 32.768 kHz crystal to the BL5340 pins P0.00/XL1 (pin 34) and P0.01/XL2 (pin 32). This provides improved protocol timing and helps with radio power consumption in the system on idle /system off sleep modes by reducing the time that the Rx window must be open.

By default, the optional external 32.768kHz crystal oscillator circuit is connected to the BL5340 module, remove R127 and R128 (to disconnect tracks going to J44).

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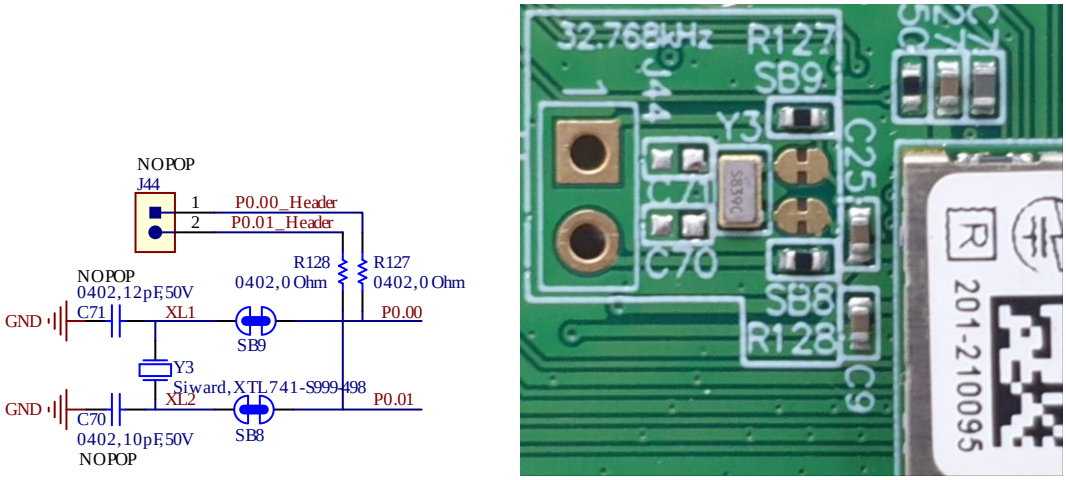

Figure 24: Optional external 32.768kHz crystal circuit schematic and PCB

The Y3 crystal is 7pF load capacitor part. The nRF5340 has internal load capacitor (configurable to 7pF, 9pF or 11pF), so to complete the oscillator the load capacitor inside the nRF5340 should be set to 7pF (in Firmware) to use Y3.

8 Other Features

8.1 Current Consumption Measurement

A removable jumper (on J7 and J9) is provided to break the power supply line directly to the module, allowing you to measure current consumption. For normal operation, the jumper on J7 (and J9) must be fitted (and is fitted by default).

IMPORTANT: To achieve the optimal power consumption of the BL5340 series module on the development board, see the Nordic System OFF sample application https://github.com/zephyrproject-rtos/zephyr/tree/master/samples/boards/nrf/system_off
DVK-BL5340 DIP switch S12 must be opened, otherwise the current consumption would be much higher.

Note: This measures the current consumption of the **BL5340** series module ONLY.

The current drawn by the BL5340 series module can be monitored on the development board. Figure 25 shows the schematic and location of measuring points on the PCB related to current measurements.

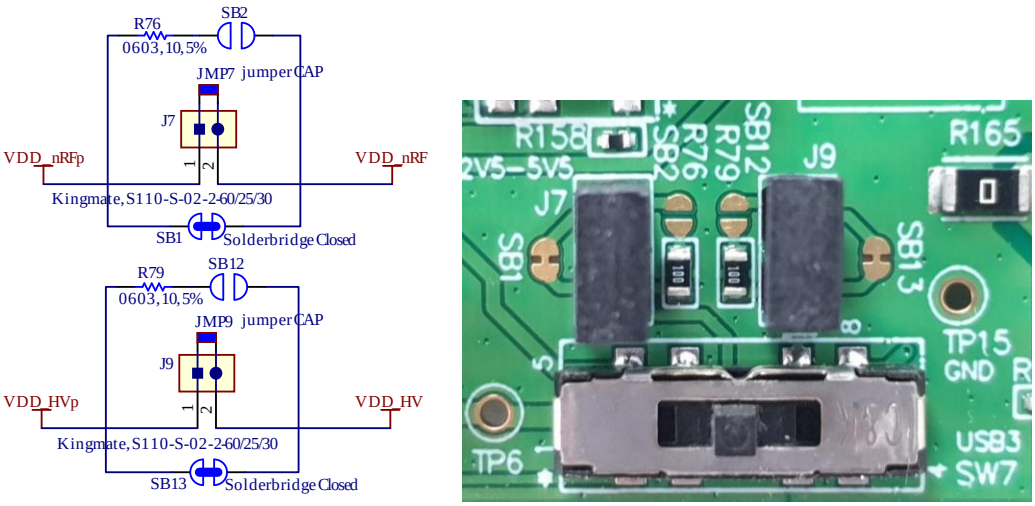

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Figure 25: Current measurement schematic and PCB

There are three primary ways to measure the current consumption:

- **Using Ammeter –** Cut solder bridge SB1 and connect an ampere meter between the two pins of J7 pins 1-2. This monitors the current directly. This is when BL5340 is powered using the normal voltage Mode (BL5340 operated VDD pin). If the BL5340 is powered using the high voltage Mode (BL5340 operated VDD_HV pin), then only cut solder bridge SB13 and connect an ampere meter between the two pins of J9 (pins 1-2).
- **Using Oscilloscope –** The open solder bridge SB2 first needs to be shorted with solder, then the on-board 10 Ohm resistor R76 which is mounted across J7 pins 1-2 can be used as current sense resistor. Connect an oscilloscope or similar with two probes on the pins on the J7 connector and measure the differential voltage drop. The voltage drop is proportional with current consumption. If the 10 Ohm resistor is chosen, 10 mV equals 1mA.

  This method allows the dynamic current consumption waveforms to be shown on an oscilloscope as the BL5340 radio operates. This can provide insight into power optimization.
- **Power Profiler Kit (PPK) from Nordic –** For more details, refer to http://www.nordicsemi.com/eng/Products/Power-Profiler-Kit/(language)/eng-GB

9 Additional Assistance

Laird Connectivity offers a variety of documentation and ancillary information to support our customers through the initial evaluation process and ultimately into mass production. Additional documentation can be accessed from the Documentation tab of the BL5340 Product Page.

Please contact your local sales representative or our support team for further assistance:

Laird Connectivity
Support Centre: https://www.lairdconnect.com/resources/support
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Web: https://www.lairdconnect.com/products

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