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THE TEST OF THE AD CONVERTERS EMBEDDED ON TWO MICROCONTROLLERS

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Testing method of ADC's implemented on microcontroller chips are descibed in the paper. The achieved results for microcontroller AT90S8535 and ADuC812 are discussed too. As a criterion of ADC precision, which allows to determine the operational condition limits, the number of effective bits has been chosen. More over, the DNL and INL measured characteristics are presented. The results are compared to some of the data brought out in vendors' data sheets.

Keywords: ADC performance testing, ADC errors and precision, microcontrollers,.

1 INTRODUCTION

Presently, the microcontrollers with analogue to digital converters (ADC) implemented on single chips and necessary analogue signal conditioning pre-processing blocks are very useful tools to design intelligent sensors. The aim of such structures is to recover the sensor's output signal as close as possible to the acquisition point in order to reduce the parasitic quantity impact. Acquired data are digitised, linearised, encoded and in the suitable format transmitted to the supervising computers which control the measuring process. Some of such microcontrollers possess general purpose voltage inputs. These inputs are sophisticated for the applications, where an additional analogue pre-processing circuit converts any output value from sensor into the ADC convenient voltage range.

2 ADC TESTING METHODS

The ADC implemented in tested microcontrollers contains a sample and hold circuit and these make possible to use dynamic testing methods in accordance with the IEEE Std. 1241 and 1057 [1,2]. The dynamic testing methods have been chosen for testing number of effective bits (ENOB) as well as for testing differential and integral non-linearity (DNL, INL). All methods enable to utilise the harmonic generator with low harmonic distortion and medium frequency stability. The total harmonic distortion (THD) of test signal can be improved by a low pass or band pass filter. For testing the ENOB the sine wave fitting test method has been chosen for various input frequencies. The medium time frequency stability of the test generator enables to approximate parameters of the harmonic signal from acquired sample data by the four parameter method [1,2]. Finally, the ENOB can be calculated from acquired and processed data. The histogram method with a sine wave input signal was used for measuring the DNL and INL. The obtained histogram was linearised by comparing to the ideal sine wave histogram and then the DNL and INL was calculated [1,2]. The Pentium based PC with National Instrument card Lab-PC-1200 was applied to control the test process. A function/arbitrary waveform generator HP33120A (Hewlett Packard) was used for generating of harmonic input signals. Moreover, a simple optional RC low pass filter was applied to improve THD at the ADC input. The filter cut-off frequency was chosen and changed in relation to the harmonic test signal frequency. Sampling frequency was given by the microcontroller program and derived from the microcontroller crystal oscillator by an internal timer, if it was needed. A microcontroller software was written, debugged and compiled in the supervising PC by the developing software tools and then the microcontroller

was programmed. The test controlling, data processing and presentation software for PC was fully developed in LabWindows/CVI programming environment (National Instruments).

3 ADuC 812 MICROCONVERTER

The ADuC812 by Analog Devices [4] is a fully integrated 12-bit data acquisition system incorporating a high performance self calibrating 8-channel ADC, dual 12-bit DACs and programmable 8 bit MCU (8052 instruction set compatible) on a single chip. The ADC conversion block provides the 8-channel mux, track/hold, on-chip reference, calibration features and A/D converter. The A/D converter consists of a conventional successive-approximation converter based on a switched capacitor DAC. A high precision, low drift and factory calibrated 2.5V reference is given on-chip. The internal reference may be overdriven via the external VREF pin. The ADC has been designed to run at a maximum speed of 1 sample every 5μs. (i.e. 200kHz sampling rate). Single step or continuous conversion modes can be initiated in software or alternatively by applying a convert signal to the an external pin. Internal timer can also be configured to generate a repetitive trigger for ADC conversions. The ADC may be configured to operate in a DMA Mode whereby the ADC block continuously converts and captures samples to an external RAM space without any interaction from the MCU core. The ADuC812 is shipped with factory programmed calibration coefficients which are automatically downloaded to the ADC on power-up ensuring optimum ADC performance. The ADC core contains automatic end point self-calibration and system calibration options that will allow the user overwrite the factory programmed coefficients if desired and tailor the ADC transfer function to the system in which it is being used. The basic specification of ADC are referred in tab. 3.

TESTING PROCESS AND EXPERIMENTAL RESULTS

The test was executed on the microcontroller implemented on the evaluation board EVAL-ADuC812QS by Analog Devices [5] with crystal frequency equal to 11.0592MHz. Input operate amplifier was disconnected and the testing signal from waveform generator was connected directly to ADC input pin of microcontroller via RC filter. The original power supply source (the board accessory) was utilized for measuring and the internal reference V_{REF}=2.5V was used as the ADC voltage reference. The ADC was tested in all conversion modes but this paper presents only the mode with the best results - continuos DMA conversion mode by using data memory on board and MCU core in IDLE operating mode. The tab.1 and the fig.3 showed the best measured results from all setting of the acquisition time for all possible setting ADC_{CLK} . The fig.1 and the fig.2 showed result of DNL and INL testing, where f_{IN}=3.3Hz, ADC_{CLK}=M_{CLK}/8 and ADC used timer2 for repetitive trigger, then f_{SAMP}=27,1kHz.

Table 1. Results of ENOB test of AduC812 for various ADC_{CLK}.

ADC_{CLK}	M_{CLK} / 8	M_{CLK} / 4	M_{CLK} / 2	M_{CLK} / 1
acq. time	2/ADC_{CLK}		4/ADC_{CLK}	
f_{SAMP} [Hz]	76800	153600	276481	526631
f_{IN}[Hz]	ENOB [bit]			
11	11.24			
33	11.27	11.25		
110	11.25	11.29	8.11	
330	11.28	11.29	8.10	5.35
1100	11.24	11.29	8.09	5.33
3300	11.22	11.27	8.10	5.35
11000	10.81	10.86	8.08	5.32
33000	9.89	9.89	8.03	5.34
66000	9.39	9.37	7.95	5.32
75000		9.30	7.94	5.36
110000			7.91	5.31
135000			7.89	5.16
260000				5.31

The sampling frequency in the last two columns are higher than specified maximal sampling frequency 200kHz.

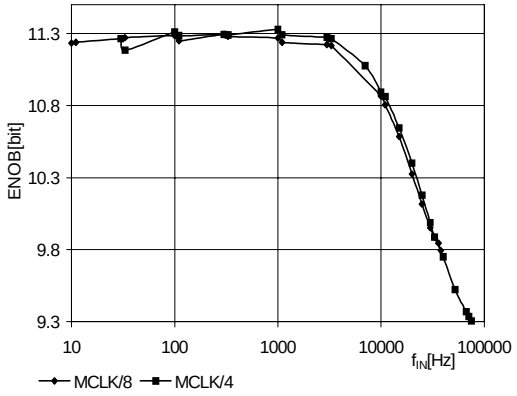

Figure 3. ENOB of ADuC812 for var. ADC_{CLK}.

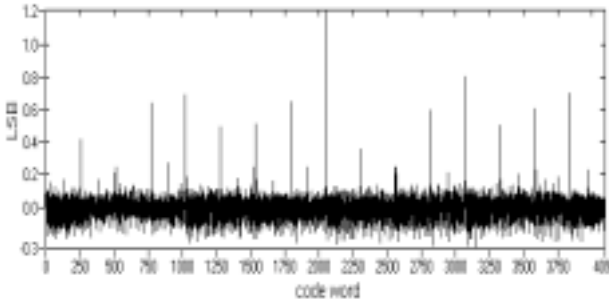

Figure 1. Differential non-linearity of ADuC812.

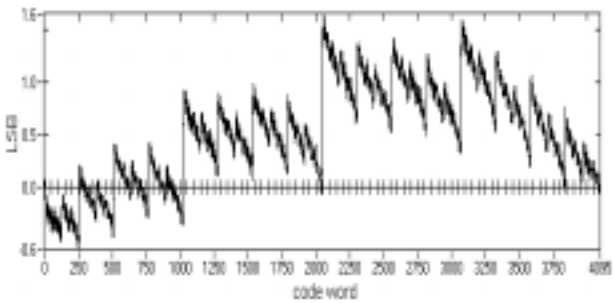

Figure 2. Integral non-linearity of ADuC812.

Without IDLE mode the ENOB is lower by about 0.3 LSB in the all conversion mode. Also an activity of internal timers causes decreasing of ENOB. For example, when the ADC was triggered by timer 2 (without DMA , without IDLE) and other internal timers were also active, maximal ENOB was 10.8 bits. The testing ADC with battery supply source had better results by about 0.2bits. Shapes of measured characteristics are identical for all conversion modes, however the absolute values depend on the disturbing factors mentioned higher.

4 AT90S8535 MICROCONTROLLER

The AT90S8535 by ATMEL [3] is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. The AT90S8535 features a 10-bit successive approximation ADC, 8-channel multiplexer and a Sample/Hold Amplifier. An external reference voltage must be applied to the A_{REF} pin. The ADC can operate in single or free run conversion mode. In the first mode, each conversion will have to be initiated by the user. In second mode, the ADC is constantly sampling and updating the ADC data register. The ADC contains a prescaler, which divides the system clock to an acceptable ADC clock frequency. The ADC accepts input clock frequencies in the range 50 - 200 kHz. Using Free Run Mode and an ADC clock frequency of 200 kHz gives the highest sampling frequency 15.4kSps. To improve noise reduction, the vendor recommends the Sleep mode of the microcontroller, when the core activities are stopped during the AD conversion. The basic specification are referred in tab. 3.

TESTING PROCESS AND EXPERIMENTAL RESULTS

The test was executed on microcontroller with crystal frequency equal to 8MHz. The testing harmonic signal from waveform generator was connected directly to ADC input pin of microcontroller via RC filter. As the external voltage reference V_{REF}=2.5V was used integrate circuit AD680 (Analog Devices). The ADC was tested in both conversion mode. The results of ENOB for ADC in free run mode (without timer) for all possible setting ADC_{CLK} are presented in the tab.2 and the fig.4. The fig.5 and the fig.6 showed result of DNL and INL testing, where f_{IN}=3.3Hz, $ADC_{CLK}=M_{CLK}/32$ and free run mode.

Table 2. Results of ENOB test of AT90S8535 in free run mode for various ADC_{CLK}.

ADC_{CLK}	$M_{CLK}/128$	$M_{CLK}/64$	$M_{CLK}/32$	$M_{CLK}/16$	$M_{CLK}/8$
f_{SAMP} [Hz]	4808	9616	19233	38337	76935
f_{IN}[Hz]	ENOB [bit]				
≤ 3.3	9,40	9,44	9,41	9,33	9,39
11	9,37	9,40	9,36	8,88	9,41
33	9,17	9,20	9,13	7,75	9,21
100	9,13	9,13	9,11	5,85	9,16
300	9,14	9,14	9,12		9,17
1000	9,04	9,09	9,08		9,15
3000	9,14	9,10	9,02		9,05
10000		9,06	8,98		9,13
30000		8,97	8,85		8,79
60000		8,38	8,39		8,30
90000		7,78	7,94		7,91
130000			7,47		7,41
250000					6,59

The ADC_{CLK} in the last three columns are higher than specified maximal 200kHz.

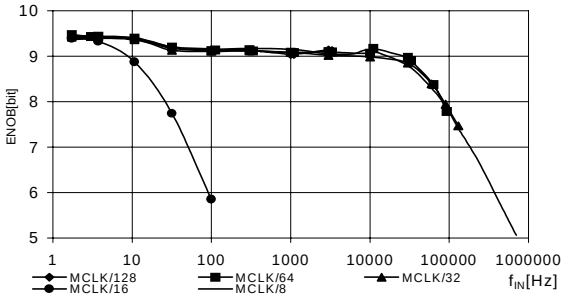

Figure 4. ENOB of AT90S8535 in free run mode for various ADC_{CLK}.

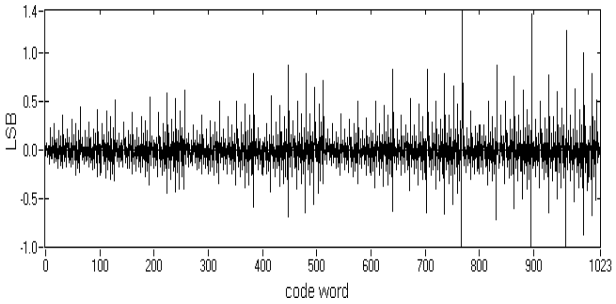

Figure 5. Differential non-linearity of AT90S8535.

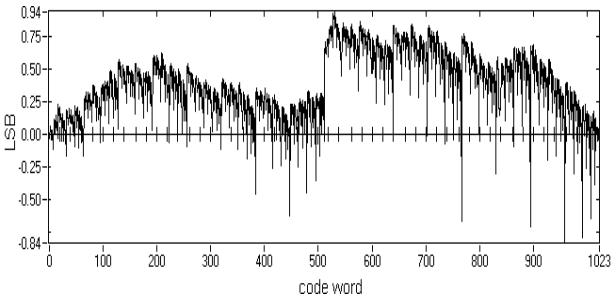

Figure 6. Integral non-linearity of AT90S8535.

ADC testing with supply from various power sources (power range $AV_{CC}=V_{CC}$ from 2,8V to 5,5V) hasn't indicated any influence of power source on ENOB. Even an application of battery supply source hasn't brought any advance.

5 CONCLUSION

The mutual comparing of ADC parameters is not easy, because the resolution of ADCs implemented on tested microcontrolers is different. Some of these parameters are presented in tab.3. However these ADCs can be compared from other point of view. Experiments with microconverter AduC812 confirmed high time punctuality of its triggering circuit. Also the microcontroller AT90S8535 has similar precise time triggering but only in free run mode. In repeated triggered single conversion mode controlled by any timer a triggering jitter was indicated. It depends on run-time optimisation of ADC start conversion subroutine. The experimental results from testing ADC implemented on AduC812 are most coherent to the expected error model of SAR ADC described in [4,5] than those from similar AD converter embedded on microcontroler AT90S8535.

Table 3. Comparison table of ADC specifications.
$AV_{DD}=DV_{DD}=AV_{CC}=V_{CC}$ =5V, V_{REF}=2.5V

	AduC812		AT90S8535	
	by vendor	measured	by vendor	measured
Resolution	12 Bits		10 Bits	
ENOB		11.3 Bits		9.45 Bits
INL (typ.)	±0.5 LSB		±0.2 LSB	
(max.)	±1.5 LSB	1.6 LSB	±0.5 LSB	1.4 LSB
DNL (typ.)	±1 LSB		±0.2 LSB	
(max.)		1.2 LSB	±0.5 LSB	0.95 LSB
SNR	70 dB	69.7 dB		58.7 dB

In order to avoid complicated testing stand authors developed new testing method described in the [6]. The stimulus signal of exponential shape is a new idea. The achieved results from both methods were compared - fig.7 versus fig.1.

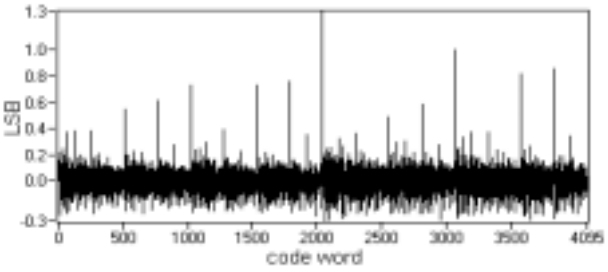

Figure 7. Differential nonlinearity of ADuC812 by exponential testing.

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