Synchronizing the ML4824 to Wide Frequency Ranges

INTRODUCTION

The material presented in this Application Note enables the user to simply and inexpensively synchronize a fixed frequency PWM controller to a wide range (>2x) of frequencies. The reader learns why synchronization is needed, and is shown a popular method of single frequency synchronization, along with its limitations. Next, the topic of wide frequency range synchronizing is covered and a block diagram presented using a novel approach based on a phase locked loop (PLL). A practical design example is given, complete with design formulas and a schematic for synchronizing the ML4824-1 to any frequency in the 25kHz to 75kHz range. The circuit presented can be used with any controller using a RC generated voltage ramp for the oscillator.

WHY SYNCHRONIZE?

Numerous electronic circuits found in the Computer and Telecommunications industry are sensitive to external noise generated by their switch-mode power source. Among the more common methods used to reduce the switcher's output noise are passive filters and linear regulators. Both are inserted between the output of the supply and the input of the circuit. The passive filter usually consists of one or more LC filter stages. These components, particularly the inductor, are costly and take up large amounts of board space. The linear regulator is commonly a low dropout (LDO) type, is costly, and is more likely to fail than the passive LC components.

Often, the switching noise disturbs the sensitive circuitry because it is asynchronous to the system clock's frequency. As an example, certain measurements (or conversions) involving D/A & A/D converters are performed once during each system clock period. If the system clock and the controller frequencies are not equal and 'phase-locked', the amount of switching noise contributed during succeeding conversions is unequal. When converting from digital to audio the result may be a noticeable hum or buzz superimposed on the reconstructed audio signal. If, however, the controller frequency is phase locked to the system clock the noise occurs at the 'edges' of each measurement time, and is thus excluded from the conversion. Or the noise occurs at the same time during each period and averages out, having no adverse affect on the signal. The results are often superior to the filtering methods mentioned earlier and far less expensive.

TRADITIONAL SYNC METHOD & LIMITATIONS

Nearly all switch-mode controllers contain circuitry that creates an oscillator from a linear voltage ramp. To set the oscillator frequency the user selects an external resistor and capacitor from a graph or formula provided by the manufacturer. Figure 1 shows the internal oscillator of a typical controller and the external frequency setting components. Figure 2 displays the resulting voltage ramp appearing across the timing capacitor CT. The voltage ramp creates the oscillator and is an input to the internal voltage comparator. This ramp voltage is compared to the error amplifier output voltage to vary the duty cycle as required. For this reason the voltage ramp must be linear throughout its rising edge.
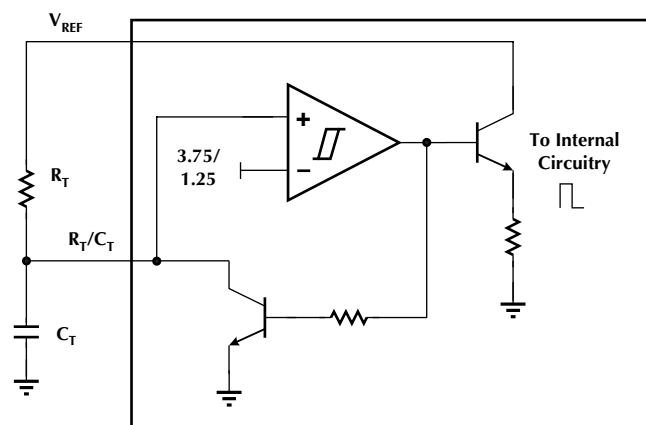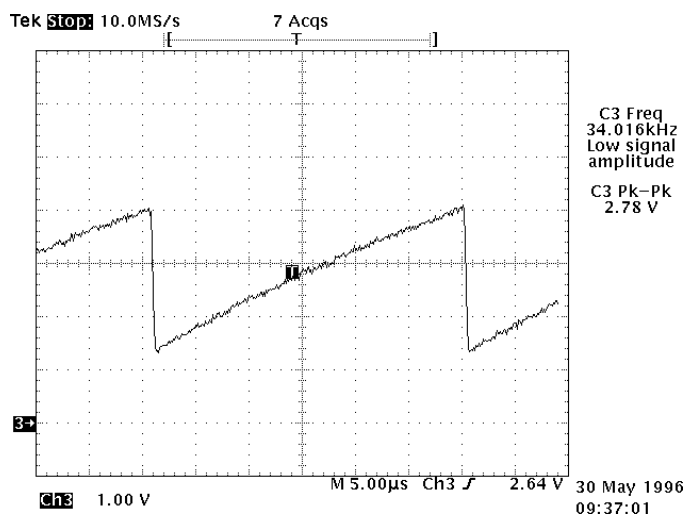

Figure 1. Typical Controller Oscillator Circuit

Figure 2. Controller Oscillator Voltage Ramp

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A simple and inexpensive method of synchronizing the controller to the system clock is shown in Figure 3. For the controller to sync, its free running frequency must be 85% to 95% of the system clock. Then, providing the sync waveform's amplitude is great enough, the controller will lock to the system clock with the resulting voltage ramp waveform shown in Figure 4. This approach always locks the controller's ramp discharge event (falling edge) to the system clock's rising edge.
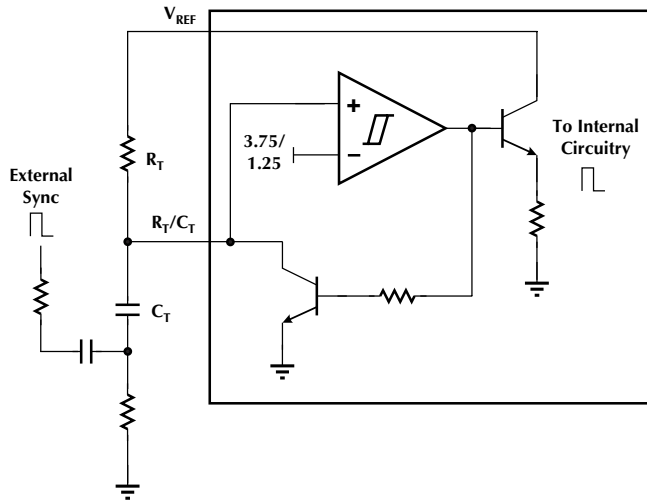

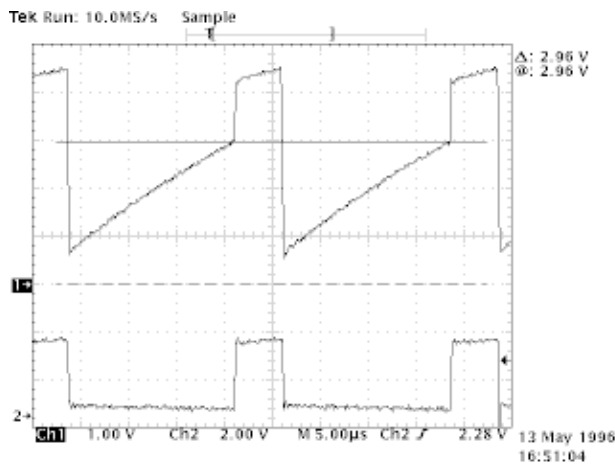**Figure 3. Controller Oscillator Circuit (with External Synchronization)**

Figure 4. Controller Oscillator Voltage Ramp (Synchronized to External Clock)

The two most obvious limitations to this method are the limited locking range (<1.2:1) and the resulting corruption of the voltage ramp (Figure 4). To overcome these limitations a more complex method is required. This usually consists of a complex digital switching scheme to select different timing resistor (or capacitor) values, especially if the frequency range is large.

WIDE FREQUENCY RANGE SYNCHRONIZATION

A novel approach for synchronizing the controller to a wide frequency range uses a PLL (Figure 5). This method locks the controller to any frequency within the range of the voltage controlled oscillator (VCO). The unique feature of this method is that the controller's oscillator becomes the VCO.
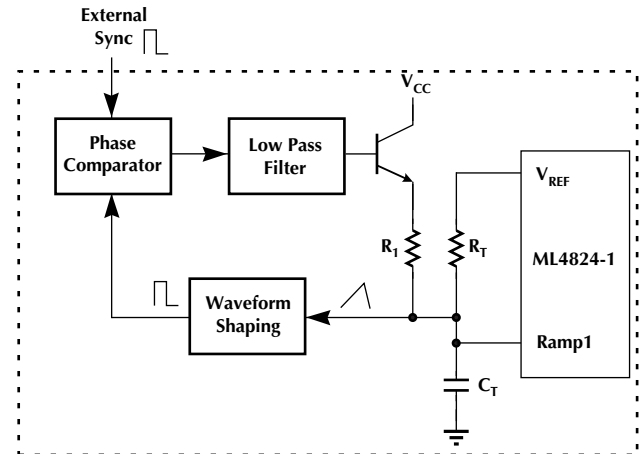

Figure 5. PLL Controlled Synchronization

PRACTICAL EXAMPLE

The circuit shown in Figure 6 is the oscillator and sync section of a fully functional power factor corrected (PFC) switch-mode supply designed to power a CRT monitor. The controller's frequency locks to the horizontal sweep frequency. The design locks to any frequency from 25kHz to 75kHz without any hardware changes.

Theory of Operation

The phase comparator (contained in U1) is the key to wide frequency range locking. When the sync input frequency is greater than the controller's input frequency the phase comparator's output voltage is high, supplying more charge current to CT via Q1 and R4. Conversely, when the sync frequency is less than the controller's the comparator's output is low, thereby reducing the controller's frequency. When the loop is balanced the controller and sync frequency are equal and the falling edge of the controller voltage ramp is locked to the rising edge of the sync waveform. The low pass filter values (R_1, C_3) were chosen empirically to result in a low ripple voltage to the base of the buffer transistor Q1. Although U1 contains additional circuitry not needed in the example circuit, some users may benefit from the internal 50% duty cycle VCO as a local reference oscillator. For more information on the internal circuitry in U1 consult the manufacturer's data book.

Design Formulas

To begin the design calculate the timing resistor from Equation 1. Note the timing capacitor CT has already
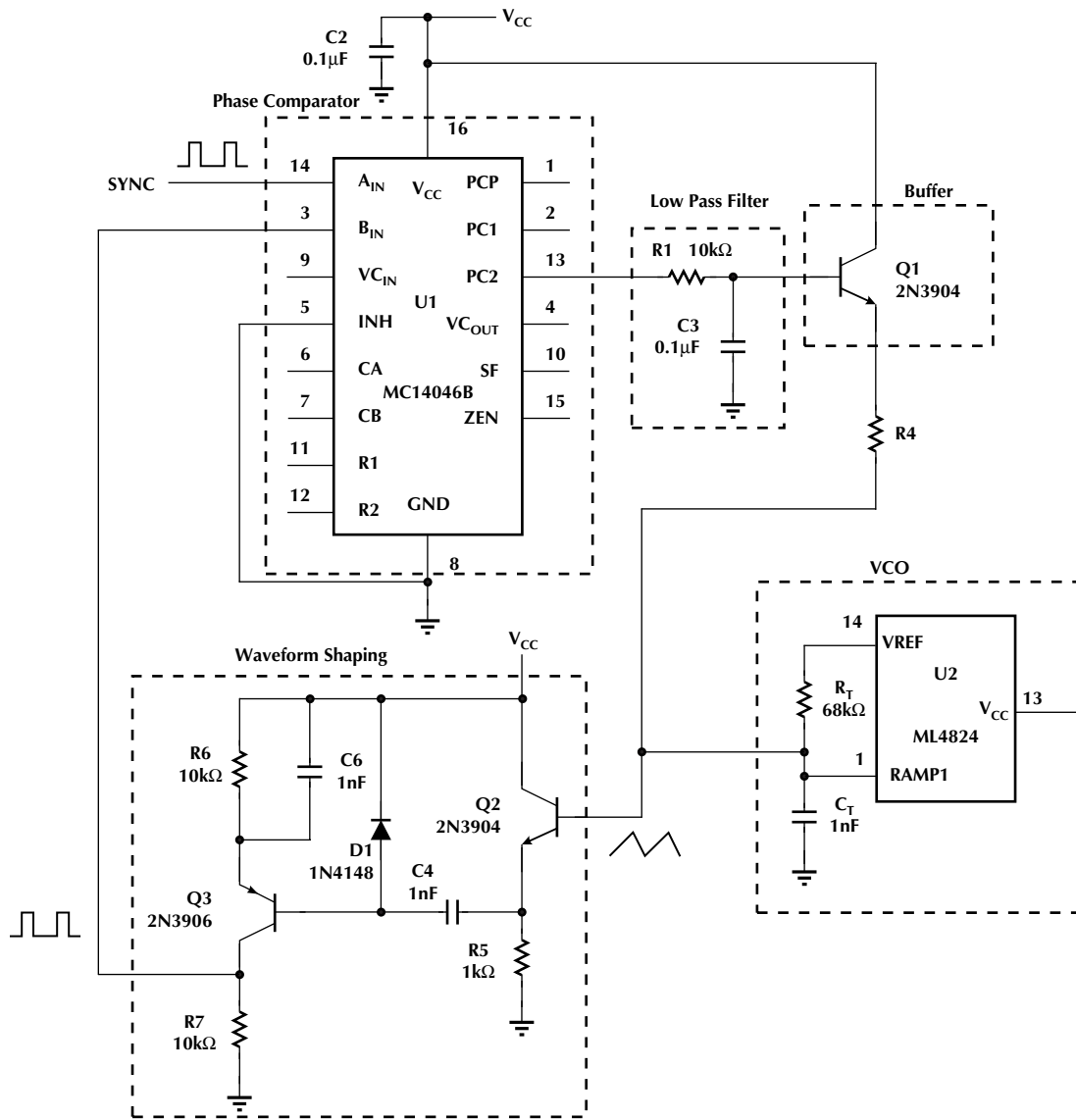
Figure 6. Wide Frequency Synchronizing Range PWM Power Supply Controller Schematic

been chosen small enough to permit the shortest possible ramp voltage discharge times with the ML4824. This results in the highest possible duty cycle in the PFC section.

$$(1) \qquad R_T \cong \frac{1}{0.51 C_T f_{osc(MIN)}}$$

$$R_T \cong \frac{1}{(0.51)\left(1 \times 10^{-9}\right)\left(2.5 \times 10^4\right)}$$

Since $R_T \cong 78.4k\Omega$ in the formula, use $82k\Omega$.

Next the frequency range is determined in Equation 2:

$$(2) \qquad f_{RANGE} \cong \frac{f_{osc(MAX)}}{f_{osc(MIN)}}$$

$$f_{RANGE} \cong \frac{75kHz}{25kHz}$$

Thus $f_{RANGE} \cong 3{:}1$.

Now the value of R1, which determines the upper frequency limit, is determined in Equation 3:

(3)

$$R_1 \cong \frac{\left(8.2 \times 10^4\right)(12 - 2.5)}{\left(\left(8.2 \times 10^4\right)\left(1 \times 10^{-9}\right)(2.5)\left(7.5 \times 10^4\right)\right) - (7.5 - 2.5)}$$

And $R_1 \cong 75k\Omega$ (where $V_{R(P-P)}$ is the peak-to-peak value of the voltage ramp.

CONCLUSION

When synchronization of the power supply controller is necessary or beneficial care must be exercised to avoid degrading the oscillator's voltage ramp. As shown, even when synchronizing to a single frequency, degradation can result with the addition of the sync pulse to the ramp. This can become even more serious due to component tolerances, the controller oscillator trip voltages, and discharge current production variations. The use of a PLL, while using the controller oscillator as a VCO, guarantees ramp voltage integrity and eliminates the influence of component tolerance. For wider frequency range synchronization the use of a PLL is necessary for proper controller operation without the cost and complexity of existing solutions.
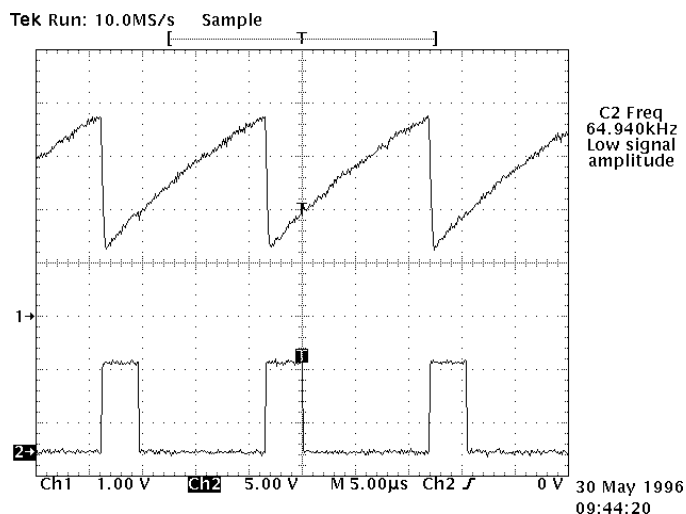
Figure 7. Controller Oscillator Voltage Ramp (Synchronized with a PLL)