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Application Note 42030

Theory and Application of the ML4821 Average Current Mode PFC Controller

THEORY OF OPERATION

The increasing importance of power factor correction has created a demand for active power factor controller Integrated Circuits. Power factor correction requires special control circuits that are able to force the input current waveshape to be sinusoidal and in phase with the input sinusoidal voltage.

There are several ways that this can be accomplished. One method is the average current mode controlled boost topology power factor correction circuit using the ML4821 dedicated average current mode controller IC. This paper is going to present enough theoretical background information, along with practical examples, to enable the design of such circuits.

Average current mode control can produce a high quality input sinusoidal current waveform. Although it can be used with many different power supply topologies, it excels when it is used with the continuous inductor current boost topology.

POWER FACTOR CORRECTION

The following information looks into how a power factor correction circuit operates.

Figure 1 shows the simplified block diagram of a power factor correction circuit. The circuit functions by monitoring the input full wave rectified line voltage as well as the output voltage. The two feedback signals are combined to modulate the average input current waveform in accordance with the rectified line voltage, while regulating the output over line and load variations.

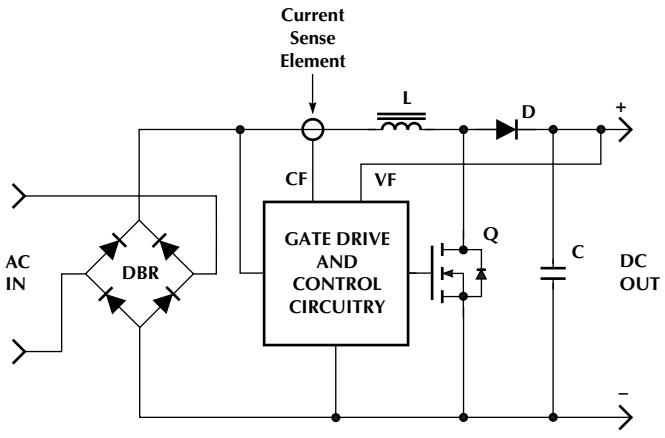

Figure 1. Top Level Block Diagram of the Power Factor Controller

Figure 2 shows the basic circuit diagram of a Power Factor Controller (PFC) with all necessary connections made. The heart of the circuit is the current modulator. The modulator consists of a linear gain modulator, a current amplifier, and a Pulse Width Modulation (PWM) comparator. These three functional blocks enable the circuit to force the input current to be sinusoidal.

A current that is proportional to the input full wave rectified voltage is produced with the help of resistor R_L. This is called the reference. The reference is applied to one of the inputs of the gain modulator. The other input of the gain modulator is the output of the voltage error amplifier. Assume that the output of the voltage error amplifier changes slowly compared to the line frequency. This is in general true since the bandwidth of this amplifier is set low by its feedback components.

The gain modulator is a current input type. This enables the gain modulator to have significant immunity to ground noise. When there is a current at its input its terminal voltage is one diode drop above ground. It is part of a current mirror. Therefore, a voltage source of low impedance should never be applied to this input.

The output of the gain modulator is a current that is the product of the reference current and the output of the error amplifier that monitors the output voltage. This output current is applied to resistor R_C (see Figure 2). This voltage subtracts from the sensed voltage across R_S and is applied to the current error amplifier. Under closed loop control the current error amplifier will try to keep this voltage differential close to zero volts. This forces the voltage produced by the return current on R_S to be equal to the voltage across R_C. Since this requires dissipative sensing, R_S is a power resistor of low value.

The amplified current error signal is then applied to the inverting input of the PWM comparator. The other input of the PWM comparator is the ramp generated by the timing capacitor of the oscillator. Pulse width modulation is obtained when the amplified error signal that sets up the trip point modulates up and down.

The rest of the circuit is very similar to conventional PWM control schemes. In this topology, however, the loops operate around zero volts.

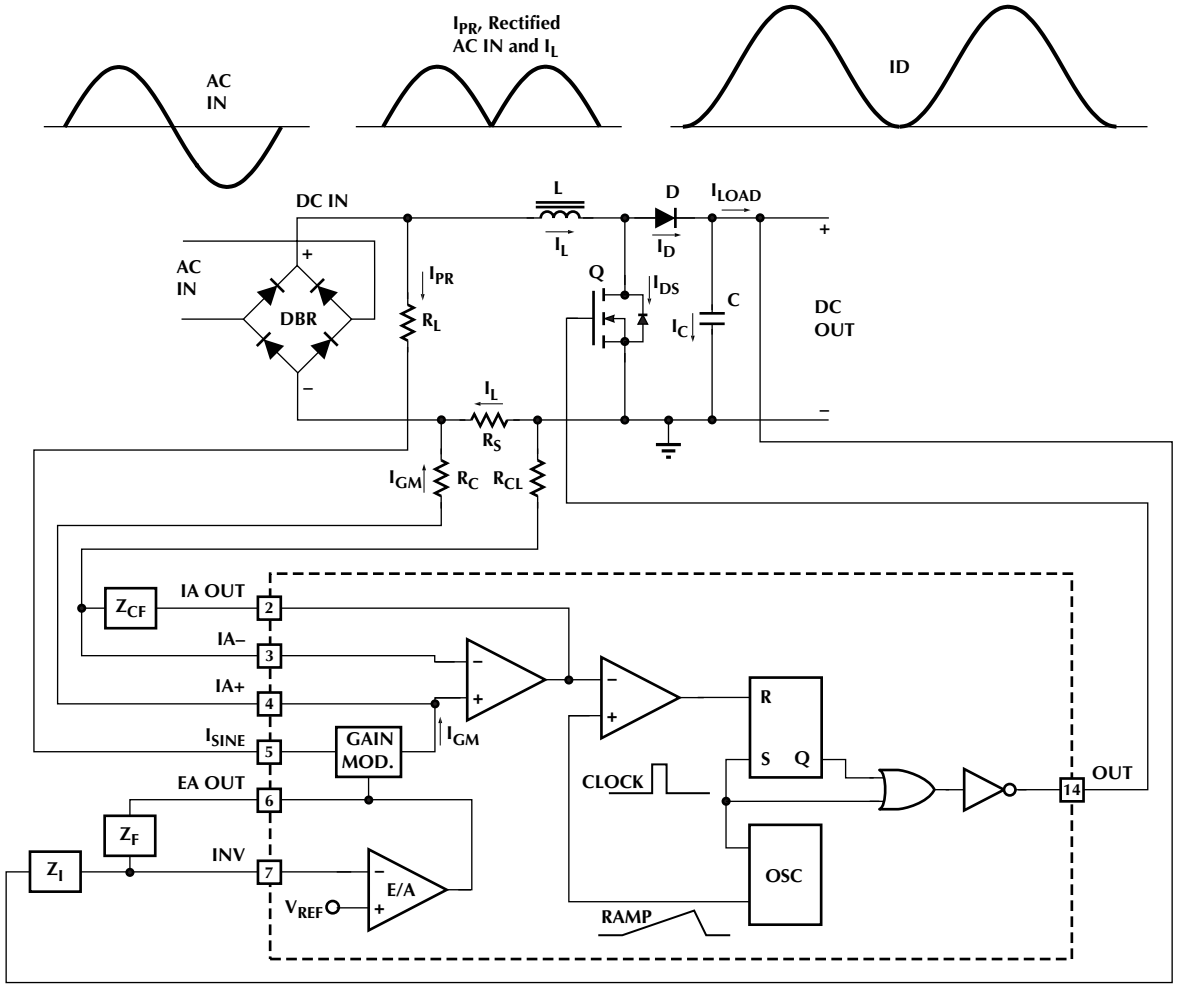

Figure 2. Basic PFC Circuit

MULTIPLE LOOP CONTROL

The PFC circuit is a multiple loop control circuit. There are two control loops, not counting the fault control loops such as peak current limit and overvoltage protection.

The first loop is the current loop that forces the input current to be sinusoidal. The second loop is the output voltage control loop that keeps the output voltage above the peak of the input voltage. The output voltage of a continuous inductor current boost regulator has to be set above the maximum peak of the input voltage in order to function correctly as a PFC. For a PFC that will operate to 260VAC the output voltage should be at least 370VDC ($260V \times \sqrt{2}$) at its minimum point.

To gain familiarity with the operation of the PFC it is necessary first to understand the waveforms and signals at the various critical points. Some of these waveforms are shown at the top of the schematic of Figure 2. By definition the average value of the input current follows a sinusoidal shape. That also means that the average value of the boost inductor L has to be sinusoidal. We say the average value because there is current ripple at the switching frequency. 100kHz is a good trade-off point between inductor size and circuit efficiency. Switching losses in the circuit will include major losses in the MOSFET, the output diode, and the inductor. Because the MOSFET is charged to the output voltage at every turnoff, switching losses will be significant at any input voltage and output current. The output diode must reverse recover high current with the full output voltage. Core losses in the inductor will not be as significant because the 100kHz AC ripple current is relatively low compared to the 120Hz polarized ripple current.

For the purposes of this next analysis ignore the 100kHz current ripple in the inductor. Also assume that somehow the MOSFET duty cycle is such that the inductor is forced to carry a current that has a full wave rectified sinusoidal waveshape. From the operation of the boost circuit there needs to be equilibrium throughout the entire 50Hz or 60Hz cycle. Large signal equations describing the operation of the boost circuit should hold.

$$V_{OUT} = \frac{V_{IN}}{1 - D_{ON}} \quad (1)$$

$$D_{ON} = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (2)$$

Since $V_{IN} = V_{IN}(t) = \sqrt{2}V_{INRMS}|\sin(\omega t)|$ we get

$$D_{ON} = d_{ON}(t) = \frac{V_{OUT} - \sqrt{2}V_{INRMS}|\sin(\omega t)|}{V_{OUT}} \quad (3)$$

Also by definition

$$i_L(t) = \sqrt{2}\frac{P_{OUT}}{V_{INRMS}}|\sin(\omega t)| \quad (4)$$

The MOSFET $i'_L(t) = \sqrt{2}\frac{P_{OUT}}{V_{INRMS}}\sin(\omega t)$ current is the inductor current chopped at high frequency with the duty cycle of equation 2. However, the diode current is the inductor current chopped at high frequency with a duty cycle of 1 – $d_{ON}(t)$. By substituting we can get an expression for the average current that passes through diode D (*i.e.*, $I_D = i_d(t)$).

Note: The prime (') following a variable (*e.g.,* i') denotes average value.

$$i'_d(t) = i'_L(t)\left[1 - d_{ON}(t)\right] \quad (5)$$

By substituting equations 3 and 4 into 5

$$i'_d(t) = 2\frac{P_{OUT}}{V_{OUT}}\sin^2(\omega t) \Rightarrow i'_d(t) = \frac{P_{OUT}}{V_{OUT}} - \frac{P_{OUT}}{V_{OUT}}\cos(2\omega t) \quad (6)$$

As can be seen from the above equation the diode current consists of two parts. It has an average value consistent with the output power and output voltage (first term). Also it has an AC component with a peak value equal to that of the average value. The DC part of this current is simply the output load current. It flows through the output load. The AC part however flows through the output capacitor C. Consequently it may become a parameter when determining the value of this capacitor.

There are two control loops for the PFC: an inner high bandwidth current loop, and a much slower outer voltage loop. Figure 3 shows the two loops in block diagram form. First the two loops will be examined separately. Then the criteria for proper connection will be shown.

THE CURRENT CONTROL LOOP

The current control loop constitutes the inner loop and its job is to force the input current waveshape to follow the shape of the input voltage. It does this by modulating the duty cycle of the MOSFET in the power stage. The input voltage is a full wave rectified sine wave. Thus it is rich in harmonics. The current control loop along with the power stage has to have enough bandwidth to follow this full wave rectified waveform. It can be shown that a bandwidth of a few kHz is sufficient. In order to proceed we need to derive expressions that give the responses of both the power stage and of the current loop.

As can be seen from Figure 4 the input of the power stage is the duty cycle output of the current pulse width modulator. Therefore we can describe the power stage as a functional block that has as its input the duty cycle information and as its output the sensed voltage across the sense resistor R_S. The average current that flows through this resistor is equal to the average current that flows at the input of the PFC.

We can define

$$G_{PS}(s) = \frac{V_S(s)}{D_{ON}(s)} \quad (7)$$

as the gain of the power stage. The response can be found by assuming that the output voltage is constant and by using the state space averaging technique. The response shows a single pole roll off and is given by

$$I_L(s) = \frac{V_{OUT} \times D_{ON}(s)}{sL} \quad (8)$$

Since $V_S(s) = R_S I_L(s)$,

$$G_{PS}(s) = \frac{V_{OUT} \times R_S}{sL} \quad (9)$$

The above expression gives the small signal gain of the power circuit in the complex s-domain. It is the ratio of

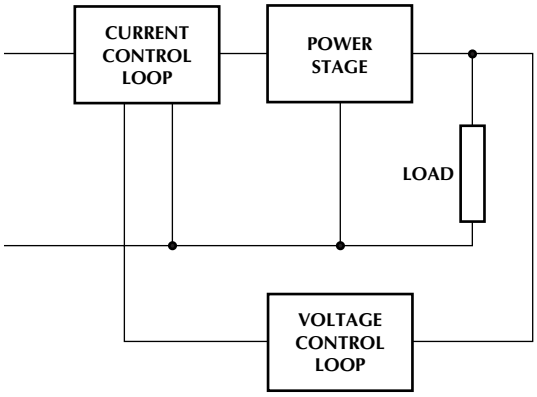

Figure 3. The Two Loops of a PFC

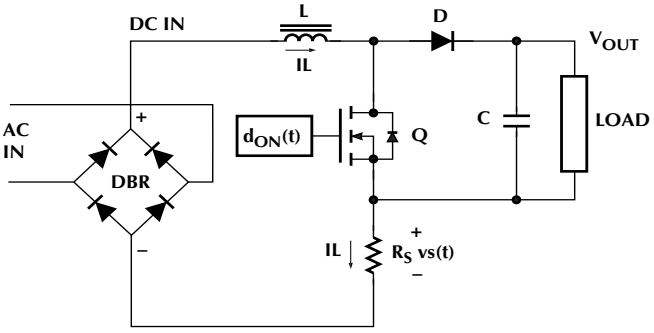

Figure 4. The Power Stage

the sensed current waveform voltage to the incremental changes in the duty cycle. The next step is to incorporate into the above power stage gain the gain of the pulse width modulator. To do this, first find the gain of the modulator itself. This requires a determination of the amplitude of the applied ramp to the noninverting input along with the allowable voltage swing range at its inverting input. The gain of the modulator is

$$G_{PWM} = \frac{\Delta D_{ON}}{\Delta V -} \quad (10)$$

where ΔV– is the voltage at the inverting input of the PWM comparator.

For the ML4821 the amplitude of the oscillator is 5.2V peak-to-peak. Therefore, when the voltage at the inverting input of the PWM comparator changes by 5.2V the duty cycle goes from zero to maximum duty cycle. If we assume that the deadtime is very small (normally around 5%) the gain of the PWM stage becomes

$$G_{PWM} = 1/5.5$$

Now we can combine the gains of the power and PWM stages to get the following

$$G_{PST} = \frac{V_S(s)}{V-(s)} = \frac{V_{OUT} \times R_S}{5.5sL} \quad (11)$$

Note that in actuality V – (s) = V_{IAOUT}(s). Therefore, the overall current loop response will be determined by the responses of the current amplifier and the power stage. This in turn will be dictated by the required current loop bandwidth. For good waveform quality the total response should have a bandwidth of at least several kHz.

DETERMINATION OF THE CURRENT LOOP BANDWIDTH

The following equation gives the theoretical upper limit for this bandwidth

$$f_{CLCO} = \frac{f_S}{6} \quad (12)$$

Thus, for an operating frequency of 100kHz, the maximum allowable current loop bandwidth is approximately 16kHz.

The Gain Adjustor

Analysis of the voltage control loop shows that as the RMS AC input voltage goes up, the system gain increases by V_{RMS}^2. The gain increases with input voltage since the input voltage drives the noninverting input to the gain modulator. The second term is because the dI/dT on the inductor increases in proportion to the input voltage.

Since the gain varies with V_{RMS}^2, it then follows that the unity gain crossover frequency of the loop will change with a 1:8 ratio as the line changes from 90VAC to 260VAC. This complicates the loop design since the wide variation in crossover frequency would require the low line crossover frequency to be set very low while the high line crossover frequency would be set high.

The ML4821 cancels the square law dependency of gain vs. V_{RMS} by adjusting the gain of the gain modulator as a function of the RMS input voltage. The gain modulator gain is of the form I_{GM} is proportional to kV_{EAOUT}, where k varies in a nonlinear fashion with respect to V_{RMS}. This gain adjustment is accomplished by deriving a DC voltage proportional to V_{RMS} and imposing it on pin 8 of the ML4821.

The following describes how to design an appropriate network that will accomplish this task. The Figure 5 curve shows the gain adjustor gain with respect to the voltage at pin 8. The curve has been separated into two parts. The right hand part shows operation under normal conditions in the voltage range from minimum line voltage to maximum line voltage (90VAC to 260VAC). The 85VAC minimum normal operating point on the curve has been chosen to account for tolerances. Under normal operating conditions as input voltage increases the gain decreases, compensating for the rise in the loop gain.

Under brownout conditions (below 85VAC) the gain decreases to limit the amount of current that is drawn from the line which prevents an overload condition. This is a very useful feature, since in many cases the load for a PFC is a constant power load and the input current has to rise to a high value to compensate for a drop in the input voltage.

Figure 6 shows the way pin 8 should be connected to the input line. The network consists of R8, C3, R9, R15 and C7 to form a two stage RC low pass filter and voltage divider. To calculate the values of the components note that the start of the brownout condition is at 85VAC, which corresponds to approximately 2V at pin 8. Then set the output voltage of the Figure 6 filter/divider network to 2.8V at 120VAC.

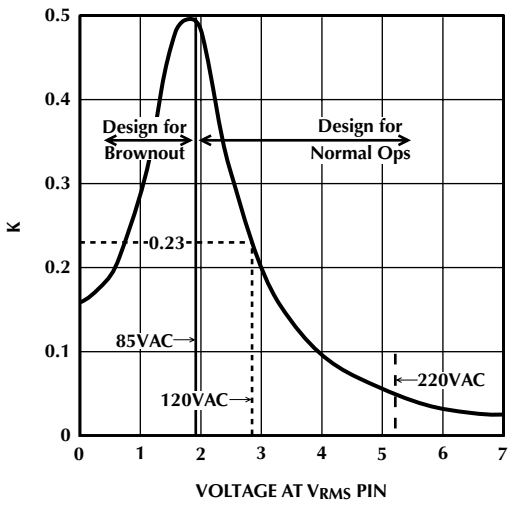

Figure 5. K Factor

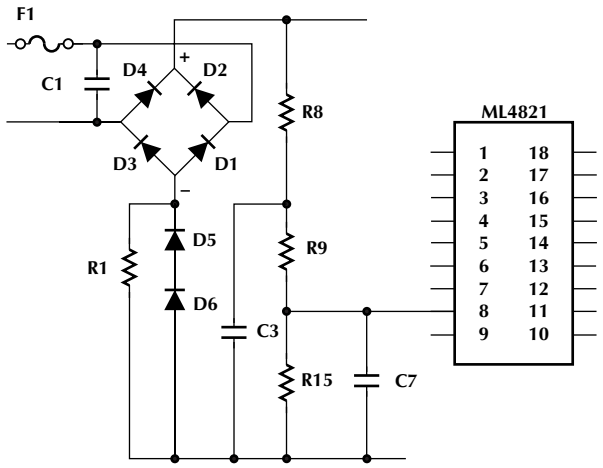

Figure 6. V_{RMS} Sensing Network

The RMS value of the input sine wave is equal to the RMS value of the full wave rectified sine wave after the full bridge rectifier. The average value of the full wave rectified sine wave is proportional to its RMS value and they are related as follows

$$V_{AVG} = \frac{2\sqrt{2}V_{INRMS}}{\pi} \quad (13)$$

The average voltage at pin 8 is given by

$$V_{PIN8} = \frac{R15}{R8 + R9 + R15} V_{AVG} \quad (14)$$

Assume R8 = 910kΩ and R9 = 91kΩ; and R15 can be found by setting equation 14 to 2.8V and solving for R15.

In this case R15 has a value of 27kΩ.

The values of C3 and C7 are chosen for attenuation at 120Hz and minimum delay. They are: C3 = 0.1µF and C7 = 0.47µF.

These capacitor values are acceptable for most applications, even though the resistors may change to accommodate different brownout or operating conditions. These values are independent of output power.

With the gain adjustor functional, the gain modulator output current is given by

$$I_{GM} = K \times I_{SINE} \times (V_{EAOUT} - 0.8) \quad (15)$$

where

I_{SINE} = reference current through pin 5.

K = gain adjustor gain This quantity is dependent on the voltage present at pin 8 (see Figure 5). This K is related to the k referred to earlier, but it is not equivalent.

V_{EAOUT} = output voltage of the error amplifier.

The maximum value of the gain modulator output current is limited by the value of the timing resistor and it is given by

$$I_{GMMAX} = \frac{2.5}{R_T} \quad (16)$$

A typical value for R21, for 100kHz operation, is 6.2kΩ, in which case I_{GMMAX} = 400µA.

It is a good idea to limit the maximum output current of the gain modulator below the current limit point, but high enough to get maximum output power.

Output Capacitance

The parameters that affect the choice of the output capacitance are:

1. Holdup time capability, usually 20msec for computer power supplies.

2. Ripple current handling capability.

3. Allowable third harmonic distortion.

The holdup time capability is the amount of time at rated output power that it will take the capacitor voltage to discharge to a minimum operating voltage. The start point of the dropout should be the minimum operating output voltage. For this type of PFC that is usually less than the nominal value of 380VDC.

$$C_{OUT} = \frac{2P_{OUT} \times t_{HLD}}{V_{OUTMIN}^2 - V_{OPMIN}^2} \quad (17)$$

where:

C_{OUT} = output capacitance.

P_{OUT} = output power.

t_{HLD} = holdup time, normally 20msec.

V_{OUTMIN} = minimum value of the regulated output voltage, normally happens at full load.

V_{OPMIN} = minimum input voltage of the driven load, usually a switching power supply.

The chosen capacitor should be able to handle the ripple current that will flow through it. The peak value of this ripple current is equal to the output DC current. The RMS ripple current through the capacitor is

$$I_{COUTRMS} = \frac{I_{OUTDC}}{\sqrt{2}} \quad (18)$$

The third consideration in the determination of the output capacitor is the output ripple voltage which can be found using the following

$$|V_{OUTRIPPLE}|_{PEAK} = I_{OUTDC}\sqrt{\left(\frac{1}{4\pi f_L \times C_{OUT}}\right)^2 + ESR^2} \quad (19)$$

where:

f_L = line frequency.

ESR = the ESR of the output capacitor.

Depending on the value of the output capacitor the contribution of the ESR on the output ripple voltage may or may not be ignored.

The output ripple voltage will contribute to the third harmonic distortion of the input current. The actual amount will depend on the value of the output ripple voltage and the gain of the error amplifier at 120Hz.

The Voltage Control Loop

The inner current control loop can be modelled as a controlled current source. This simplifies the analysis of the voltage control loop.

Typical loads for a PFC are switching power supplies which are essentially constant power loads. These kinds of loads exhibit negative resistance at their input terminals. An increase in the input voltage causes a drop in the input current. It is important that the voltage control loop error amplifier is correctly compensated. The two other types of loads are constant resistance and constant current.

It is necessary to analyze the loop to find out what parameters affect its dynamics. It has been noted that this loop has a very low bandwidth. If the bandwidth of this loop is high, an excessive amount of the second harmonic component present at the output will be injected in the control loop causing third harmonic distortion of the input current. Typical values for this loop are between 10Hz and 20Hz. The voltage control loop's open loop gain is calculated by finding the change in the output voltage of the error amplifier that produces the required maximum output power change. This can be done by using the following expression

$$\Delta V_{EAOUT} = \frac{P_{IN} \times R_S \times R_L}{R_{GM} \times K \times V_{RMS}^2} \quad (20)$$

where:

P_{IN} = maximum input power.

R_S = current sense resistor.

R_L = input voltage sense resistor that connect to pin 5.

R_{GM} = resistor at the output of the gain modulator.

K= gain adjustor gain at V_{RMS}, from the curve of Figure 5; K at 120VAC is 0.23.

V_{RMS} = input RMS voltage, this voltage is normally 120VAC.

Thus the open loop gain can be found to be

$$|G_{V.O.L.}|_{dB} = 20\log\frac{P_{IN}}{2\pi f C_{OUT} \times V_{OUTDC} \times \Delta V_{EAOUT}} \quad (21)$$

where $G_{V.O.L.}$ is the open loop response for the voltage error amplifier.

Equation 21 gives the response of the magnitude with respect to frequency. The response has a –20dB/decade slope and a constant phase lag of 90 degrees. A suitable error amplifier configuration is shown in Figure 7.

Calculation of the Output Voltage Sense Resistors

Pick a value for the output voltage under full load. The load regulation of the PFC can be expected to be 15V to 30V. For a minimum output that is high under full load there is the danger that under no load conditions the output voltage will be over 400V. Normally a minimum value of 370V will result in a high value of less than 400V. The reason for this seemingly poor regulation is because of a configuration of the error amplifier with a feedback resistor, R_F, that is equal to or less than R_H. Much better DC regulation can be obtained by using a blocking capacitor in series with R_F, but it will degrade the transient response of the circuit, introducing a bounciness to the input current under transient conditions.

The output voltage of the error amplifier should be designed for 4V to 5V maximum at full load. Higher voltage gives better noise immunity and dynamic range. However, that means the output voltage will have a larger variation due to its influence on the output voltage dividers. Start with 4.4V. A value for R_H is picked that is normally between 680kΩ and 1MΩ. In this case it is 825KΩ. The value of the feedback resistor is found based on the loop design criteria. With these two values and the minimum output voltage defined, R_L can be calculated using the following formula:

$$R_L = \frac{5 \times R_H \times R_F}{R_F(V_{OUTMIN} - 5) - 0.6R_H} \quad (22)$$

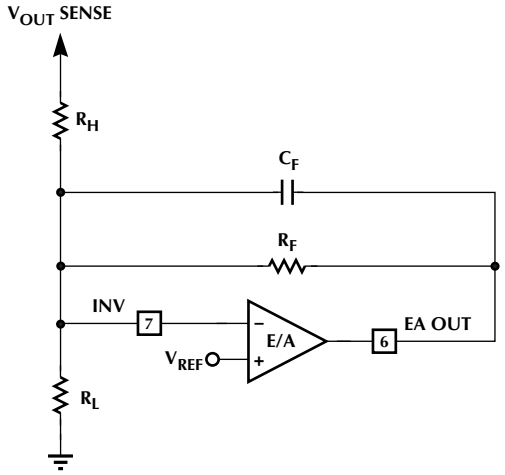

Figure 7. Error Amplifier Configuration

See Figure 8 for definitions of the parts.

With the above chosen and calculated values one now can determine the maximum output voltage under no load conditions as follows:

$$V_{OUTMAX} = R_H\left(\frac{4.3}{R_F} + \frac{5}{R_L}\right) + 5 \qquad (23)$$

Calculation of the OVP components:

The sense resistors for the OVP circuit are easier to calculate. The voltage point at which the OVP circuit will act is determined in part by the maximum voltage at the output before damage due to overvoltage can occur. A good rule of thumb, which may not be applicable in all cases, is to set a voltage that is 10 to 15V higher than V_{OUTMAX} as calculated in formula 24. Therefore $V_{OVP} = V_{OUTMAX} + 10V$.

OVP protection is facilitated by connecting a voltage divider to pin 11. The high side of this divider is connected to the output terminals of the PFC and the low side to ground. Call these two resistors R_{OVPH} and R_{OVPL}. Assume a value for the high side resistor and calculate the value of the low side. For that purpose one can use the following formula

$$R_{OVPL} = \frac{5 \times R_{OVPH}}{V_{OVP} - 5} \qquad (24)$$

The OVP pin on ML4821 is a multifunction pin. Pin 11 is also used for remote shutdown. When this pin is pulled to ground the IC shuts down. The pin can be pulled to ground using a small signal FET or bipolar transistor, such as the 2N2222. Due to this multifunctionality the pin should be biased higher than 1.0V whenever the part needs to be operated without input power applied. Extreme care should be exercised, however, when input power is applied. Make sure that the voltage on this pin reflects the correct divided-down output voltage for safe operation.

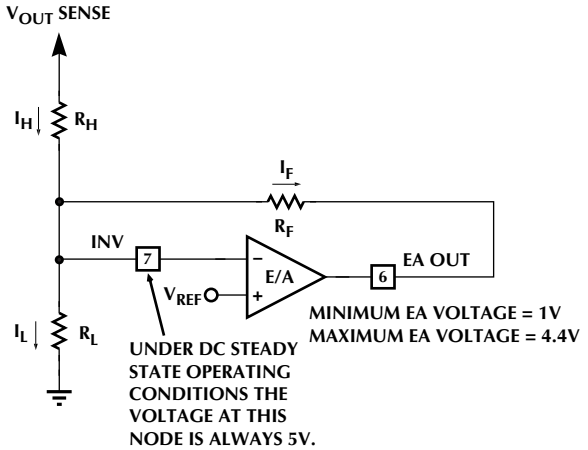

Figure 8. DC Part of the Feedback Circuit

Block Diagram of the ML4821

Figure 9 shows the block diagram of the ML4821. There are other functions beyond those previously discussed which extend its usefulness in various applications. One of them is the SYNC function that enables the IC to frequency lock to an external oscillator. Pin 10 is reserved for this function. A positive pulse on this pin ≥2V resets the oscillator's comparator and initiates a discharge cycle for the timing capacitor connected to pin 17. For proper operation, however, the ML4821 oscillator should be set to operate at a frequency that is roughly 10% to 15% lower than that of the external driving source.

The rectangular block labeled gain modulator combines both the gain modulator function and the gain adjustor functions that were mentioned earlier.

Another useful function is the Soft Start function. This may be applied where controlled output voltage rise is desired. To use this function effectively, however, it is necessary to have an auxiliary bias power supply to supply and maintain power to the control circuitry while the output voltage of the PFC is slowly rising. The amount of the Soft Start capacitance required is a function of the delay in the output voltage rise time and the internal charging current.

The undervoltage lockout function of the IC reduces current drawn from the rectified line to power the IC in order to simplify bootstrap circuit designs. An example of such bootstrapping is illustrated in Figure 10 (components C12 - C14, D7, D8, and R10).

The Boost Inductor

One of the key components in the PFC is the boost inductor. The value of this inductor affects many other design parameters. Most of the current that flows through this inductor is at low frequency (assuming low percentage ripple). This is particularly true at the lowest input voltage where the input current is highest.

Normally the acceptable level of ripple current is between 10% and 20%. For operation at 100kHz the following formula will produce acceptable results

$$L = \frac{150 \times V_{OUT} \times V_{MINRMS}}{P_{OUT} F_{SW} X} mH \qquad (25)$$

where:

V_{OUT} = Bus voltage.

V_{MINRMS} = Low line input voltage.

P_{OUT} = Output power.

F_{SW} = Switching frequency.

X = Ripple current factor.

The peak to peak ripple current for any input/output voltage combination can be found by using the following formula

$$\Delta I_{L_{p-p}} = \frac{V_{IN}(V_{OUTDC} - V_{IN})}{fLV_{OUTDC}} \quad (26)$$

where:

V_{IN} = peak value of the input full wave rectified waveform.

f = operating frequency.

For an output voltage of 380V the maximum peak-to-peak ripple happens when the input voltage is 134VAC and its value can be calculated using

$$\Delta I_{L_{p-p}MAX} = \frac{V_{OUTDC}}{4fL} \quad (27)$$

This triangular ripple current, made up of components of both the switching frequency and its harmonics, will produce a ripple voltage on the input impedance.

The Input High Frequency Bypass Capacitor

This capacitor, which should normally be at the line side of the input bridge rectifier, helps to bypass the high frequency ripple current. Its impedance is a few Ohms at the switching frequency. Therefore, there is a need for additional filtering at the input, if differential conducted noise specifications are to be met. Note that this capacitor has to be an approved across the line type (an X-type capacitor).

DESIGN OF A 200W 100KHZ PFC

The complete schematic diagram of a 200W PFC is shown in Figure 10. The following paragraphs cover in detail the pin by pin design of this PFC. The formulas and the procedures presented in the previous sections will be used. Although the design is at 200W it can easily be extended for power levels above that.

Begin by choosing the main components such as the boost inductor L1 and the output capacitance.

The Boost Inductor

We can use equation 25 for the calculation of the inductor value

$$L = \frac{150 \times 380V \times 85V}{200W \times 100kHz \times 0.15} = 1.6mH$$

The ripple current factor, X, is a peak-to-peak current expressed as a percentage of the peak input sinusoid current. The peak of this ripple current will be added to the peak of the input sinusoid. Therefore, the maximum peak current that the inductor will see is simply the peak of the input sinusoid plus ½ the ripple current at 85VAC.

Assuming 85% efficiency for the boost stage the input power will be 235W. If there is another conversion stage, such as a PWM, the efficiency of that stage should also be considered in equation 25. This results in an input RMS current of approximately $2.6A_{RMS}$ with a corresponding peak value of 3.7A.

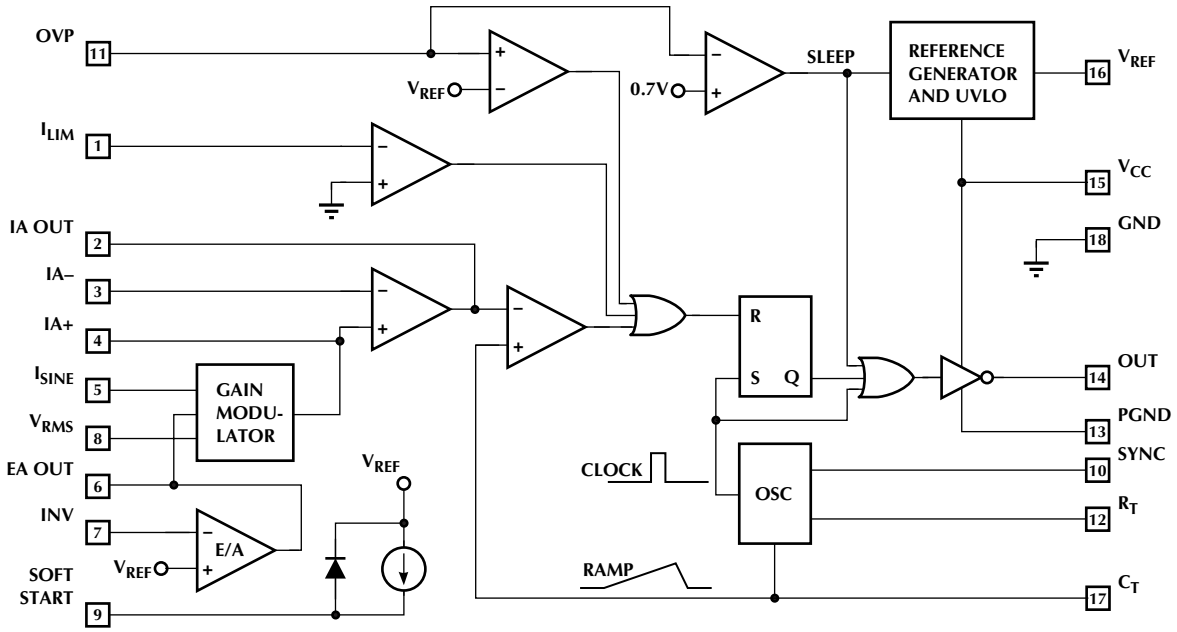

Figure 9. Block Diagram of ML4821

The peak ripple current is arbitrarily chosen to be 15% of the peak current at 85VAC. Therefore, the peak inductor current is 4A.

$$I_{LPEAK} = 3.7A + 0.555A/2 = 4A$$

The choice of core material should be such that the inductance will not change significantly when this current passes through the winding.

It is important to remember that the higher the inductance the lower the ripple current, which in turn means less filtering is required on the input line to meet line-conducted noise requirements. It also means lower core losses. The consequence is a greater number of turns and higher copper losses, or a physically larger inductor. With excessively large inductance values the low ripple current will produce a low signal to noise ratio in the current control loop and may cause erratic switching.

Good candidates for core materials are:

Powder Iron Cores

Mollypermalloy Cores

Gapped Ferrite Cores, provided that the gap is not excessive.

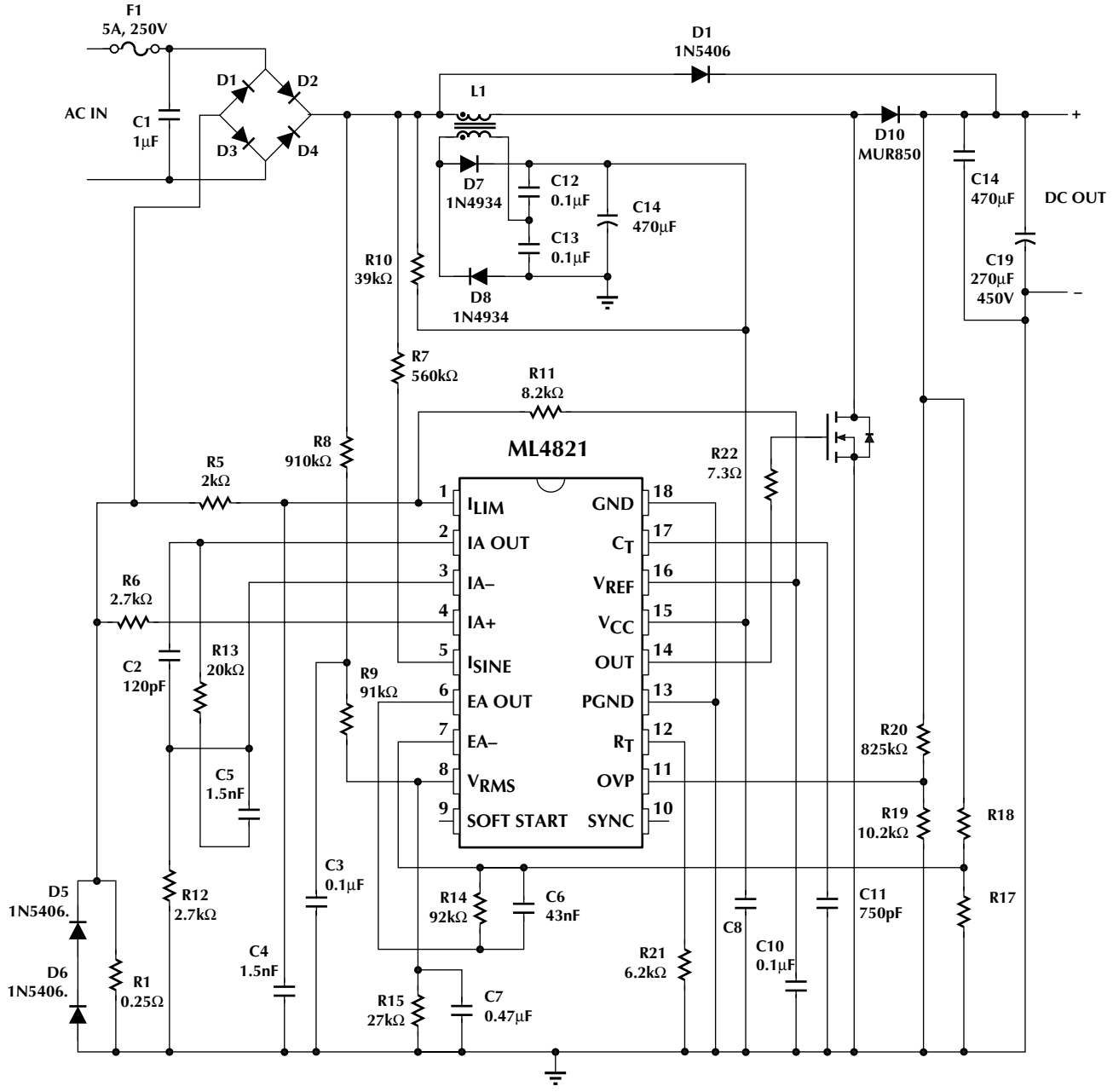

Figure 10. Schematic Diagram of the 200W PFC

Normally, for any reasonable core material, core loss is not an issue due to the large number of turns required for such an inductor. The critical parameter is the change in its permeability under high current excitation with a large number of turns. Therefore, a careful analysis should be made to determine suitability of a core material for the given application.

For the present application we are going to choose a powder iron core of toroidal form. The core material is from Micrometals, Inc., and the part number is T184-40. Using the given inductance value it will contain 106 turns. Since a single layer winding for 22AWG is 102 turns, that is the value that will be used. This gives a ripple factor of 0.16, rather than 0.15. The inductor will maintain approximately 80% of its zero current inductance at 4A. Therefore, the inductance value will drop to 1.2mH at 4A.

This inductance value should then be used to check the ripple factor to see if it is still acceptable. With an inductance of 1.2mH at 4A the ripple factor is 0.2. This is still a reasonable value. The ripple current is of consideration both when designing the line input filter for the PFC and the ESR value of the bulk capacitor on the output. Because of the increased ripple current the total peak current will be slightly higher and the current limit point should therefore be correspondingly increased.

The Output Storage Capacitor

The criteria for the selection of this capacitor was covered earlier. Assume that a holdup time of 20msec is needed and the output voltage is allowed to drop from 370V to 330V before regulation is lost in the driven switching power supply. Use equation 17 to calculate a capacitance value

$$C_{OUT} = \frac{2 \times 200W \times 20msec}{(370V)^2 - (330V)^2} = 285\mu F$$

The rated voltage of this capacitor should be at least 450V. The closest standard value offered by United Chemi-Con is a 270µF type SMG with a voltage rating of 450V (a 330µF can also be used). Note that two capacitors of lower voltage rating (*i.e.*, 250V) can also be connected in series provided that shunt ballasting resistors are also used.

The Output Diode

The output diode (D10) should be an ultra fast type capable of supporting the peak input current for a couple of milliseconds. Power dissipation is the limiting factor. For this design an MUR850 was chosen. Note that various manufacturers (IR, Harris, APT, IXYS, *etc.*) have since developed FREDs (Fast Recovery Epitaxial Diodes) which will in general provide greater efficiency and reliability.

Surge Bypass Diode

This diode, labeled D9 on Figure 10, helps to bypass surges at the input line during start-up. This prevents possible saturation of inductor L1.

Output Circuit Very High Frequency Bypass

Capacitor C16 serves this purpose. It is used to control the output dI/dT loop. It can be a high voltage high frequency ceramic type of 0.01µF.

Oscillator Circuit

The choice for timing resistor R21 sets both the charging current for the timing capacitor and some other internal currents. One of them is the maximum gain modulator current (see equation 16). For a PFC operating at 100kHz a typical value for this resistor is 6.2kΩ. For details on how to calculate timing capacitor C11's value refer to the data sheet. For this application its value is 720pF.

Gate Drive

The gate driver of the IC can directly drive power MOSFETs. Normally a series resistor is used to damp any oscillations that may arise due to parasitic trace inductances and the gate capacitance. Its value should be chosen such that it will not result in excessive switching losses. If two paralleled MOSFETs are driven their gates should be decoupled using two individual gate resistors. For this example a gate resistor of 10Ω was used.

Depending on the layout a Schottky diode may be necessary across the gate drive to ground due to substrate current injection which can produce unpredictable behavior. The cathode should be connected to pin 14 and the anode to ground. It should be placed as physically close to the IC as possible. Substrate current injection occurs when an output pin is forced more than about 0.5V below ground.

Power and Signal Grounds

These two grounds should go to ground plane and they should be connected together with the shortest possible trace length.

V_{REF}

The VREF pin of the IC should be decoupled with a high quality ceramic capacitor. A typical value is 1µF. For higher power levels (P_{OUT} > 500W) additional capacitance may be required for proper operation.

Overvoltage Protection

This protects against accidental increases of the output voltage. This could occur because of the low bandwidth of the voltage control loop under situations such as the sudden removal of the output load. As soon as a voltage higher than the set limit is detected the IC stops sending

pulses to the MOSFET until the voltage has dropped to safe limits. In a boost regulator, if the voltage loop ceases to operate, the only way to limit the output voltage from rising to destructive levels is the overvoltage protection circuit, or an external crowbar circuit.

Equation 24 is used to set the activation limit of the OVP circuit. From Figure 10, assuming the value of R20 = 825kΩ, R19 can be found as follows

$$R19 = \frac{5 \times \left(825 \times 10^3\right)}{400 - 5} = 10.2k\Omega$$

V_{CC}

This is the supply pin of the IC. Normally a quality ceramic capacitor should be connected to this pin as close as possible to the body of the IC for effective decoupling. For low power applications (< 500W) 1µF may be sufficient, but for higher power applications experience shows that two individual capacitors could be necessary.

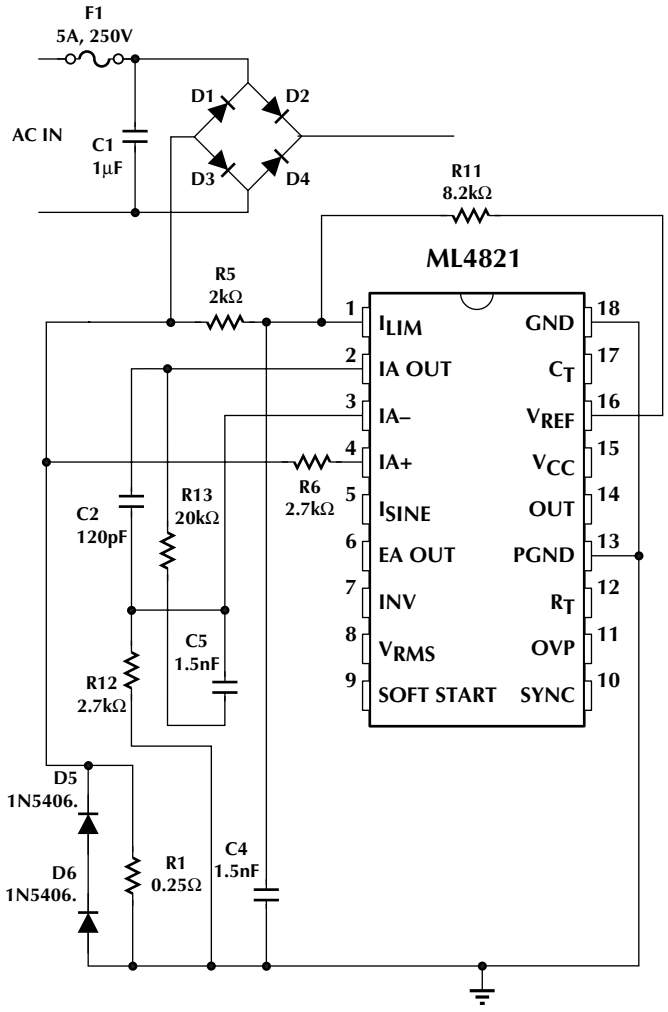

Figure 11. Current Limit and Current Sense Circuit Connections

In order to facilitate off-line start-up the IC has a large Under Voltage Lockout hysteresis. For bootstrapped operation a reservoir capacitor (C14) is charged with a small current through R10, which is connected to the input high voltage line. When the voltage on this capacitor reaches 16V the IC "wakes-up". A winding on L1 (see Figure 10) "steals" part of the energy to supply the current requirements of the IC. This way the circuit continues to operate.

The time that it takes initially for the voltage to reach 16V, and therefore for the circuit to start, is a function of the resistor R10. This is a power resistor, and for as long as power is applied it wastes power, usually about 2W.

The value of C14 is being determined by the current requirements of the circuit. C14 has to be sufficiently large for the circuit to bootstrap. However, it should not be too large because then it will take a long time to charge to 16V and turn on the IC.

Current Limit

There is a need for current limiting in the PFC, as in every switching regulator. Figure 11 illustrates its operation.

The current limit point is set by R11 and R5. The value of R5 can be selected first. Then the value of R11 is calculated using the following equation. In this case R5 = 2.0kΩ. Assuming a current limit voltage of 1.2V across the sense resistor

$$R11 = \frac{V_{REF}}{V_S} R5 = \frac{V_{REF}}{I_{IN} R1} R5 \qquad (28)$$

where:

I_{IN} = current at which limiting action should start.

R1 = sense resistor.

$$R11 = \frac{5}{1.2} 2k\Omega = 8.2k\Omega$$

For proper operation the sense voltage across R1 that triggers the current limiting action should be greater than the sense voltage produced at low line and full load. In this case current limiting action starts when the sense voltage is 1.2V. Therefore, at full load and at low line the sense voltage should be less than 1.2V. A 15% lower voltage corresponds to 1.0V.

Current Sense Circuit

Pins 3 and 4 are used to sense the return current of the power circuit. The average value of this current is forced to follow the sine wave shape under the ML4821's control. Pin 4 is at the same time connected to the output of the gain modulator. The maximum value of the gain modulator output current was set to be 400µA by timing resistor R21.

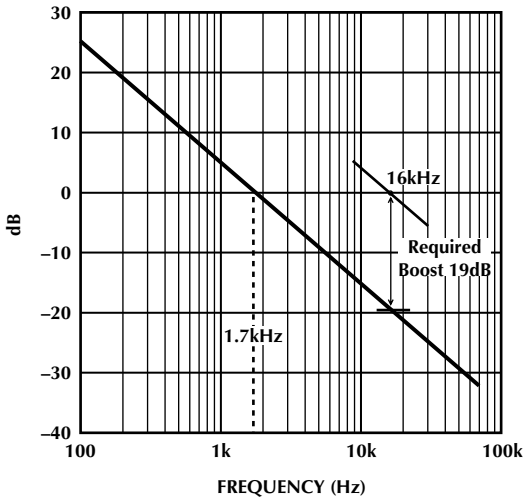

Figure 12. Open Loop Response of the Power Stage, and Required Boost for the 16kHz Loop Crossover

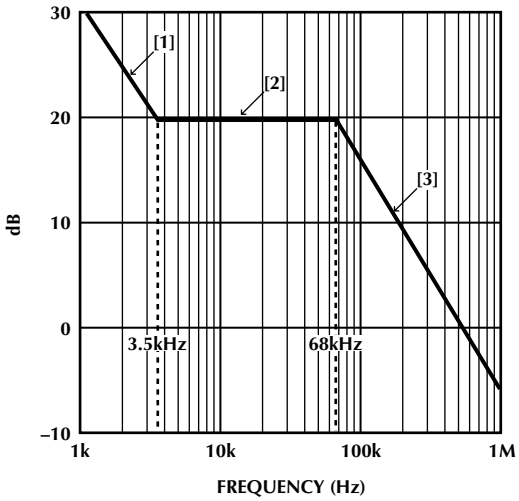

Figure 13. Desired Current Error Amplifier Response

In the current limit section it was noted that at maximum power and low line the sense voltage should be 1.0V. Therefore, R6 should be chosen such that it will produce 1.0V at 400µA.

$$R6 = \frac{1V}{400\mu A} \cong 2.7k\Omega$$

The expected maximum peak current was calculated at 4.0A. Using this value R1 can now be calculated

$$R1 = \frac{1V}{4A} \cong .25\Omega$$

The value of R12, which is a feedback resistor for the current amplifier, is set to be equal to R6. This will cancel out the input bias current of the current amplifier. So R12 = 2.7kΩ.

Design of the Current Loop Amplifier

The design of the current loop is one of the most critical tasks in the overall design. It is necessary to have knowledge of the open loop response of the power stage. Equation 12 gives this response which is plotted in Figure 12. The required gain boost for unity gain crossover at 16KHz, as set by equation 12, can be calculated by using equation 11.

$$\frac{380 \times 0.24}{2\pi \times 5.5 \times 16kHz \times 1.5mH} = 0.11 \text{ or } -19dB$$

An appropriate current amplifier response that will accomplish this is shown in Figure 13. The equations that give the asymptotic gain response in each one of the three regions are given below.

[1] $$|G|_{dB} = 20\log\frac{1}{2\pi f \times R12 \times C5} \quad (29)$$

[2] $$|G|_{dB} = 20\log\frac{R13}{R12} \quad (30)$$

[3] $$|G|_{dB} = 20\log\frac{1}{2\pi f \times R12 \times C2} \quad (31)$$

Calculate the feedback component values to complete the design of the current control loop. Using equation 30 the value of R13 is found as

$$20\log\frac{R13}{R12} = 19dB \Rightarrow R13 \cong 20k\Omega$$

$$C5 = \frac{1}{2\pi f \times R12 \times 10^{\frac{19}{20}}} \Rightarrow C5 \cong 2.3nF$$

where:

f = 3.5kHz

R12 = 2.7kΩ

Gain boost = 19dB

$$C2 = \frac{1}{2\pi f \times R12 \times 10^{\frac{19}{20}}} \Rightarrow C2 \cong 120pF$$

where:

f = 68kHz

With the values of the feedback components calculated the overall closed loop response of the inner current loop can be plotted. Logarithmic slopes and gain values just need to be added to get the overall response. The result is shown in Figure 14.

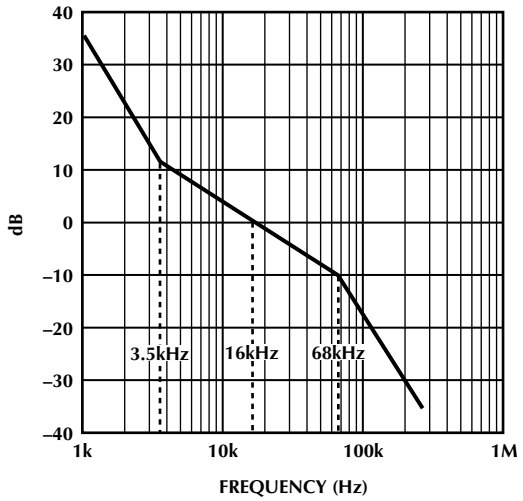

Figure 14. Overall Closed Current Loop Response

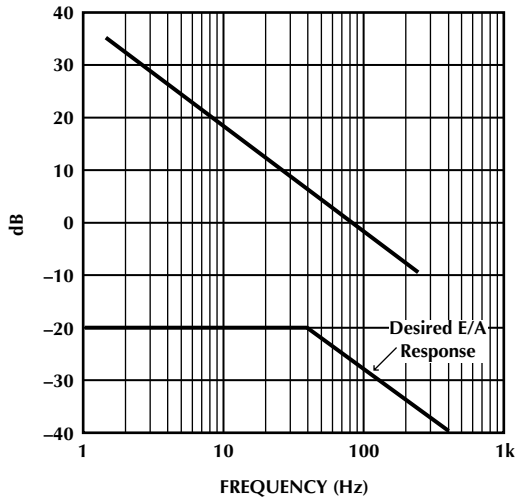

Figure 15. Open Loop and Desired Error Amplifier Response

Calculation of R7, the I_{SINE} Resistor

Previously the maximum voltage of the error amplifier has been assumed at 4.4V. The minimum voltage under normal operating conditions is about 0.8V. That necessitates a change in the output voltage of the error amplifier of 3.6V from no load to full load. Note that due to feedforward compensation the output of the error amplifier will not change for line variations. It is important also to note that the amplifier output is capable of going to 7.5V.

Equation 20 can be solved for R7

$$R7 = \frac{\Delta V_{EAOUT} \times K \times V_{RMS}^2 \times R6}{R1 \times P_{IN}} \qquad (32)$$

Substituting the known values into the above we get

$$R7 = \frac{3.6 \times 0.23 \times 120^2 \times 2200}{210 \times 0.24} = 535k\Omega$$

The nearest standard value for R7 is 560kΩ. With this resistor value the I_{SINE} current should be calculated to check the input current range corresponding to the line input voltage range. The gain modulator requires that the I_{SINE} current be less than 500µA as suggested in Figure 8 of the data sheet.

Design of the Voltage Loop Amplifier

Equation 21 gives the magnitude of the open loop gain. The response has a -20dB/decade slope with constant 90 degree phase lag. To proceed with the design of the error amplifier feedback components pick the unity gain crossover frequency. In this circuit the chosen 0dB crossover frequency is 10Hz.

The frequency where the open loop response crosses over the 0dB (unity gain) line can be found by solving equation 21 for f. Figure 15 shows the open loop along with the desired amplifier responses

$$f = \frac{P_{IN}}{2\pi C_{OUT} \times V_{OUTDC} \times \Delta V_{EAOUT}} \qquad (33)$$

$$f = \frac{210}{2\pi \times 270 \times 10^{-6} \times 380 \times 3.7} = 88Hz$$

For unity gain crossover at 10Hz the amplifier needs to have an attenuation of 19dB at 10Hz.

$$20\log\frac{R14}{R18} = -19dB \Rightarrow R14 \cong 92k\Omega$$

Then calculate the value of C6. Look up the asymptotic break point of the response curve, which in this case is 40Hz.

$$C6 = \frac{1}{2\pi f R14} = \frac{1}{2\pi \times 40 \times 92k} = 43nF$$

Figure 16 shows the overall closed voltage loop response.

Voltage Sense Resistor Calculation

R18 was set to 825kΩ. R17 can be calculated using equation 22.

$$R17 = \frac{5 \times 825k\Omega \times 92k\Omega}{92k\Omega(370-5) - 0.6 \times 825k\Omega}$$

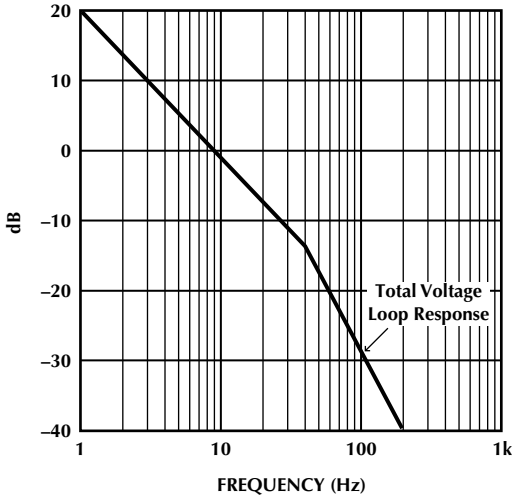

Figure 16. Total Voltage Closed Loop Response

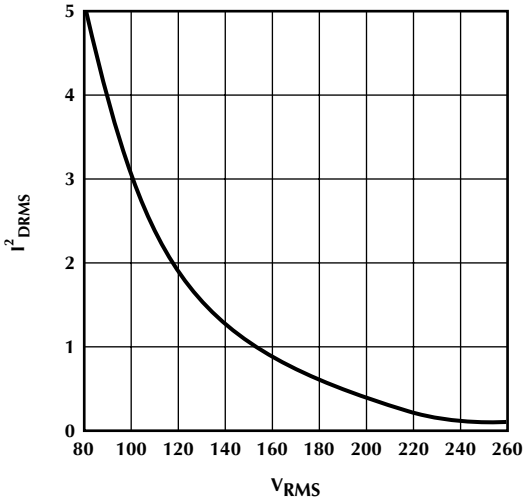

Figure 17. Square RMS Drain Current vs Input RMS Voltage

Losses In The Power MOSFET Q1

There are three kind of losses in the power MOSFET:

1. Conduction Losses due to the conduction of the drain current.
2. Capacitive Losses due to the charge and discharge of the total drain source capacitance. This is a switching loss.
3. Turn-On and Turn-Off Losses. These are also switching losses.

The conduction losses can be calculated by using equation 34, which gives the RMS value of the drain current that can be used to calculate the conduction losses. It is a function of the input power and input and output voltages.

$$I_{DRMS} = \frac{2P_{IN}}{V_{INRMS}} \sqrt{\frac{1}{4} - \frac{2\sqrt{2}V_{INRMS}}{3\pi V_{OUT}}} \qquad (34)$$

This assumes that the ripple to average current ratio is very small, which is normally true for this kind of PFC. It happens in the low input voltage range. In reality the nonzero ripple will increase the value of the calculated RMS current by a small amount.

Figure 17 gives the value of the square of the RMS drain current with respect to the input RMS voltage. This graph can be used to calculate the power loss due to conduction in the MOSFET. This is simply

$$P_{CMOSFET} = I^2_{DRMS} \times R_{D-SON} \qquad (35)$$

In the design example the minimum line was 85VAC. Using Figure 18 that corresponds to a value of 4.5W. Using an IRF840 type MOSFET and assuming that its ON resistance at the operating temperature will be 50% higher than its 25°C resistance, the conduction power loss will be 5.4W. At 120VAC the power loss will be 2.2W, and at 220VAC will be 0.34W. It is quite difficult to have both an optimum circuit and at the same time wide input voltage range. For specific applications where the input voltage range is narrow it is more advantageous to have the output voltage closer to the maximum peak of the input voltage.

Here is an example with respect to the last statement made in the preceding paragraph. Assume that the power level is still the same, but that the operating voltage range is 85VAC to 135VAC and that the output voltage is 200VDC. With these operating parameters equation 35 yields a value of 2.99, which corresponds to a power loss of 3.6W. Compare this to 5.4W in the preceding example.

Normally efficiency measurements are made at nominal operating voltages, *i.e.*, 120VAC. However, the PFC should be able to function without failure at low line conditions. That necessitates careful selection of components and thermal design for good reliability.

Capacitive losses in the MOSFET are due to discharge of the total drain source capacitance. We use the term total because the drain gate capacitance contributes to this loss, too. The losses can be calculated using equation 36.

$$P_{CAP(D-S)} = \frac{1}{2} C_{D-S} \times V^2_{OUT} \times f_S \qquad (36)$$

If we assume a total capacitance of 350pF then equation 36 yields 2.5W.

The calculation of switching losses are a little more difficult since they are a function of many things, such as gate drive conditions and physical layout. In any case equation 37 can be used to give some indication of these losses

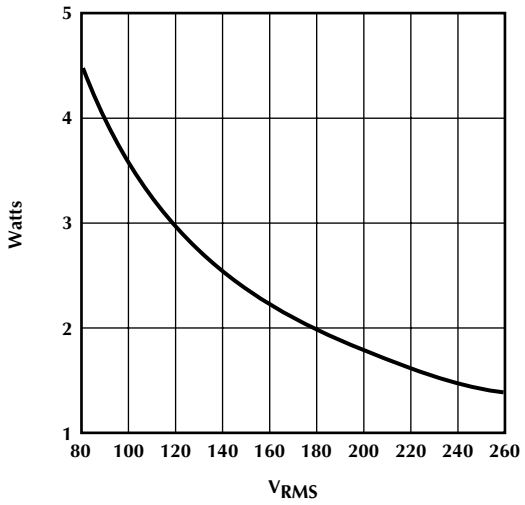

Figure 18. Switching Power Loss for a 200W PFC at 100kHz vs the Input Voltage

$$P_{SWITCHING} = \frac{2\sqrt{2}V_{OUT} \times f_S \times P_{IN} \times t_{TR}}{\pi V_{INRMS}} \qquad (37)$$

where

t_{TR} = transition time

f_S = switching frequency (100kHz in this case)

Assuming waveform symmetry during both turn-on and turn-off transitions, and ignoring possible secondary effects, we can use equation 37 to calculate the switching losses. Our example was designed at 120VAC and 210W input with a reasonable value for the transition time of 50ns. The resulting losses are approximately 3W.

As a final step add up all the losses in the MOSFET for 120VAC. The resulting total loss is 7.7W. If this yields an unacceptable efficiency an optimized MOSFET switch should be used. Loss calculations can be made using equations 35, 36 and 37.

EVALUATING A PFC CIRCUIT

This part of the application note will give practical information that may be useful when trying to get the breadboard to meet the required specifications. It will show that measuring power factor, harmonic current content, and efficiency may impose new challenges to even experienced power supply design engineers. Also it will contain some performance data that may serve as a reference point.

Waveforms

Operating waveforms are shown in the following figures. They are taken with output at 200W and input at 120VAC. Figure 19 shows the power factor corrected input current waveform. The upper waveform is current at 1A per division. The voltage and current waveforms are in phase and identical. Figure 20 shows the inductor waveform. The shaded portion of the upper waveform indicates the ripple current riding on top of a rectified sinusoidal current. The lower waveform is an expanded view of the upper waveform. Figure 21 shows the current limit waveform on pin 1. As the input current increases the valleys of this waveform approach zero volts. However, because the gain modulator current is limited to 400µA, the current waveform will sag before the current reaches the current limit level. Current limit level is reached during a transient condition when the inductor current increases rapidly before the voltage loop can compensate for it. Figure 22 shows the output of the current amplifier (pin 4). It sets up the trip points of the PWM comparator.

REMINDER: The OVP pin requires at least 0.7V for the chip to begin operation.

Layout

Board layout is critical in this application as it is in any power control circuits. Pay close attention to the high current circulating paths. The control circuitry and its associated ground plane should be kept away from the high current power paths as much as possible. Current should be steered away from the high impedance nodes, such as the input to both error amplifiers, as well as to both current limit and OVP comparators. Also, magnetic fields generated by the magnetics components, as well the switching power components, can inject noise into the high impedance nodes such as the current limit comparator. The heat sink should either be grounded or AC coupled to ground by a high frequency ceramic capacitor, and kept as far away from the IC as possible.

Power Factor

Input power factor, harmonic current content, and waveshape are all used when describing the performance of a power factor circuit. It is important to keep in mind that regulatory specifications such as the IEC1000-2-3 for Europe will require that just the harmonic current levels meet certain limits. The proposal currently sets these limits — for Class D — as a function of power level up to 600W. Above 600W the limits are absolute. Thus even a low power factor number at high input line voltage can easily meet the limits since the input current level is proportionally low. Nevertheless, power factor is a good parameter for measuring the capabilities of a power factor circuit.

Measuring power factor requires a very reliable power meter that accurately measures both apparent power (product of RMS voltage and RMS current) and true average power. Some of the older model meters measure power factor by determining the phase angle between current and voltage waveforms.

True average power for distorted AC waveforms can only be determined when the current and voltage are

simultaneously sampled, and then multiplied and integrated. There are several meters on the market that are possible candidates for this purpose. The Voltech PM1000 measures true power by sampling the waveform and analyzing the analog signal using digital methods, and is the recommended instrument. It uses DSP to filter, multiply, and integrate both voltage and current simultaneously.

Note: A study was done comparing the results of power factor measurements between the Voltech and that of another well known meter manufacturer (which performs the multiplication and integration of the power signal via analog methods). Both meters gave nearly identical measurements when evaluated against a calibrated standard reference unit. However, when the units were set up in the lab to measure power factor of an actual switching power circuit, only the Voltech gave the expected measurement readings. For whatever reason the analog meter gave grossly false readings. Noise in the switching circuit is the prime suspect. This does not suggest that meters with analog circuits cannot be designed to reject noise and work effectively.

Harmonic current

Harmonic current content can be measured using the Voltech PM1000. It gives a percentage of the fundamental up to the 13th harmonic. Results of this method were compared to that of the HP spectrum analyzer 3585A, and they were quite close. The Voltech PM3000, which is a three phase power meter, measures harmonic currents to the 99th. Results show that harmonic current level beyond the 13th harmonic remain low throughout the spectrum. The proposed IEC1000-2-3 specification is expected to require harmonic current content conformity to the 40th.

Efficiency

Almost all of the losses come from the three power devices. The inductor, MOSFET, and diode were selected to meet performance specifications at relatively low cost. An IRF840 MOSFET seemed to provide the best performance at these power levels. A larger MOSFET (APT5025) did improve efficiency at low input voltage; however, its larger output capacitance increased switching losses significantly at 100KHz. A very common 8A ultra-fast rectifier (MUR850) was used for the output diode. This oversizing was done because larger diodes have lower reverse recovery times for a given current level. New diodes have since been introduced with even lower reverse recovery times. A low cost ferrite EC core was used with AWG21 wire. There was very little temperature rise in the magnetic material. However, the wire heated up at low input voltage where RMS current is significant. A low cost powdered iron core with AWG20 magnet wire was also tried, but efficiency decreased about one percent.

Efficiency measurement requires accurate measurement of the output average power as well as the input average power. Because the output voltage and current are DC, one might just measure the two readings using a typical lab DMM. However, this approach did not match the measurement results of the average power reading of the Voltech power meter. The output power measurement was off by almost 6%. The benchtop DMM used was Fluke's 8050A. To get truly accurate efficiency measurements,

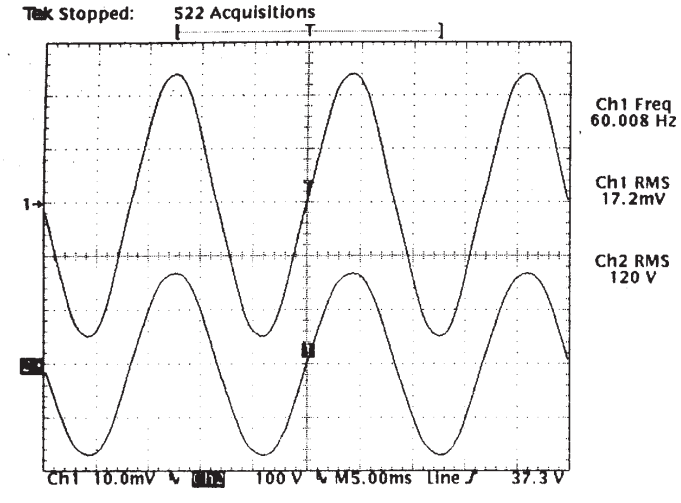

Figure 19. Input Current

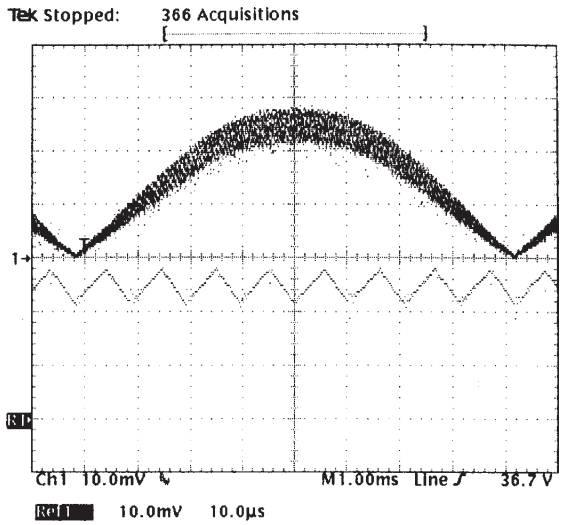

Figure 20. Inductor Current (Magnified)

the same power meter should be used to measure both the output power and the input power.

Efficiency measurements for this application note were done on a Voltech PM3000 three phase power meter. This meter allows the connection of both the input power and the output power into one metering unit. Accuracy, however, does not come easily even with this approach. The output power reading randomly varied up to 3% under steady state conditions.

Two different meters from the same manufacturer gave current readings that differed by two to three percent. This might indicate that two meters from the same manufacturer might not be guaranteed to be as accurate as one may require.

Performance Data

Table 1 shows the results obtained from an application circuit. Pertinent power and power factor measurements were taken and the harmonic current content as a percentage of the fundamental. It is intended to be a typical reference point in which to judge new designs. It is likely that the performance can be improved and optimized.

The following are specifications for two inductors that may be considered for the 200W PFC converter.

Magnetics, Inc.	Micrometals
(412) 282-8282	(714) 630-7420
OP44317 (Ferrite, EC)	T184-40 (Powdered Iron, Toroid)
N_P = 118 turns, AWG21	N_P = 102 turns, AWG20
N_s = 5 turns, AWG30	N_s = 3 turns, AWG30
gap = 1.7mm	

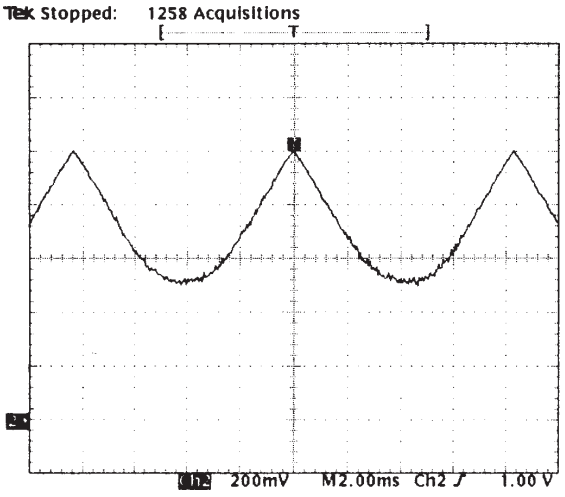

Figure 21. Current Limit Comparator

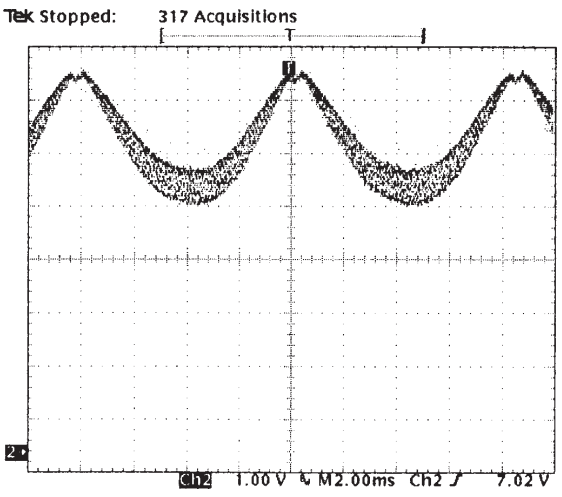

Figure 22. Current Amp Output

Table 1. Performance Data

	PO = 50W					PO = 100W					PO = 150W					PO = 200W				
	V_O	P_O	P_I	PF	n	V_O	P_O	P_I	PF	n	V_O	P_O	P_I	PF	n	V_O	P_O	P_I	PF	n
	$I_{FUNDAMENTAL}$					$I_{FUNDAMENTAL}$					$I_{FUNDAMENTAL}$					$I_{FUNDAMENTAL}$				
HARMONICS	3rd	5th	7th	9th	11th	3rd	5th	7th	9th	11th	3rd	5th	7th	9th	11th	3rd	5th	7th	9th	11th
	13th	15th	17th	19th	21st	13th	15th	17th	19th	21st	13th	15th	17th	19th	21st	13th	15th	17th	19th	21st
	395	54	62	0.99	0.87	387	105	117	0.99	0.90	379	153	166	0.99	0.92	371	197	218	0.99	0.90
V_{IN} = 90VAC	I_{FUND} = 0.67A					I_{FUND} = 1.3A					I_{FUND} = 1.8A					I_{FUND} = 2.4A				
Harmonic Distortion	3.5	1.7	0.04	0.32	0.30	3.1	1.6	0.02	0.23	0.21	2.9	1.5	0.05	0.22	0.24	2.4	1.6	0.20	0.27	0.37
	0.06	0.05	0.05	0.01	0.11	0.04	0.03	0.06	0.01	0.01	0.09	0.18	0.18	0.12	0.13	0.24	0.24	0.24	0.15	0.15
	393	52	61	0.99	0.85	386	105	115	0.99	0.91	378	150	161	0.99	0.94	369	194	212	0.99	0.91
V_{IN} = 120VAC	I_{FUND} = 0.51A					I_{FUND} = 0.96A					I_{FUND} = 1.3A					I_{FUND} = 1.8A				
Harmonic Distortion	3.7	2.2	0.12	0.46	0.37	3.2	1.9	0.05	0.29	0.25	3.1	1.9	0.01	0.21	0.26	2.9	1.9	0.09	0.15	0.12
	0.14	0.05	0.08	0.05	0.23	0.10	0.07	0.11	0.05	0.03	0.07	0.05	0.09	0.07	0.03	0.09	0.03	0.03	0.01	0.02
	394	52	60	0.96	0.87	385	105	114	0.99	0.92	378	151	163	0.99	0.93	369	190	207	0.99	0.92
V_{IN} = 180VAC	I_{FUND} = 0.34A					I_{FUND} = 0.64A					I_{FUND} = 0.87A					I_{FUND} = 1.2A				
Harmonic Distortion	4.6	2.3	1.6	2.1	2.7	4.7	2.2	0.06	0.51	0.49	4.5	2.0	0.03	0.39	0.34	4.4	1.7	0.08	0.31	0.28
	1.9	1.0	0.87	0.95	0.66	0.18	0.17	0.12	0.12	0.08	0.11	0.12	0.12	0.10	0.04	0.11	0.09	0.09	0.04	0.02
	393	53	61	0.93	0.87	383	102	114	0.97	0.90	374	150	162	0.99	0.93	365	192	207	0.99	0.93
V_{IN} = 220VAC	I_{FUND} = 0.28A					I_{FUND} = 0.52A					I_{FUND} = 0.71A					I_{FUND} = 0.95A				
Harmonic Distortion	5.4	2.4	0.21	1.0	1.0	5.3	2.8	0.02	0.77	0.51	4.9	2.3	0.08	0.56	0.35	4.7	2.3	0.06	0.47	0.33
	1.8	2.8	2.7	2.0	1.0	0.41	0.47	0.38	0.25	0.15	0.21	0.25	0.23	0.17	0.06	0.15	0.21	0.18	0.18	0.04
	394	53	62	0.87	0.85	387	103	115	0.95	0.90	379	153	164	0.97	0.93	372	195	208	0.98	0.94
V_{IN} = 260VAC	I_{FUND} = 0.24A					I_{FUND} = 0.44A					I_{FUND} = 0.61A					I_{FUND} = 0.82A				
Harmonic Distortion	6.2	4.5	0.59	0.76	1.3	5.3	3.4	0.94	0.47	1.7	4.9	2.8	0.27	0.63	0.58	4.7	2.4	0.16	0.51	0.34
	0.96	1.1	0.36	1.5	2.3	1.4	0.8	1.0	1.4	1.0	0.26	0.35	0.53	0.24	0.10	0.24	0.26	0.38	0.14	0.01