Mihail Popov

Research Scientist

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I am interested in high performance computing and machine learning.

Experience

- 2021 Research Scientist, Inria STORM, Bordeaux, France.
 - Exploring ML methods for performance optimization.
- 2020 Senior Software Researcher, Huawei 2012 Research Labs, Edinburgh, UK.
 - Developed compiler transformations for ML.
- 2018 2019 Postdoc Researcher, UART Architecture Group Uppsala University, Uppsala, Sweden.
 - Designed ML models to optimize/explore hardware parameters and NUMA effects (ICS20).
 - Optimized performance on NUMA systems by exploring a larger search space of thread and page mappings. The additional exploration cost is amortized with sampled execution (ICS19).
 - 2017 Postdoc Researcher, University of Versailles Saint-Quentin (UVSQ), Versailles, France.
 - Characterized HPC applications performance over the last decade (**Proceedings of the IEEE**).
 - $\circ~$ Improved autotuning of compiler optimization with clustering (CCPE).
- 2013 2016 Ph.D. Student, UVSQ/Paris-Saclay, Versailles, France.

Title: Automatic Decomposition of Parallel Programs for Optimization and Performance Prediction Ph.D. advisors: Assistant Prof. Pablo de Oliveira Castro and Full Prof. William Jalby

- Decomposed applications into codelets with CERE. Codelets map loops or OpenMP regions and are replayed as standalone programs. (IPDPS, TACO).
- Proposed a piecewise holistic approach to tune compiler optimizations and thread configurations through codelets. Codelet autotuning achieves better speedups at lower tuning cost (Euro-Par).
- 2016 Intern, UVSQ/Intel Software Tools, Champaign, USA.
 - $\circ~$ Worked on profiling methods and simulation with codelets.
- 2013 Intern, Exascale Computing Research (ECR), Versailles, France.
 - Participated in the elaboration of a method to reduce the benchmarking cost. I clustered codes with similar computation patterns and which are sensitive to the same architectural changes (CGO).
- 2012 Intern, ECR, Versailles, France.
 - Developed a method to quantify a distance between applications using compression tools.

Prizes and Awards

2016 Euro-Par publication in the best paper issue, 3% acceptance rate, 5 our of 176.

— Computing Skills

General Linux, Performance Characterization

Parallelism OpenMP (threads and tasks), Processes, Cuda, Vectorization

ML Clustering, ANN, Data Analysis, Automatic Differentiation

Compilation LLVM

 ${\bf Languages} \ \ {\bf Python}, \ {\bf C/C++}, \ {\bf R}, \ {\bf Fortran}, \ {\bf Latex}$

Education

- 2010 2013 Master Degree in Engineering and Computer Science, *ISTY*, France. European master degree of computer science.
- 2012 2013 Master Degree in High Performance Computing, UVSQ/Ecole Centrale Paris.

 Master degree obtained in parallel of the last year of the master degree in engineering.

Supervision

2015-2019 Main advisor.

- Ph.D. internship on prefetchers and NUMA systems.
- Master thesis on parallel application optimization for NUMA systems.
- Bachelor internship on locks and LLVM code extraction for parallel applications.
- Two bachelor internships on iterative compilation.
- 2019 Main teacher, 16 hours, Uppsala master course, Low Level Parallel Programming.

 Presented different parallelization strategies including OpenMP (threads and tasks), SIMD vectorization, C++ threads, and CUDA. 4/5 rating by 20 students.
- 2015 Main teacher, 20 hours, ISTY master course, Operating Systems Project.

 Designed a project to model the Linux file system. Focused on low level structures (inodes, blocks).
- 2014 2015 **Teaching Assistant**, **73 hours**, ISTY/UVSQ, Operating Systems/Computer architecture.
 - o Introduction to Linux: processes and internal structures. Received an excellent feedback.
 - Introduction to computer architecture with an emphasize on floating point arithmetic.

Publications

I Sánchez, D Black-Schaffer, M Moretó, M Casas, A. Stupnikova, and **M. Popov**, "Modeling and optimizing numa effects and prefetching with machine learning," in *Proceedings of the ACM International Conference on Supercomputing*, **ICS**, **2020. 20-minute Video**.

M. Popov, A. Jimborean, and D. Black-Schaffer, "Efficient thread/page/parallelism autotuning for numa systems," in *Proceedings of the ACM International Conference on Supercomputing*, ICS., 2019. 5-minute Video.

W. Jalby, D. Kuck, A. D. Malony, M. Masella, A. Mazouz, and M. Popov, "The long and winding road toward efficient high-performance computing," in *Proceedings of the IEEE*, 2018.

- M. Popov, C. Akel, Y. Chatelain, W. Jalby, and P. de Oliveira Castro, "Piecewise holistic autotuning of parallel programs with cere," in *Wiley Online Library Concurrency and Computation: Practice and Experience*, CCPE, 2017.
- M. Popov, C. Akel, W. Jalby, and P. de Oliveira Castro, "Piecewise holistic autotuning of compiler and runtime parameters," in *European Conference on Parallel Processing*, **Euro-Par**, **2016** (included in the Best Paper Issue).
- M. Popov, C. Akel, F. Conti, W. Jalby, and P. de Oliveira Castro, "Pcere: Fine-grained parallel benchmark decomposition for scalability prediction," in *IEEE International Parallel and Distributed Processing Symposium*, IPDPS, 2015.
- P. D. O. Castro, C. Akel, E. Petit, **M. Popov**, and W. Jalby, "Cere: Llvm-based codelet extractor and replayer for piecewise benchmarking and optimization," in *ACM Transactions on Architecture and Code Optimization*, **TACO**, **2015**.
- P. de Oliveira Castro, Y. Kashnikov, C. Akel, M. Popov, and W. Jalby, "Fine-grained benchmark subsetting for system selection," in *Proceedings of Annual IEEE/ACM International Symposium on Code Generation and Optimization*, CGO, 2014.

Volunteer Experience

- 2021 Program Committee/Reviewer.
 - ICCS.
 - $\circ\,$ ISC High Performance
 - JPDC.
 - PDP'29.
- 2020 Program Committee.
 - HPCS'18 CADO.
 - o PDP'28.

- 2020 Reviewer.
 - Journal of Systems Architecture.
- 2019 Web Chair.
 - o ACM CC'29.
- 2018 Reviewer.
 - Euro-Par'24.
 - o CC'28.
 - IEEE TC.