# ECEN 351 – Lab10: Standard Cells (50 points)

**Purposes:**

1. Learn how do design a large digital circuit using Standard Cells.

2. Learn how to work as a team by instantiating Cells laid out by others.

3. Get a feel for the complexity of a larger digital project.

**Procedure:**

1. Review the circuits necessary to design a 1-bit register file with 3 address bits (8 memory locations). This design can be broken down into 3 main functional blocks:

* Address Decoder Block
* The Register Block
* The Output Multiplexer

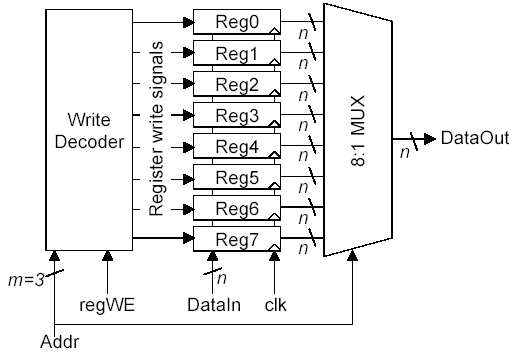
Each student will implement the schematic and layout of one of these three functional blocks and rely on the work of two other individuals in order to complete the entire project.

2. Collaborate with others on the physical and electrical requirements of this design in order to ensure that each completed layout will interface properly.

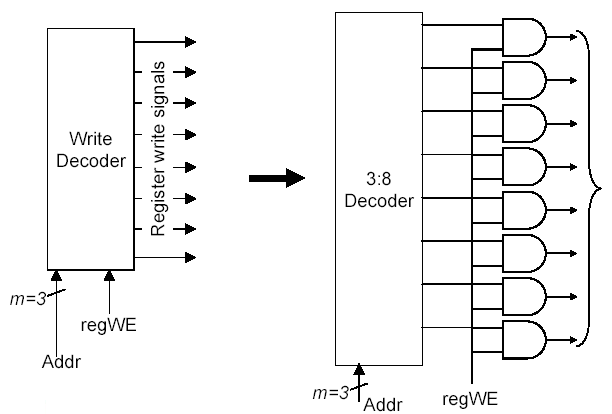
3. Design and Simulate the schematic of the circuit you have selected.

4. Layout your selected circuit according to the requirements of your cooperative group.

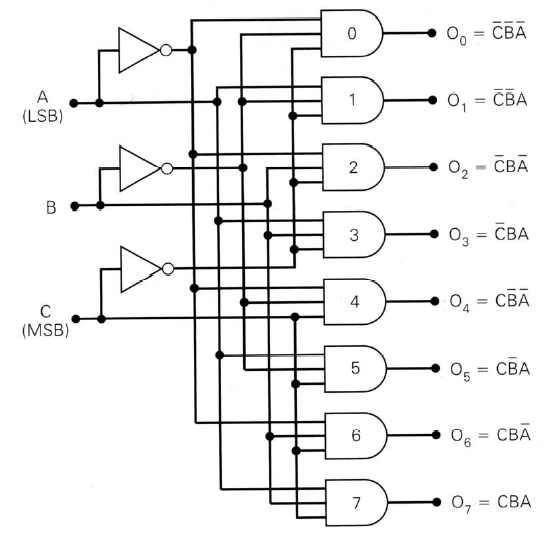
5. Combine your design with the other two designs in your cooperative group.

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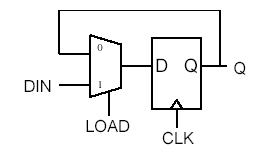
**Figure 1 – Register File**

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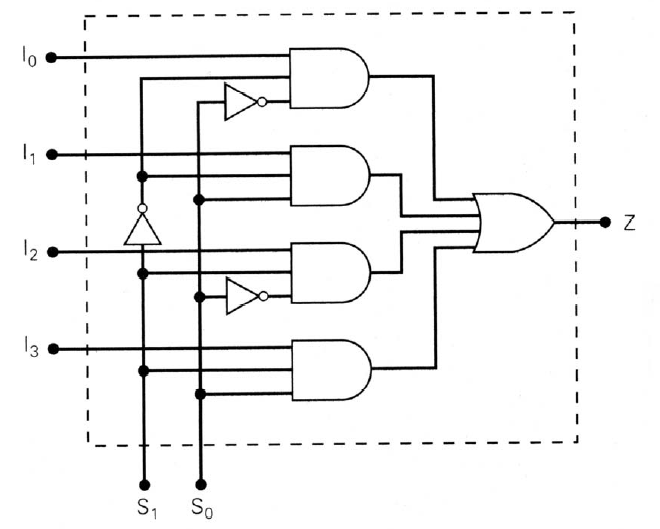
**Figure 2 – Write Decoder**

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**Figure 3 – 3 to 8 Decoder**

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**Figure 4 – Loadable Register**

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**Figure 5 – 4 input MUX**

**Verification:**

Use LTSpice to verify your design through simulation. The appendix, A.5 of the textbook is a good resource for obtaining this information. In general, use the “PULSE” voltage source for periodic signals and the “PWL” voltage source for non-periodic signals.

The syntax for “PULSE” is found in A.5.3 of the textbook. It will look like this:

Vclk clk 0 PULSE 0 3 10n 100p 100p 9.9n 20n

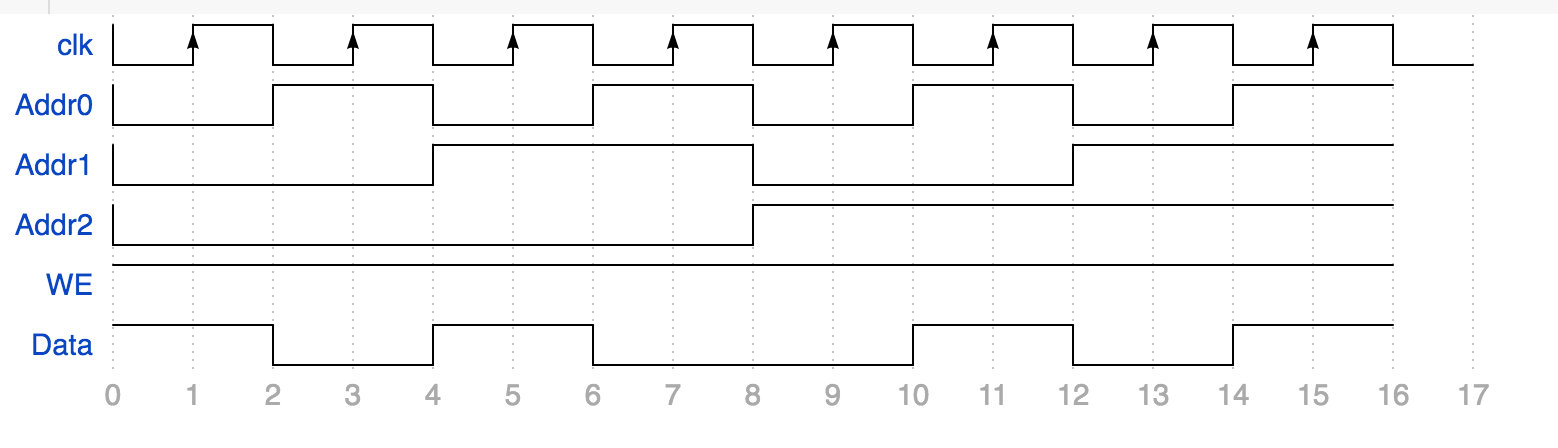
Where “Vclk” is the name of the voltage source, “clk 0” are the names of the nets to which you will connect this voltage source, “PULSE” is a SPICE directive indicating that you want a periodic pulse, “0 3” are the respective low and high voltage levels of your pulse, “100p 100p” represents the rise and fall times of the pulse, “9.9n” is the pulse width, and 20n is the period of the signal. Remember that period is 1/frequency.

The syntax for “PWL” is found in Ch. 8 of the textbook. It will look like this:

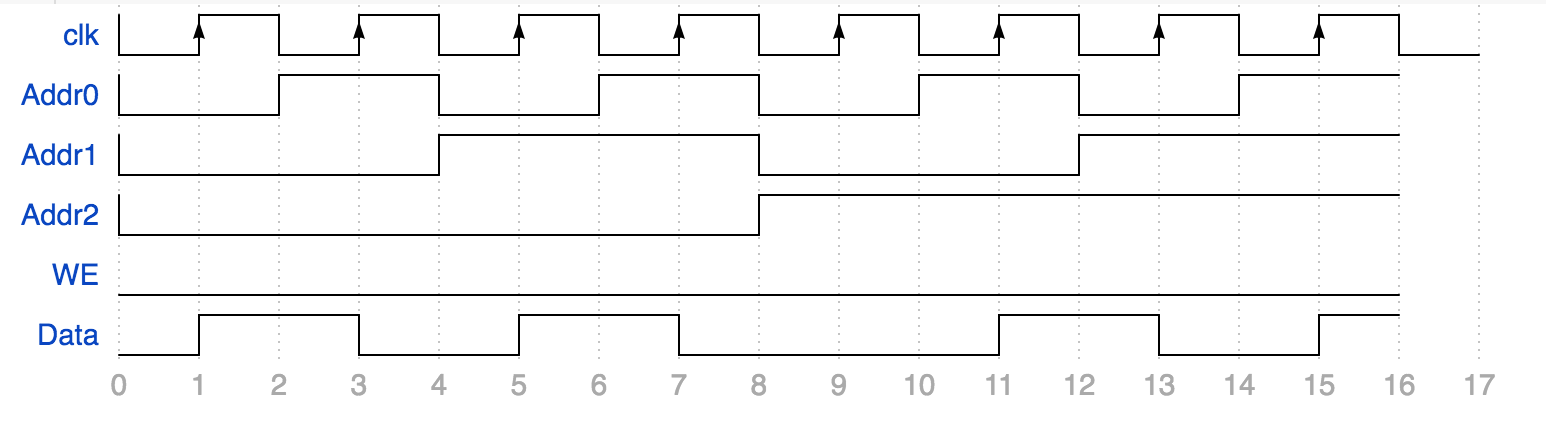
Vdata din 0 PWL 0 0 10n 0 11n 3 …

Where “Vdata” is the name of the voltage source, “din 0” are the names of the nets to which you wish to connect this voltage source, “PWL” is a SPICE directive indicating that you want a piece-wise-linear signal, and the numbers after that are “time and voltage” pairs. The first “0 0” in this example means that at time 0, you want a voltage of 0V, at 10ns, you still want a voltage of 0V, and at 11ns, you want the voltage to change to 3V. You can have as many “time and

voltage” pairs as you wish, but if you need to overflow, to the next line, use “+” to indicate continuation from last line.



**Figure 6 – Example Write Data**

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**Figure 7 – Example Read Data**

**.tran 200n**

**vclk clk 0 pulse 0 3 10n 100p 100p 9.9n 20n**

**vaddr0 addr0 0 pulse 0 3 20n 100p 100p 19.9n 40n**

**vaddr1 addr1 0 pulse 0 3 40n 100p 100p 39.9n 80n**

**vaddr2 addr2 0 pulse 0 3 80n 100p 100p 79.9n 160n**

**Vwe we 0 3**

**Vdata data 0 pwl 0n 3v 20n 3v 20.1n 0v 40n 0v 40.1n 3v 60n 3v 60.1n 0v**

**+ 100n 0v 100.1n 3v 120n 3v 120.1n 0v 140n 0v 140.1n 3v**

**Scoring:**

The grading will be weighted more heavily on your own work. Please indicate the cell you designed and implemented. 80% of the weight will be on this cell. It should be DRC clean and LVS clean.

**Submitting your report:**Submit a report for all parts of this lab. The report should be professional quality—meaning it will be neat, well organized, and use proper English. It should be complete enough that a peer could read it and understand what you did and what you learned. Your report should include the following:

1. Your simulation conditions and the key wave-forms for each simulation.

2. A discussion of the challenges added when multiple designers are involved in a single design.

3. Screen shots of the schematics and the layouts.

4. A conclusion statement wrapping up your observations of standard cells and team-based design.