Project 21: Han Carlson Adder

A Comprehensive Study of Advanced Digital Circuits

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1 Introduction

The Han-Carlson adder is a high-speed parallel-prefix adder designed to efficiently perform binary addition. It enhances the carry propagation mechanism over traditional carry-lookahead adders by using a parallel-prefix approach. This design reduces the critical path length and improves overall addition speed, making it suitable for high-performance digital systems where speed is crucial.

2 Key Concepts

- **Parallel-Prefix Addition:** The Han-Carlson adder utilizes parallel-prefix techniques to perform binary addition. This approach computes carry values in parallel, significantly speeding up the addition process compared to serial methods.
- **Generate (G) and Propagate (P) Signals:**
  - *Generate Signal (G):* Represents whether a carry will be generated at a specific bit position. It is calculated as *G[i] = A[i] & B[i]*.
  - *Propagate Signal (P):* Indicates if a carry input will propagate to the next bit position, calculated as $P[i] = A[i] \oplus B[i]$.
- **Carry Propagation:** The Han-Carlson adder improves carry propagation efficiency by computing carries in parallel, reducing the time required for carry calculation compared to traditional methods.
- **Critical Path Reduction:** The use of parallel computation in carry propagation minimizes the critical path length, resulting in faster addition operations compared to ripple-carry or basic carry-lookahead adders.
- **Scalability:** The adder's parallel-prefix architecture allows it to handle larger bit-widths efficiently, making it suitable for high-performance applications due to its better scalability.

3 Steps in Han Carlson Adder

- **Generate and Propagate Signals:**
  - For each bit i, calculate the generate (G_i) and propagate (P_i) signals:

$$G_i = A_i \wedge B_i$$

$$P_i = A_i \oplus B_i$$

- **Initial Prefix Calculation:**
  - Perform the first level of prefix operations to calculate group generate and propagate values for pairs of adjacent bits.
- **Middle Stages:**
  - Use a tree structure similar to a Kogge-Stone adder for the middle stages. This involves multiple levels of prefix operations, where each level combines the results from the previous level.
  - These stages compute intermediate carry values based on grouped generate and propagate signals.
- **Final Prefix Stage:**
  - In the final stage, perform selective prefix operations on the carry signals, similar to a Brent-Kung adder, but only for the remaining unprocessed bits. This reduces the number of operations compared to a full Kogge-Stone structure.
- **Sum Calculation:**

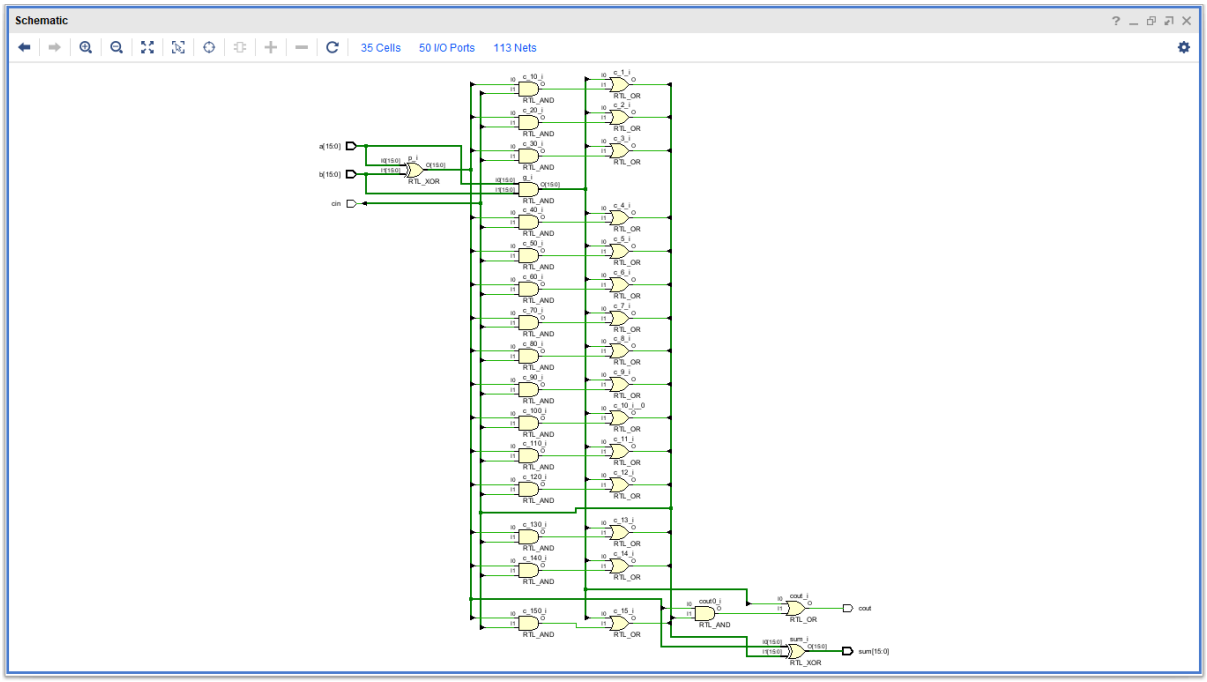

Figure 1: Schematic of Han Carlson Adder

  - Calculate the sum bits using the propagate signals and the final carry values:

$$S_i = P_i \oplus C_{i-1}$$

  - Here, C_{i-1} is the carry for the previous bit.

- **Final Carry-Out:**
  - The carry-out is derived from the final group generate signal in the last stage of the adder.

4 Why to Choose It

- **High Speed:** The Han-Carlson adder employs parallel-prefix computation, which allows for rapid carry propagation across all bit positions. This results in faster addition compared to traditional adders like ripple-carry and carry-lookahead adders.
- **Efficient Carry Propagation:** By using parallel computation for carry signals, the Han-Carlson adder significantly reduces the time required to propagate carries through the adder, improving overall performance.
- **Scalability:** Its design scales effectively to handle larger bit-widths, making it suitable for modern high-performance digital systems where speed and efficiency are critical.
- **Critical Path Reduction:** The parallel-prefix approach reduces the critical path length, which is the longest delay path in the adder. This contributes to a more efficient and faster adder compared to those with longer critical paths.
- **Improved Performance in Complex Designs:** For applications requiring high-speed arithmetic operations, such as processors and digital signal processors, the Han-Carlson adder offers significant performance improvements over simpler adder designs.

5 Synthesis

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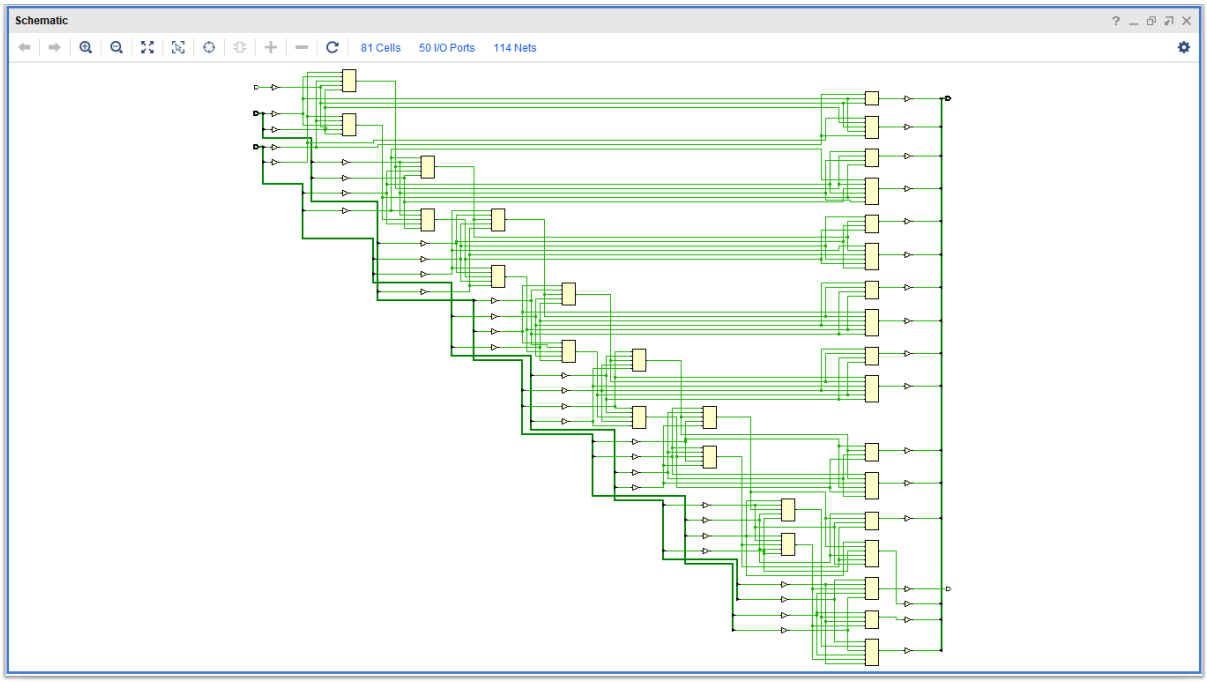

Figure 2: Synthesis of Han Carlson Adder

6 SystemVerilog Code

Listing 1: Han Carlson Adder RTL Code

```
module han_carlson_adder (
    input  logic [15:0] a,      // 16-bit input A
    input  logic [15:0] b,      // 16-bit input B
    input  logic        cin,    // Carry-in
    output logic [15:0] sum,    // 16-bit sum
    output logic        cout    // Carry-out
);

    logic [15:0] p, g;          // Propagate and Generate
    logic [15:0] c;             // Carry

    // Generate and propagate signals
    assign p = a ^ b;           // Propagate signal
    assign g = a & b;           // Generate signal

    // Carry calculation using Han-Carlson logic
    assign c[0] = cin;
    genvar i;
    generate
        for (i = 1; i < 16; i = i + 1) begin : carry_gen
            assign c[i] = g[i-1]  (p[i-1] & c[i-1]);
        end
    endgenerate

    // Sum calculation
    assign sum = p ^ c;

    // Carry-out
    assign cout = g[15]  (p[15] & c[15]);
```

```
endmodule
```

7 Testbench

Listing 2: Han Calson Adder Testbench

```
module tb_han_carlson_adder;

    // Testbench signals
    logic [15:0] a;
    logic [15:0] b;
    logic cin;
    logic [15:0] sum;
    logic cout;

    // Instantiate the Han-Carlson adder
    han_carlson_adder uut (
        .a(a),
        .b(b),
        .cin(cin),
        .sum(sum),
        .cout(cout)
    );

    // Stimulus process
    initial begin
        // Display header
        $display("A\tB\tCin\tSum\t\tCout");

        // Test case 1
        a = 16'h00FF; b = 16'h0001; cin = 0;
        #10;
        $display("%h\t%h\t%b\t%h\t%b", a, b, cin, sum, cout);

        // Test case 2
        a = 16'hFFFF; b = 16'hFFFF; cin = 1;
        #10;
        $display("%h\t%h\t%b\t%h\t%b", a, b, cin, sum, cout);

        // Test case 3
        a = 16'h1234; b = 16'hABCD; cin = 0;
        #10;
        $display("%h\t%h\t%b\t%h\t%b", a, b, cin, sum, cout);

        // Test case 4
        a = 16'h5678; b = 16'h9ABC; cin = 1;
        #10;
        $display("%h\t%h\t%b\t%h\t%b", a, b, cin, sum, cout);

        // End simulation
        $finish;
    end

endmodule
```

8 Conclusion

The Han-Carlson adder is a high-performance parallel-prefix adder that addresses the limitations of traditional addition methods by leveraging parallel computation for carry propagation. Its design significantly accelerates binary addition through efficient handling of carry signals, which leads to a reduction in critical path length and overall addition time. The adder's scalability makes it well-suited for wide-bit-width applications, ensuring that it can handle modern, high-speed digital systems effectively. By choosing the Han-Carlson adder, designers can achieve improved performance and efficiency in complex arithmetic operations, making it a valuable component in high-performance computing systems.

9 Simulation Results

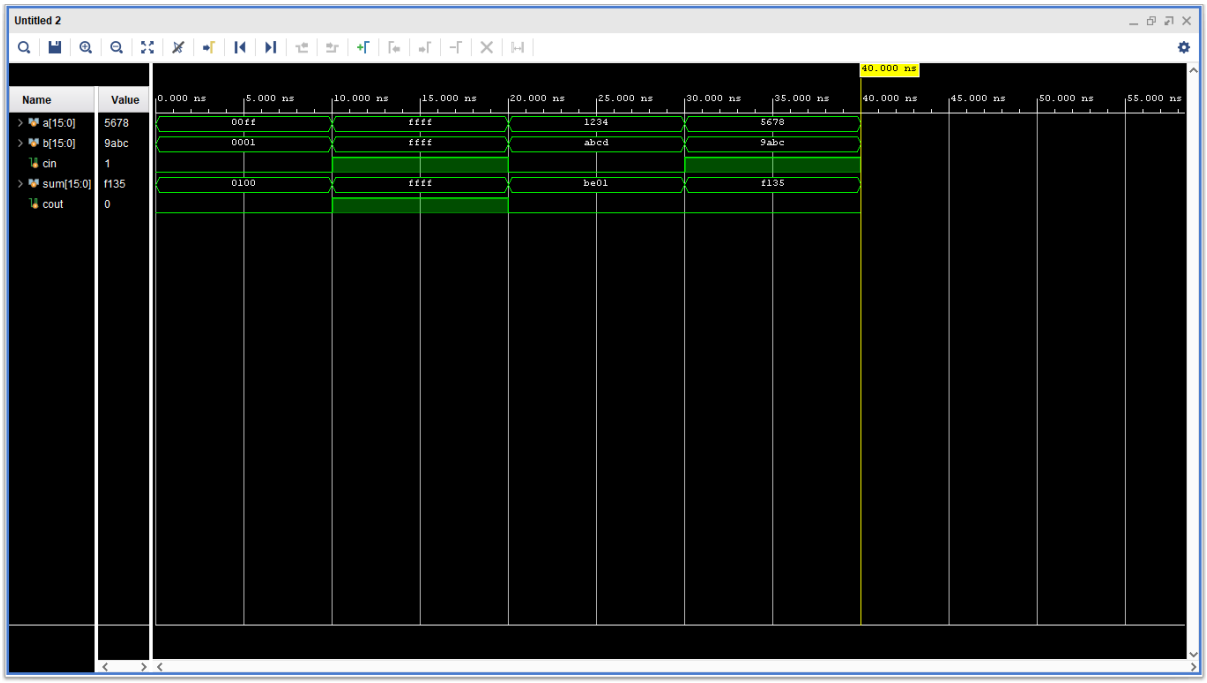

Figure 3: Simulation of Han Carlson Adder

10 References

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