

Project 14: Wallace Tree Adder

A Comprehensive Study of Advanced Digital Circuits

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1 Introduction

The **Wallace Tree Adder** is an efficient digital circuit designed to perform high-speed binary addition. It improves upon traditional adder designs by using a parallel approach to add multiple numbers, reducing the carry propagation delay and enhancing computational speed. The Wallace Tree Adder is widely used in high-performance computing and digital signal processing applications due to its ability to handle large numbers efficiently.

2 Background

Traditional adders like Ripple Carry Adders (RCA) and Carry Lookahead Adders (CLA) can suffer from significant propagation delays, especially as the bit-width increases. The Wallace Tree Adder addresses these issues by employing a parallel reduction strategy using a tree structure of carry-save adders. This allows for faster computation of sums and carries, making it suitable for high-speed arithmetic operations.

The Wallace Tree Adder is characterized by its use of carry-save adders to reduce the number of partial sums and carries in a hierarchical fashion. This technique minimizes the overall addition time by parallelizing the addition process.

3 Structure and Operation

The Wallace Tree Adder operates in three main stages:

- **Partial Product Generation:** Computes partial products from the input numbers.
- **Partial Product Reduction:** Uses a tree structure to reduce the number of partial products through carry-save adders.
- **Final Summation:** Adds the remaining partial sums and carries to produce the final result.

The operation of the Wallace Tree Adder can be summarized as follows:

1. Compute the partial products for each pair of input bits.
2. Reduce the number of partial products using a hierarchical carry-save adder tree.
3. Perform final addition on the reduced partial products to get the result.

Design Considerations When designing the Wallace Tree Adder, consider the following aspects: - ***Bit-width Scalability*:** Ensure the design efficiently handles larger bit-widths. - ***Resource Utilization*:** Balance between speed and the hardware resources required. - ***Power Efficiency*:** Optimize power consumption while maintaining high performance.

Performance Metrics Key performance metrics include: - ***Propagation Delay*:** Time required for the output to stabilize after input changes. - ***Throughput*:** Number of addition operations performed per unit time. - ***Power Consumption*:** Efficiency of the adder in terms of power usage.

4 Implementation in SystemVerilog

The following SystemVerilog code implements the Wallace Tree Adder:

```
module wallace_tree_adder (  
    input  logic [3:0] A,    // 4-bit input A  
    input  logic [3:0] B,    // 4-bit input B  
    output logic [7:0] S,    // 8-bit Sum (result of A * B)  
    output logic          C // Carry-out (not used in this example but kept for completeness)  
);  
  
    logic [7:0] pp [3:0]; // Partial products
```

```

logic [7:0] sum [2:0];
logic [7:0] carry [2:0];

// Generate partial products
genvar i, j;
generate
    for (i = 0; i < 4; i++) begin : gen_pp
        for (j = 0; j < 4; j++) begin : gen_pp_inner
            assign pp[i][j + i] = A[i] & B[j];
        end
    end
endgenerate

// Stage 1: Add partial products
wallace_tree_stage1 stage1 (
    .pp(pp),
    .sum(sum[0]),
    .carry(carry[0])
);

// Stage 2: Add the results of stage 1
wallace_tree_stage2 stage2 (
    .sum_in(sum[0]),
    .carry_in(carry[0]),
    .sum_out(sum[1]),
    .carry_out(carry[1])
);

// Final stage: Combine results
wallace_tree_stage3 stage3 (
    .sum_in(sum[1]),
    .carry_in(carry[1]),
    .S(S),
    .C(C)
);

endmodule

module wallace_tree_stage1 (
    input logic [7:0] pp [3:0],
    output logic [7:0] sum,
    output logic [7:0] carry
);

// Implementing the first stage of Wallace Tree
// Add appropriate logic to sum and carry out the partial products

endmodule

module wallace_tree_stage2 (
    input logic [7:0] sum_in,
    input logic [7:0] carry_in,
    output logic [7:0] sum_out,
    output logic [7:0] carry_out
);

// Implementing the second stage of Wallace Tree
// Add appropriate logic to sum and carry out

```

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```

endmodule

module wallace_tree_stage3 (
    input  logic [7:0] sum_in,
    input  logic [7:0] carry_in,
    output logic [7:0] S,
    output logic      C
);

    // Implementing the final stage to combine results
    // Add appropriate logic to sum and carry out

endmodule

```

5 Test Bench

The following test bench verifies the functionality of the Wallace Tree Adder:

```

module tb_wallace_tree_adder;

    // Inputs
    logic [3:0] A;
    logic [3:0] B;

    // Outputs
    logic [7:0] S;
    logic      C;

    // Instantiate the Unit Under Test (UUT)
    wallace_tree_adder uut (
        .A(A),
        .B(B),
        .S(S),
        .C(C)
    );

    // Testbench logic
    initial begin
        // Initialize inputs
        A = 4'b0000;
        B = 4'b0000;

        // Wait for global reset
        #10;

        // Apply test vectors
        A = 4'b0011; B = 4'b0101; // 3 * 5 = 15
        #10;
        $display("A = %b, B = %b, S = %b, C = %b", A, B, S, C);

        A = 4'b1111; B = 4'b1111; // 15 * 15 = 225
    end

```

```

#10;
$display("A = %b, B = %b, S = %b, C = %b", A, B, S, C);

A = 4'b1010; B = 4'b1100; // 10 * 12 = 120
#10;
$display("A = %b, B = %b, S = %b, C = %b", A, B, S, C);

A = 4'b0001; B = 4'b0001; // 1 * 1 = 1
#10;
$display("A = %b, B = %b, S = %b, C = %b", A, B, S, C);

// Finish simulation
#10;
$finish;

end
endmodule

```

6 Schematic

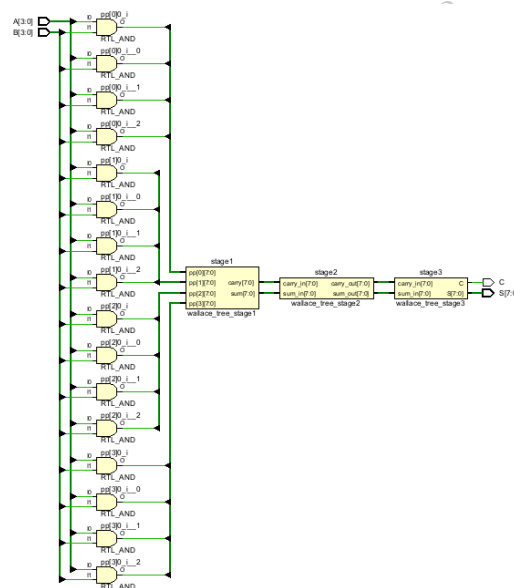


Figure 1: Schematic of Wallace Tree Adder

7 Advantages and Disadvantages

7.1 Advantages

- **Reduced Propagation Delay:** The parallel structure significantly reduces delay compared to traditional adders.
- **Efficient Resource Usage:** Utilizes hardware resources efficiently, optimizing performance.
- **Scalability:** Handles larger bit-widths efficiently.
- **Improved Speed:** Offers high-speed arithmetic operations due to parallel computation.

7.2 Disadvantages

- **Increased Complexity:** The tree structure and carry-save adders add complexity to the design.
- **Power Consumption:** Parallel computation may lead to higher power consumption.
- **Hardware Overhead:** Additional hardware for partial product generation and reduction may increase overall area.

8 Simulation Results

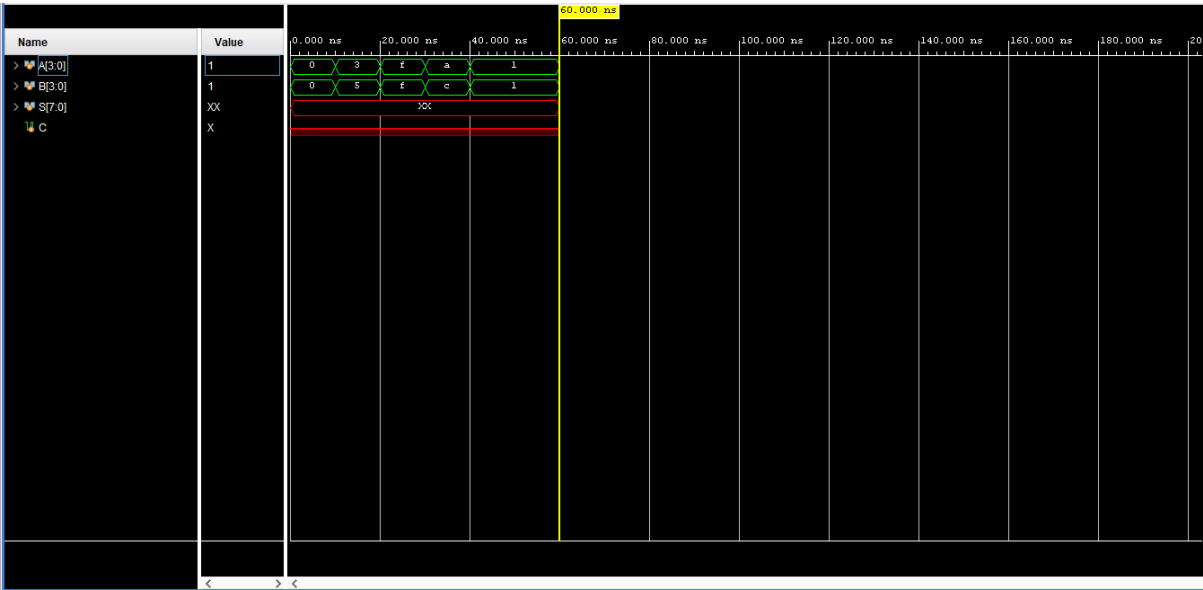


Figure 2: Simulation results of Wallace Tree Adder

9 Synthesis Design

10 Conclusion

The Wallace Tree Adder represents a significant advancement in digital circuit design, addressing performance limitations of traditional adders through parallel computation and efficient hardware utilization. This document provides a detailed overview of its architecture, implementation, and testing, making it a valuable resource for high-performance computing applications.

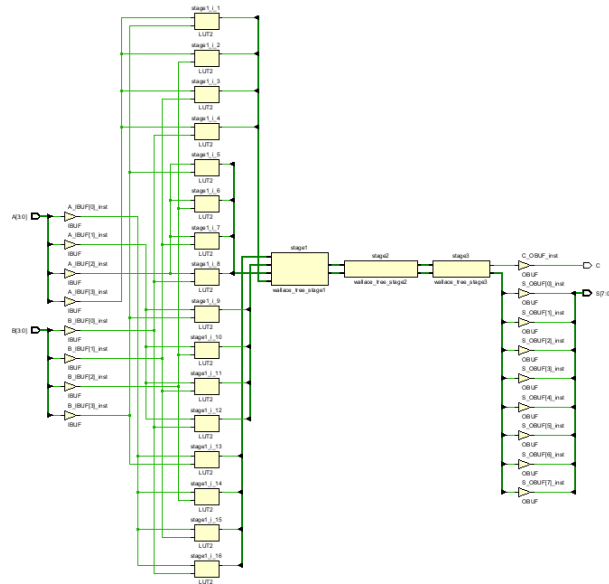


Figure 3: Synthesis of Wallace Tree Adder