Name:Arjunsingh Gautam **Date:23/7/24** **PRN:22070123043**

Experiment No. 2

Aim: Implementation of all gates using Gate flow modelling in Verilog.

Software Tool: Vivado Design Suite,Verilog Programming

Truth Table:

A	B	AND	NAND	OR	NOR	XOR	XNOR
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

Procedure:

1) Open the Xilinx Vivado Design Suite
2) Go to file and click new project
3) Enter the project name and click next
4) Select the family name of the FPGA Device, parameter setting and HDL is verilog click next and click finish.
5) Click new source.
6) Select Verilog module and type file name and click next.
7) Assign input and output port and click next.
8) Finally, the report is shown click finish.
9) Type the program save and check syntax error.
10) To see the output waveform select ISim simulator
11) Give values to the input variables using force clock or force constant and then click run
12) In wave window, click run icon and you can see corresponding output.
13) For synthesis of the design, open XST synthesis tool and run the design for synthesis.
14) Open RTL schematic and Technology schematic and understand implemented design on FPGA
15) Open synthesis result to know resource utilization of the design.

Code:

```
23  module all_gates(
24      input a,
25      input b,
26      output x,
27      output y,
28      output z,
29      output k,
30      output l,
31      output m,
32      output n
33      );
34          and (x, a, b);
35          nand (y, a, b);
36          or (z, a, b);
37          nor (k, a, b);
38          xor (l, a, b);
39          xnor (m, a, b);
40          not (n, a);
41
42  endmodule
43  //22070123043
```

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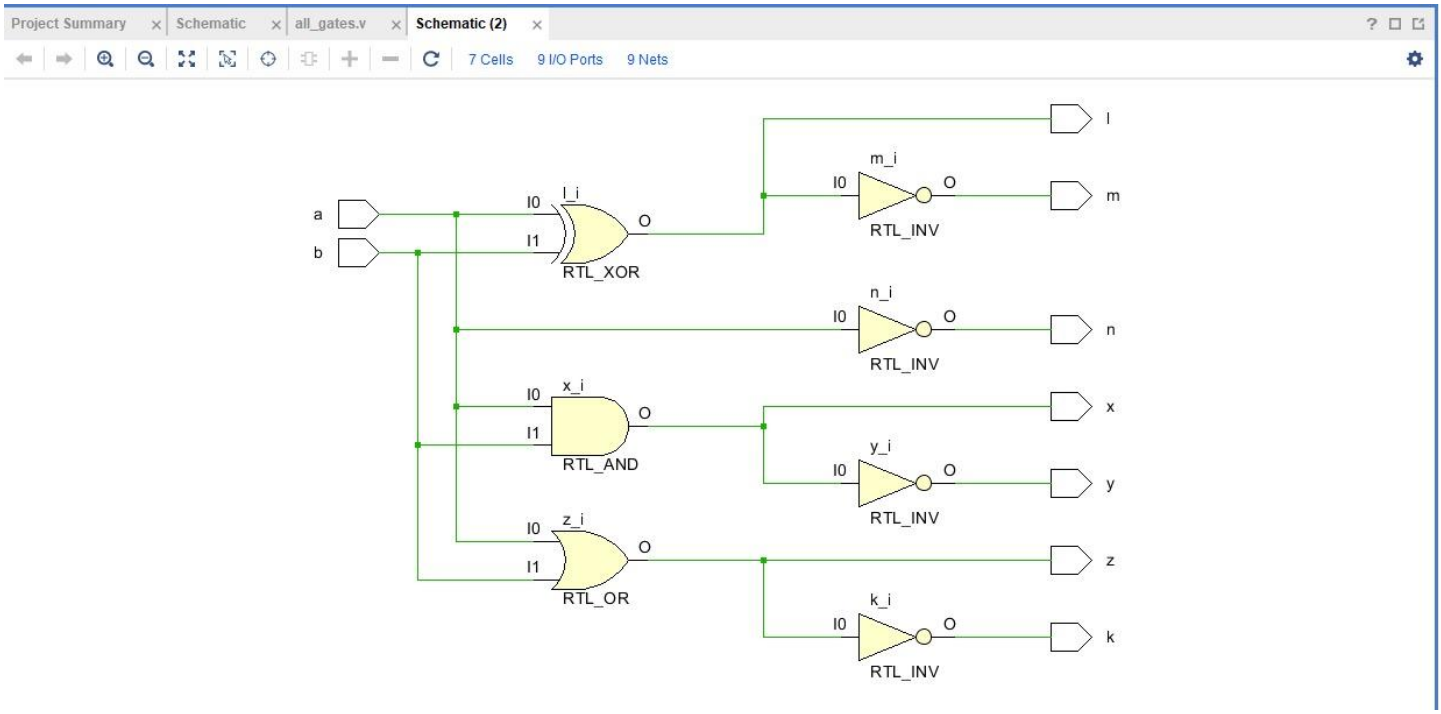
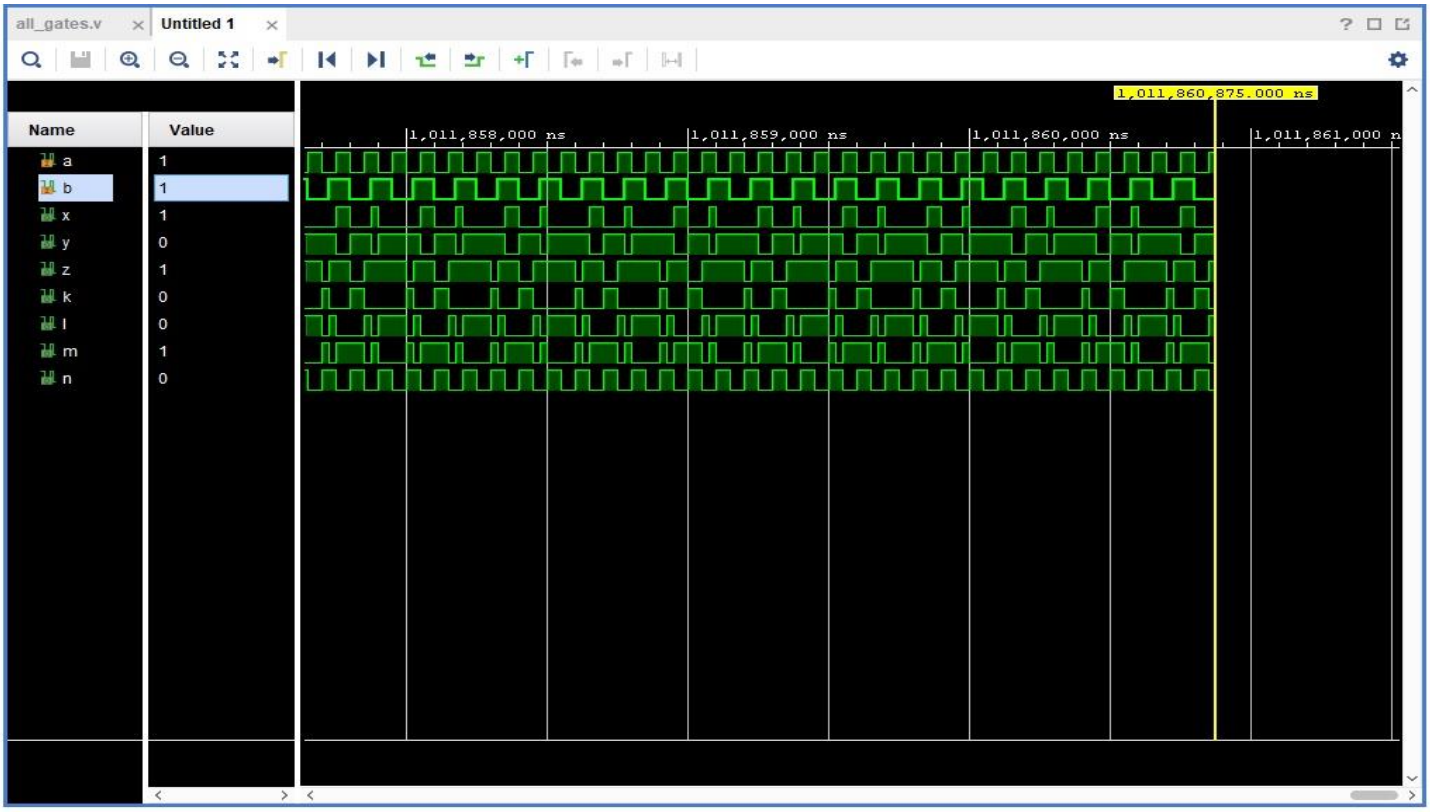
Schematic Design:



Simulation Graph:



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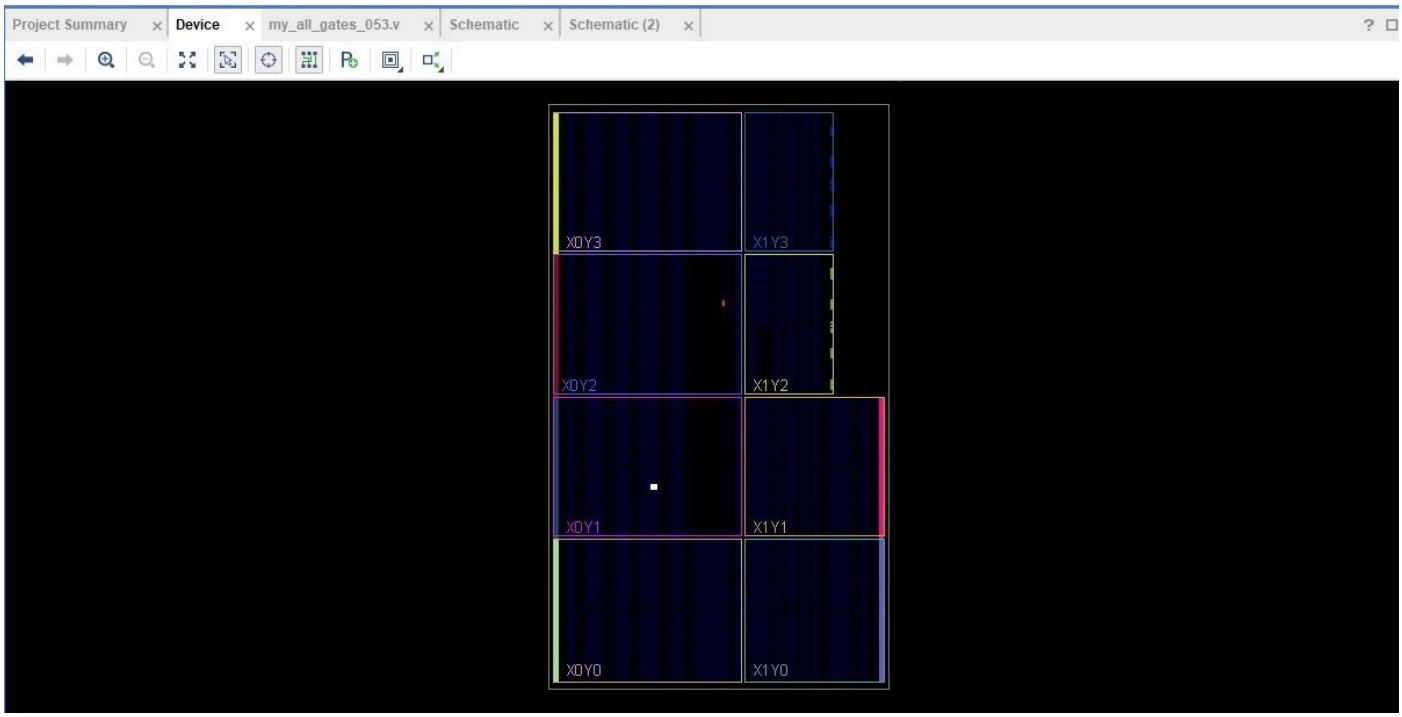
Elaborate Design:



Conclusion:

Implementing fundamental logic gates using Verilog in the Vivado Design Suite provides a comprehensive understanding of digital design and synthesis. The process includes designing each gate (AND, OR, NOT, NAND, NOR, XOR, XNOR) using Verilog, simulating the designs to verify functionality, and analyzing the results through schematic views and waveform simulations.

The use of Vivado's simulation and schematic analysis tools facilitates the verification of logic gate functionality and timing characteristics. Through this approach, designers can confirm that the implemented gates meet the expected logical behavior and performance criteria. This exercise not only reinforces the principles of digital logic design but also provides practical experience with the Vivado Design Suite's features, aiding in the development of skills necessary for more complex digital system designs.