Name:Arjunsingh Gautam **Date:13/8/24** **PRN:22070123043**

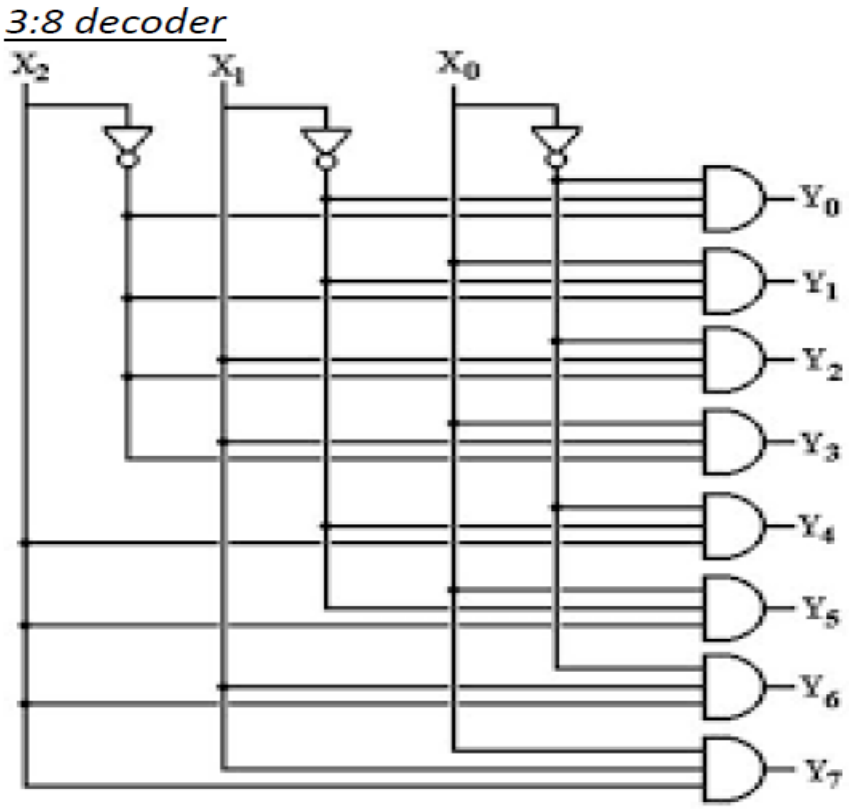
Experiment 4

Aim-1: Implementation of 3:8 decoder using Behavioral Modelling in Verilog.

Software: Xilinx Vivado Design Suite

Theory: Truth table of 8:1 Mux

IN_2	IN_1	IN_0	OUT_7	OUT_6	OUT_5	OUT_4	OUT_3	OUT_2	OUT_1	OUT_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0



Procedure:

1) Open the Xilinx Vivado Design Suite
2) Go to file and click new project
3) Enter the project name and click next
4) Select the family name of the FPGA Device, parameter setting and HDL is verilog click next and click finish.
5) Click new source.

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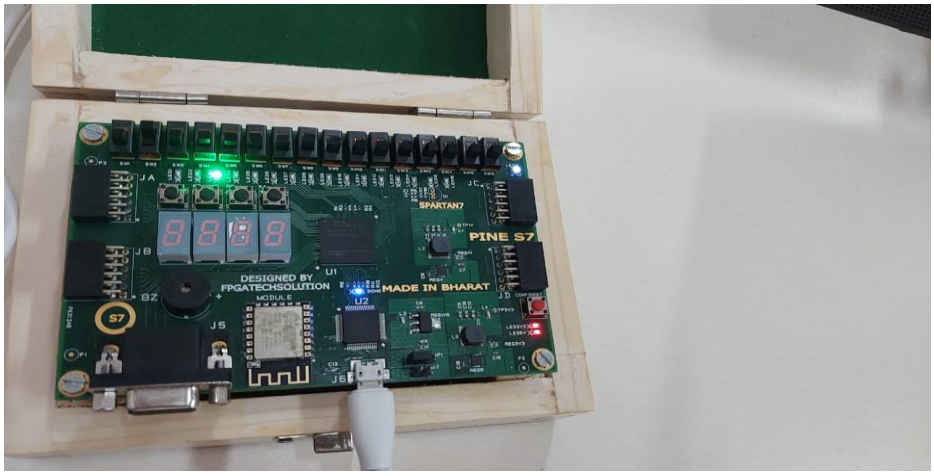
6) Select Verilog module and type file name and click next.
7) Assign input and output port and click next.
8) Finally, the report is shown click finish.
9) Type the program save and check syntax error.
10) To see the output waveform select ISim simulator
11) Give values to the input variables using force clock or force constant and then click run
12) In wave window, click run icon and you can see corresponding output.
13) For synthesis of the design, open XST synthesis tool and run the design for synthesis.
14) Open RTL schematic and Technology schematic and understand implemented design on FPGA
15) Open synthesis result to know resource utilization of the design.

Code:

```
module decoder3to8_ (
input [2:0] in,
output reg [7:0] out
);
always @(in)
case (in)
3'b000 : out = 8'b00000001;
3'b001 : out = 8'b00000010;
3'b010 : out = 8'b00000100;
3'b011 : out = 8'b00001000;
3'b100 : out = 8'b00010000;
3'b101 : out = 8'b00100000;
3'b110 : out = 8'b01000000;
3'b111 : out = 8'b10000000;
default : out = 8'b00000000;
endcase
endmodule
```

Result:



Spartan-7 Physical Simulation

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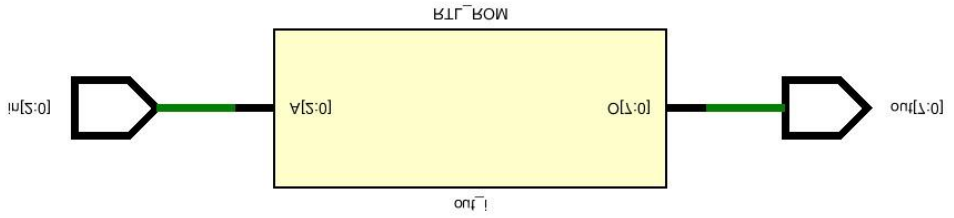
Constraint File

```
set_property -dict { PACKAGE_PIN A5    IOSTANDARD LVCMOS33 } [get_ports { in[0] }];
set_property -dict { PACKAGE_PIN B6    IOSTANDARD LVCMOS33 } [get_ports { in[1] }];
set_property -dict { PACKAGE_PIN F4    IOSTANDARD LVCMOS33 } [get_ports { in[2] }];
set_property -dict { PACKAGE_PIN F3    IOSTANDARD LVCMOS33} [get_ports {out[0]}];
set_property -dict { PACKAGE_PIN E4    IOSTANDARD LVCMOS33} [get_ports {out[1]}];
set_property -dict { PACKAGE_PIN D3    IOSTANDARD LVCMOS33} [get_ports {out[2]}];
set_property -dict { PACKAGE_PIN D4    IOSTANDARD LVCMOS33} [get_ports {out[3]}];
set_property -dict { PACKAGE_PIN C5    IOSTANDARD LVCMOS33} [get_ports {out[4]}];
set_property -dict { PACKAGE_PIN A12   IOSTANDARD LVCMOS33} [get_ports {out[5]}];
set_property -dict { PACKAGE_PIN A13   IOSTANDARD LVCMOS33} [get_ports {out[6]}];
set_property -dict { PACKAGE_PIN B14   IOSTANDARD LVCMOS33} [get_ports {out[7]}];
```

Verilog Code

```
module decoder(
    input [2:0] in,
    output reg [7:0] out
    );
    always @(in)
case (in)
3'b000 : out = 8'b00000001;
3'b001 : out = 8'b00000010;
3'b010 : out = 8'b00000100;
3'b011 : out = 8'b00001000;
3'b100 : out = 8'b00010000;
3'b101 : out = 8'b00100000;
3'b110 : out = 8'b01000000;
3'b111 : out = 8'b10000000;
default : out = 8'b00000000;
endcase
endmodule
//Arjunsingh Gautam
//22070123043
```

Schematic Design



Aim-2: Implementation of 8**:1 mux using:**

a) **Dataflow modeling**
b) **Implementing the design of Spartan-7 kit**

Apparatus: Xilinx Vivado Design Suite

Theory: Truth table of 8:1 Mux

S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4

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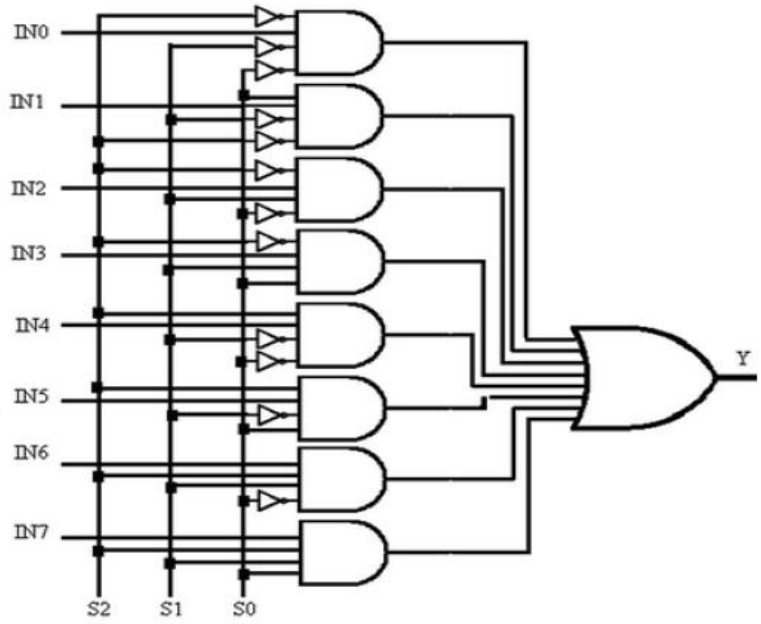
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

CIRCUIT DIAGRAM



Procedure:

1) Open the Xilinx Vivado Design Suite
2) Go to file and click new project
3) Enter the project name and click next
4) Select the family name of the FPGA Device, parameter setting and HDL is verilog click next and click finish.
5) Click new source.
6) Select Verilog module and type file name and click next.
7) Assign input and output port and click next.
8) Finally, the report is shown click finish.
9) Type the program save and check syntax error.
10) To see the output waveform select ISim simulator
11) Give values to the input variables using force clock or force constant and then click run
12) In wave window, click run icon and you can see corresponding output.
13) For synthesis of the design, open XST synthesis tool and run the design for synthesis.
14) Open RTL schematic and Technology schematic and understand implemented design on FPGA
15) Open synthesis result to know resource utilization of the design.

Code:

Dataflow Modelling

```
module mux81_dataflow(
input i0,i1,i2,i3,i4,i5,i6,i7,
input s0,s1,s2,
output out
```

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```
);
assign out = s2?(s1?(s0?i7:i6):(s0?i5:i4)):(s1?(s0?i3:i2):(s0?i1:i0));
endmodule
```

Result:

1.Verilog Code:

```
module mul_df(
    input i0,
    input i1,
    input i2,
    input i3,
    input i4,
    input i5,
    input i6,
    input i7,
    input s0,
    input s1,
    input s2,
    output out
    );
    assign out = s2?(s1?(s0?i7:i6):(s0?i5:i4)):(s1?(s0?i3:i2):(s0?i1:i0));
endmodule
//Arjunsingh Gautam
//22070123043
```

2.Constraint File:

```
set_property -dict { PACKAGE_PIN A5    IOSTANDARD LVCMOS33 } [get_ports { i0 }];
set_property -dict { PACKAGE_PIN B6    IOSTANDARD LVCMOS33 } [get_ports { i1 }];
set_property -dict { PACKAGE_PIN F4    IOSTANDARD LVCMOS33 } [get_ports { i2 }];
set_property -dict { PACKAGE_PIN C3    IOSTANDARD LVCMOS33 } [get_ports { i3 }];
set_property -dict { PACKAGE_PIN C4    IOSTANDARD LVCMOS33 } [get_ports { i4 }];
set_property -dict { PACKAGE_PIN A10   IOSTANDARD LVCMOS33 } [get_ports { i5 }];
set_property -dict { PACKAGE_PIN B13   IOSTANDARD LVCMOS33 } [get_ports { i6 }];
set_property -dict { PACKAGE_PIN C14   IOSTANDARD LVCMOS33 } [get_ports { i7 }];
set_property -dict { PACKAGE_PIN D13   IOSTANDARD LVCMOS33 } [get_ports { s0 }];
set_property -dict { PACKAGE_PIN F14   IOSTANDARD LVCMOS33 } [get_ports { s1 }];
set_property -dict { PACKAGE_PIN G14   IOSTANDARD LVCMOS33 } [get_ports { s2 }];
set_property -dict { PACKAGE_PIN F3    IOSTANDARD LVCMOS33} [get_ports {out}];
```

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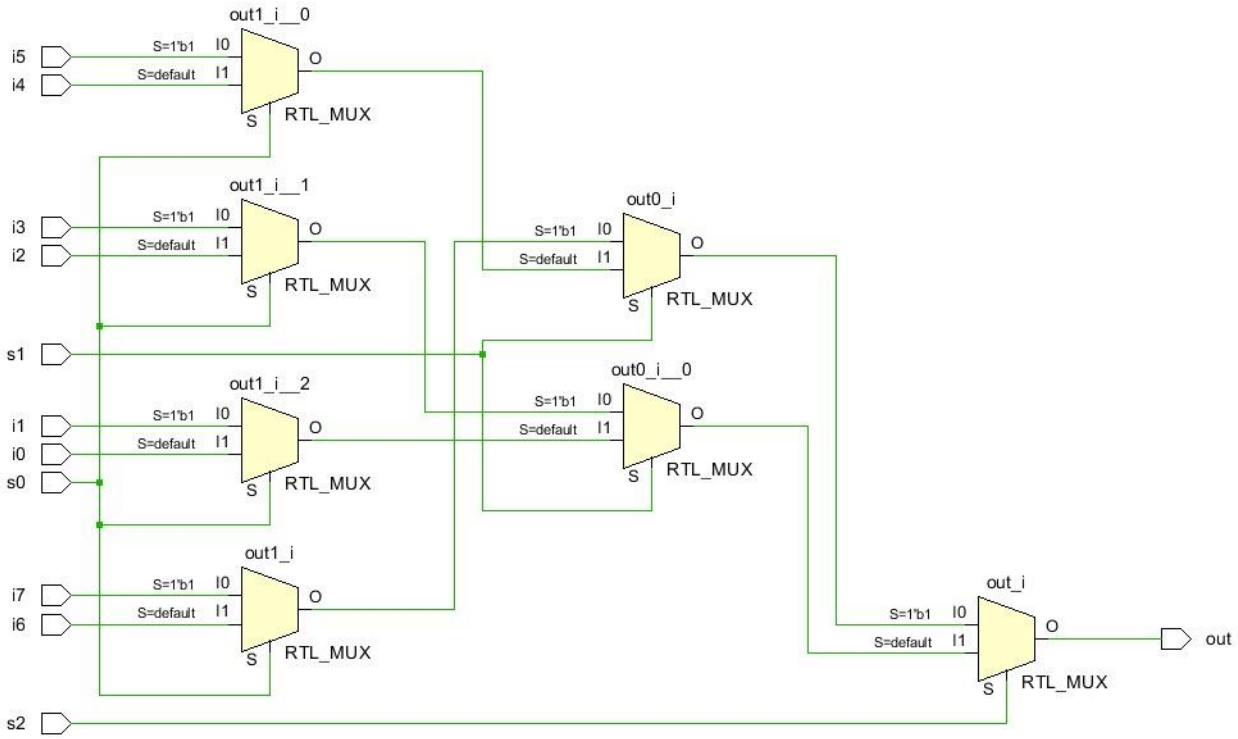
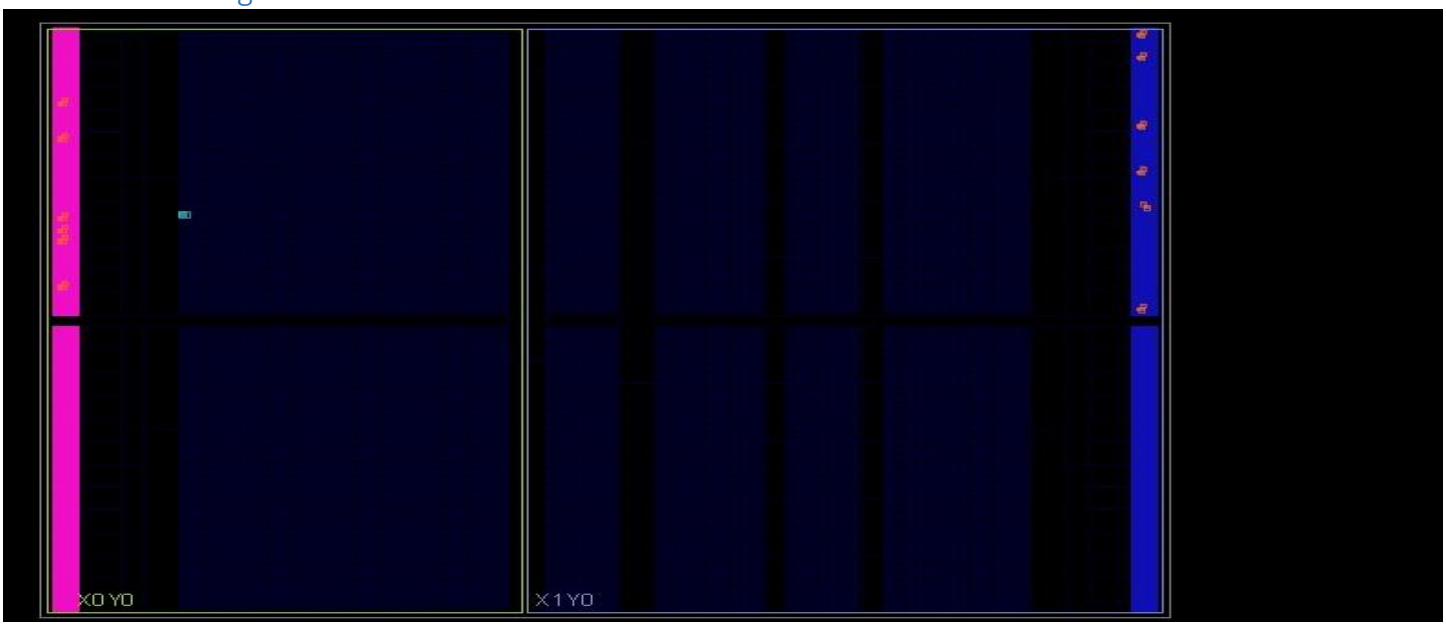
3. Schematic Design:



4. Elaborate Design:



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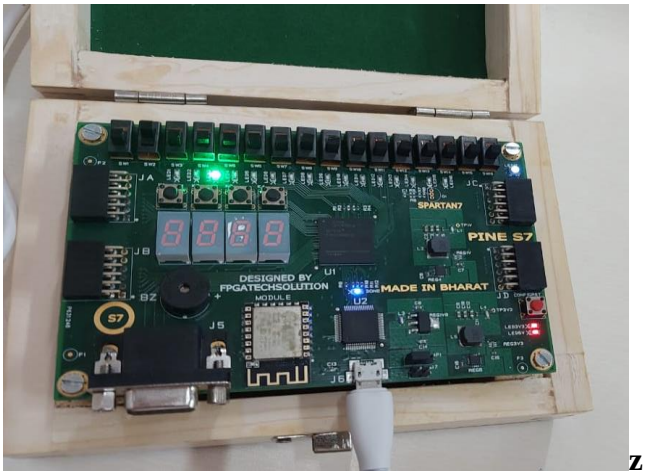
5.FPGA Kit Simulation:



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Conclusion:

- In this experiment we study the functioning of a decoder and also implement the Verilog design on Spartan-7 Hardware board and physically stimulate the design
- We also study about multiplexer and implemented 8:1 multiplexer using data-flow level modelling on Spartan-7 FPGA kit