1.a) Write difference between tasks and functions.
b) Illustrate with an example Array of Instances of Primitives.
c) What are Tristate gates?
d) Mention data types used in Verilog HDL.
e) Write any two sequential models can be used.
f) Write about bidirectional gates.
g) What are parallel blocks?
h) What are time delays with switch primitives?
i) Draw the diagram of NAND gate using CMOS switches.
j) Write Verilog code using Case statement.

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.a) What is functional verification?
b) Write short notes on programming language Interface.
c) Define tri-gate state.
d) What is array of Instances of primitives?
e) Define Initial Construct.
f) Define Blocking and Non-Blocking assignments.
g) Explain Bi-Directional gates.
h) Explain parameter declaration and assignments.
i) Explain Feedback model.
j) Explain test bench techniques.

2. Explain the following "lexical conventions" with examples.
a) White space b) strengths c) Operators [3+3+4]

OR

3.a) Write a short notes on concurrency and functional verification.
b) Explain port Declaration with an example using Verilog code. [5+5]

4.a) Classify and explain strengths and contention resolution.
b) Write Verilog code for 1 to 4 demultiplexer module by using 2 to 4 decoder? [5+5]

OR

5.a) Write Verilog module for a positive edge triggered flip flop with test bench.
b) Explain how the ALWAYS statements are used in Verilog. [5+5]

6.a) Design Verilog module Event construct for a serial data receive and test bench for the same.
b) Design a counter module and test bench to illustrate the use of WAIT. [5+5]

OR

.a) Design half-adder using CMOS switches.
b) Write about basic switch primitives. [5+5]

OR

.a) What do you mean by user defined primitives (UDP) and explain the types with examples?
b) Explain edge sensitive path using an example. [5+5]

).a) What are the rules to be followed to declare and use the bidirectional lines?
b) Write a Verilog module for PLA. [5+5]

OR

1.a) Explain in detail about formal verification of a system.
b) What is the use of assert cycle sequence and assert next? Explain using an example. [5+5]

a) Write a verilog program for 8x1 MUX using Structured I

b) Write a verilog program for Half adder using Structured

a) Write, verify and synth size a 16 bit adder sub tractor.

Write down the Verilog code for 4-to-1 Multiplexer using Behavioral modelling.
Write down the Verilog code for 4-to-1 multiplexer using logic equation or using conditional operator in data flow modelling.

Write a short note on the following.
(i) Casex and casez statement
(ii) Power and Ground
(iii) Parallel connection and full connection

Distinguish between always and initial constructs in Verilog HDL?
Explain the role of Sensitivity list in Behavioral Modeling?
What do you mean by Zero assignment delay?
Explain about Level-Sensitive event control construct?
Generate clock using forever loop construct?
Describe the role of local variables?
Explain the concept of disable construct in Verilog HDL?
Find the output value of A and B in following two cases?

```
A = 2'b00;
B = 2'b01;
A <= B;
B <= A;
```

```
A = 2'b00;
B = 2'b01;
A = B;
B = A;
```

What is the result of case statement without default statement?
Distinguish between active and inactive events in simulation flow?
Draw the flow chat of if-else construct?
Difference between “repeat” and “for” loop construct with valid example?
Draw the flow chat “for” construct?
Give the example of “force-release”?
Explain the concept of “event” construct with valid example?
Design a 2 to 4 Decoder using case construct?
Distinguish between $display and $write?
Explain the use of the character set “%0d” in display system Task?
What is the difference between the following two lines of Verilog code?
#5 a = b;
a = #5 b;
Write a Verilog code for synchronous and asynchronous reset?
Explain the concept of Multiple initial constructs?
Explain the concept of Multiple always constructs?
Distinguish between Blocking and Non-Blocking Assignments with examples?
Explain 3:8 Decoder using Case Construct?
a) Distinguish between casex and casez?
b) Write the 2:4 Priority Encoder Verilog HDL code.
Design an up down counter using ternary operator with reference to negative edge of clock?
Explain the concept of Event control in behavioral modeling?
Design a Priority Encoder circuit using case/casex/casez concept?
Distinguish between always and initial block
Design a module and test bench of a shift register with facility for right and left?
Describe each block in Flowchart of Simulation flow?

Design a 1:4 De-Mux using if-else construct?
Explain the concept of Multiple initial constructs?
Explain the concept of Multiple always constructs?
Distinguish between Blocking and Non-Blocking Assignments with examples?
Explain 3:8 Decoder using Case Construct?
a) Distinguish between casex and casez?
b) Write the 2:4 Priority Encoder Verilog HDL code.
Design an up down counter using ternary operator with reference to negative edge of clock?
Explain the concept of Event control in behavioral modeling?
Design a Priority Encoder circuit using case/casex/casez concept?
Explain the concept of assign – deassign Concept using example?
Explain the concept of "disable" Concept using example?
Distinguish between Sequential Block (begin-end) and Parallel Block (fork-join) with examples?
Design a module and test bench of a shift register with facility for right and left?
Describe each block in Flowchart of Simulation flow?
Design a 1:4 De-Mux using if-else construct?
Write a Verilog code for binary to gray code and vice-versa.

Write a Verilog code for 4 : 1 Multiplexer.

What are delay Delay models , types of delays

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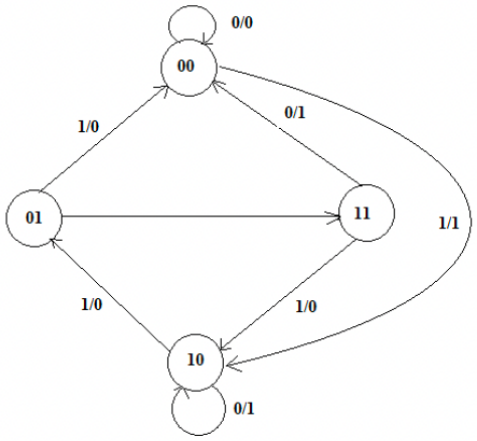
Define concurrency.
Explain about identifiers.
Discuss about latch.
Explain in brief the built-in primitive gates in verilog HDL.
Give the syntax of event construct.
Give the syntax of disable construct.
Define $finish task.
What is the purpose of using system tasks and functions in verilog

a. Explain Mealy and Moore model of a clocked synchronous sequential network.
b. Construct a sequential logic circuit with single input and single output by obtaining the state and table for the given state diagram using JK FF



- FSM for arbiter logic, priority detector, traffic light controllers
- Sequence detectors using mealy and moore draw state diagrams, and write Verilog codes.

- Describe mealy and moore machine and difference between them

Discuss the different levels of abstraction used in Verilog modelling.
What is stimulus? Explain different types of stimulus block instantiation.
Describe the digital system design using hierarchical design methodologies

How is Verilog different from High level language.

Describe the digital system design using hierarchical design methodologies
What are primitives in Verilog give examples

Bring out the difference between task and functions.
Write Verilog program to call a function called calc_parity which computes the parity of a 32-bit data, [31-0]Data and display odd or even parity message.
What do you mean by simulation and synthesis in VLSI design
What do you mean by PLD's?

Difference between PLD PLA and PALs
Memories and their application in FPGA/CPLD
Architecture of CPLD and FPGA(basic)
Interconnects, logic blocks, CLBs and I/O blocks

Also study whatever we have studied in class . PPTs are already shared with you