INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR

COMPUTER ORGANIZATION LABORATORY

ASSIGNMENT 5

DESIGN OF FINITE STATE MACHINES

GROUP MEMBERS

GROUP 54:

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Q1] **Linear Feedback Shift Register**

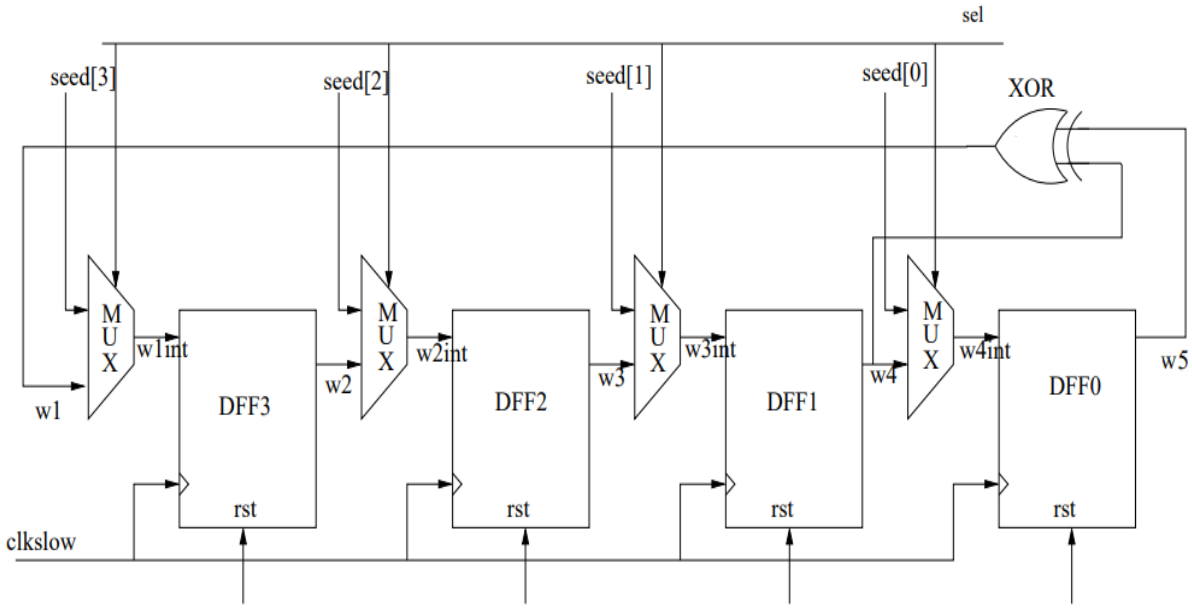

Fig. Sequential LFSR Circuit Diagram

Given an input seed, LFSR is capable of generating pseudo random numbers by shifting bits and computing the next input bit using an XOR gate. The ‘rst’ bit is used to restore all the flip-flop values to zero and the ‘sel’ bit helps in storing the seed into the flip-flop.

Design Summary

```
Top Level Output File Name         : LFSR_main.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 5
#      LUT2                        : 1
#      LUT3                        : 4
# FlipFlops/Latches                : 4
#      FDC                         : 4
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 10
#      IBUF                        : 6
#      OBUF                        : 4

Device utilization summary:
---------------------------

Selected Device : 7a100tcsg324-1


Slice Logic Utilization:
 Number of Slice Registers:                 4  out of  126800     0%
 Number of Slice LUTs:                      5  out of  63400      0%
    Number used as Logic:                   5  out of  63400      0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:        9
   Number with an unused Flip Flop:         5  out of      9     55%
   Number with an unused LUT:               4  out of      9     44%
   Number of fully used LUT-FF pairs:       0  out of      9      0%
   Number of unique control sets:           4

IO Utilization:
 Number of IOs:                            11
 Number of bonded IOBs:                    11  out of    210      5%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                  1  out of     32      3%
```

Timing Report

- Timing analysis when the FSM is active

```
Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 1.719ns (frequency: 581.734MHz)
  Total number of paths / destination ports: 5 / 4
-------------------------------------------------------------------------
Delay:               1.719ns (Levels of Logic = 4)
  Source:            DFF0/Q (FF)
  Destination:       DFF3/Q (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: DFF0/Q to DFF3/Q
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q             2   0.478   0.542  Q (Q)
     end scope: 'DFF0:Q'
     LUT2:I0->O           1   0.124   0.421  Mxor_nextBit_xo<0>1 (nextBit)
     begin scope: 'MUX3:b'
     LUT3:I2->O           1   0.124   0.000  Mmux_f11 (f)
     end scope: 'MUX3:f'
     begin scope: 'DFF3:D'
     FDC:D                    0.030          Q
    ----------------------------------------
    Total                     1.719ns (0.756ns logic, 0.963ns route)
                                      (44.0% logic, 56.0% route)

-------------------------------------------------------------------------
```

The delay associated with the critical path is 1.719 ns.

Q2] **FSM for 2's Complement**

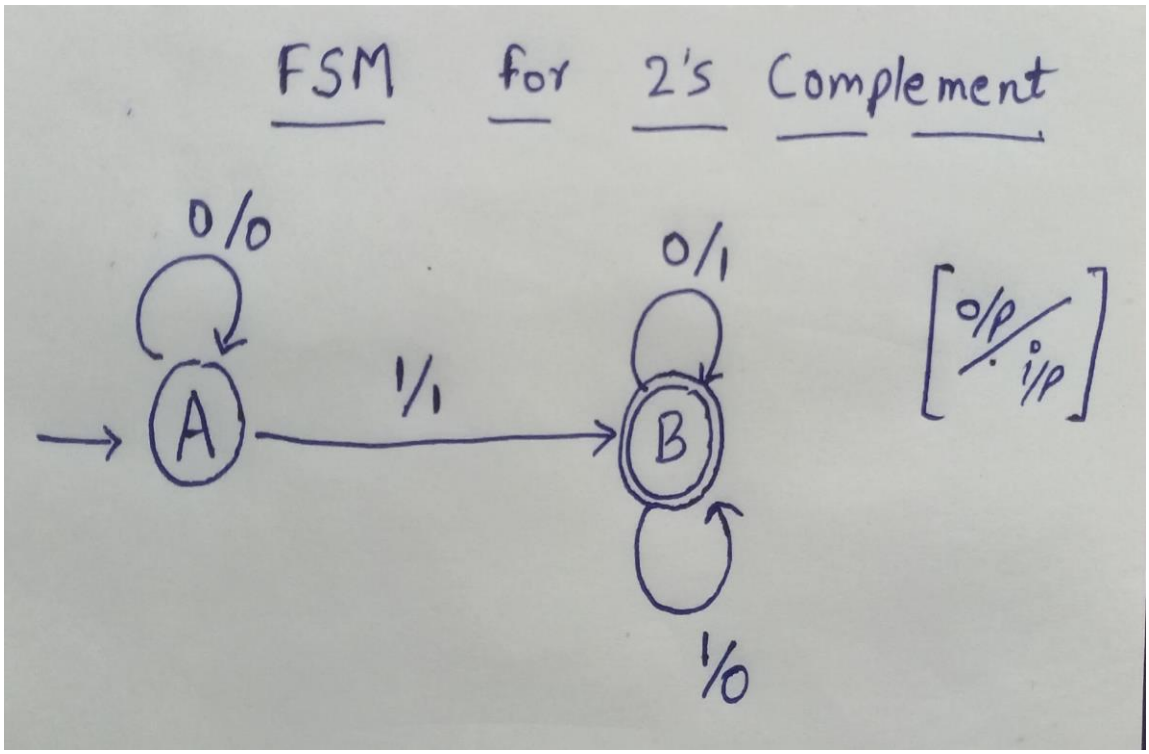

Fig. State Diagram

For an input binary bit stream, the FSM outputs the 2's complement. Follows the implementation of a Mealy Machine.

Design Summary

```
Top Level Output File Name         : twos_comp.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 2
#      LUT2                        : 2
# FlipFlops/Latches                : 2
#      FDC                         : 2
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 3
#      IBUF                        : 2
#      OBUF                        : 1

Device utilization summary:
---------------------------

Selected Device : 7a100tcsg324-1


Slice Logic Utilization:
 Number of Slice Registers:              2  out of  126800     0%
 Number of Slice LUTs:                   2  out of  63400      0%
    Number used as Logic:                2  out of  63400      0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     4
   Number with an unused Flip Flop:      2  out of      4     50%
   Number with an unused LUT:            2  out of      4     50%
   Number of fully used LUT-FF pairs:    0  out of      4      0%
   Number of unique control sets:        1

IO Utilization:
 Number of IOs:                          4
 Number of bonded IOBs:                  4  out of    210      1%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     32      3%
```

Timing Report

- Timing analysis when the FSM is active

```
Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 1.059ns (frequency: 944.287MHz)
  Total number of paths / destination ports: 2 / 2
-------------------------------------------------------------------------
Delay:               1.059ns (Levels of Logic = 1)
  Source:            state (FF)
  Destination:       state (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: state to state
                            Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q              2   0.478   0.427  state (state)
     LUT2:I1->O            1   0.124   0.000  Mmux_GND_1_o_GND_1_o_MUX_2_o11 (GND_1_o_GND_1_o_MUX_2_o)
     FDC:D                     0.030          out
    ----------------------------------------
    Total                      1.059ns (0.632ns logic, 0.427ns route)
                                       (59.7% logic, 40.3% route)
```

The delay associated with the critical path is 1.059 ns.

Q3] **Divisibility of a binary number by 3**

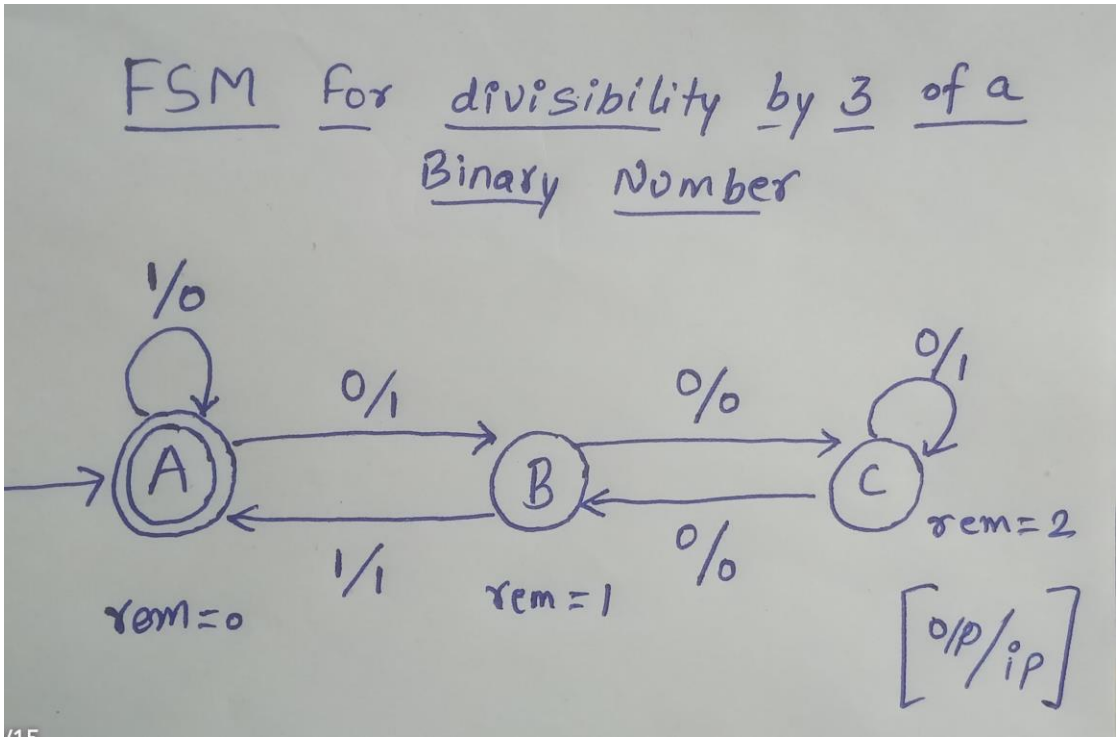

Fig. State Diagram

Here, State A: accept state (remainder = 0)
Input 0: Current binary number (already divisible by 3) is multiplied by 2, which also makes it divisible by 3.
Input 1: Current binary number (already divisible by 3) is multiplied by 2 and 1 is added to the result. Thus, the remainder is 1 and the current state transitions to state B.

Similarly, State B: (remainder = 1)
Input 0: newNum = (currNum * 2),
Remainder (=1) is multiplied by 2, thus transitioning to state C.

Input 1: newNum = (currNum * 2) + 1,
Remainder (=1) is multiplied by 2 and finally 1 is added,
Rem = (1 * 2) + 1 = 3, that is divisible by 3, thus, transitioning to state A.

State C: (remainder = 2)
Input 0: newNum = (currNum * 2),
Remainder (=2) is multiplied by 2, thus transitioning to state B.

Input 1: newNum = (currNum * 2) + 1,
Remainder (=2) is multiplied by 2 and finally 1 is added,
Rem = (2 * 2) + 1 = 5%3 = 2, thus, transitioning to state C.

Design Summary

```
================================================================================
*                            Design Summary                                    *
================================================================================

Top Level Output File Name         : multi_3_fsm.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 3
#      LUT3                        : 2
#      LUT4                        : 1
# FlipFlops/Latches                : 3
#      FDR                         : 3
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 3
#      IBUF                        : 2
#      OBUF                        : 1

Device utilization summary:
---------------------------

Selected Device : 7a100tcsg324-1


Slice Logic Utilization:
 Number of Slice Registers:                3  out of  126800     0%
 Number of Slice LUTs:                     3  out of  63400      0%
    Number used as Logic:                  3  out of  63400      0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:       6
   Number with an unused Flip Flop:        3  out of      6     50%
   Number with an unused LUT:              3  out of      6     50%
   Number of fully used LUT-FF pairs:      0  out of      6      0%
   Number of unique control sets:          1

IO Utilization:
 Number of IOs:                            4
 Number of bonded IOBs:                    4  out of    210      1%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                 1  out of     32      3%
```

Timing Report

- Timing analysis when the FSM is active

```
Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 1.354ns (frequency: 738.552MHz)
  Total number of paths / destination ports: 7 / 3
-------------------------------------------------------------------------
Delay:               1.354ns (Levels of Logic = 1)
  Source:            out (FF)
  Destination:       out (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: out to out
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q             2   0.478   0.722  out (out_OBUF)
     LUT4:I1->O           1   0.124   0.000  out_rstpot (out_rstpot)
     FDR:D                    0.030          out
    ----------------------------------------
    Total                     1.354ns (0.632ns logic, 0.722ns route)
                                      (46.7% logic, 53.3% route)
```

The delay associated with the critical path is 1.354 ns.

Q4] **32-bit Sequential Unsigned Comparator**

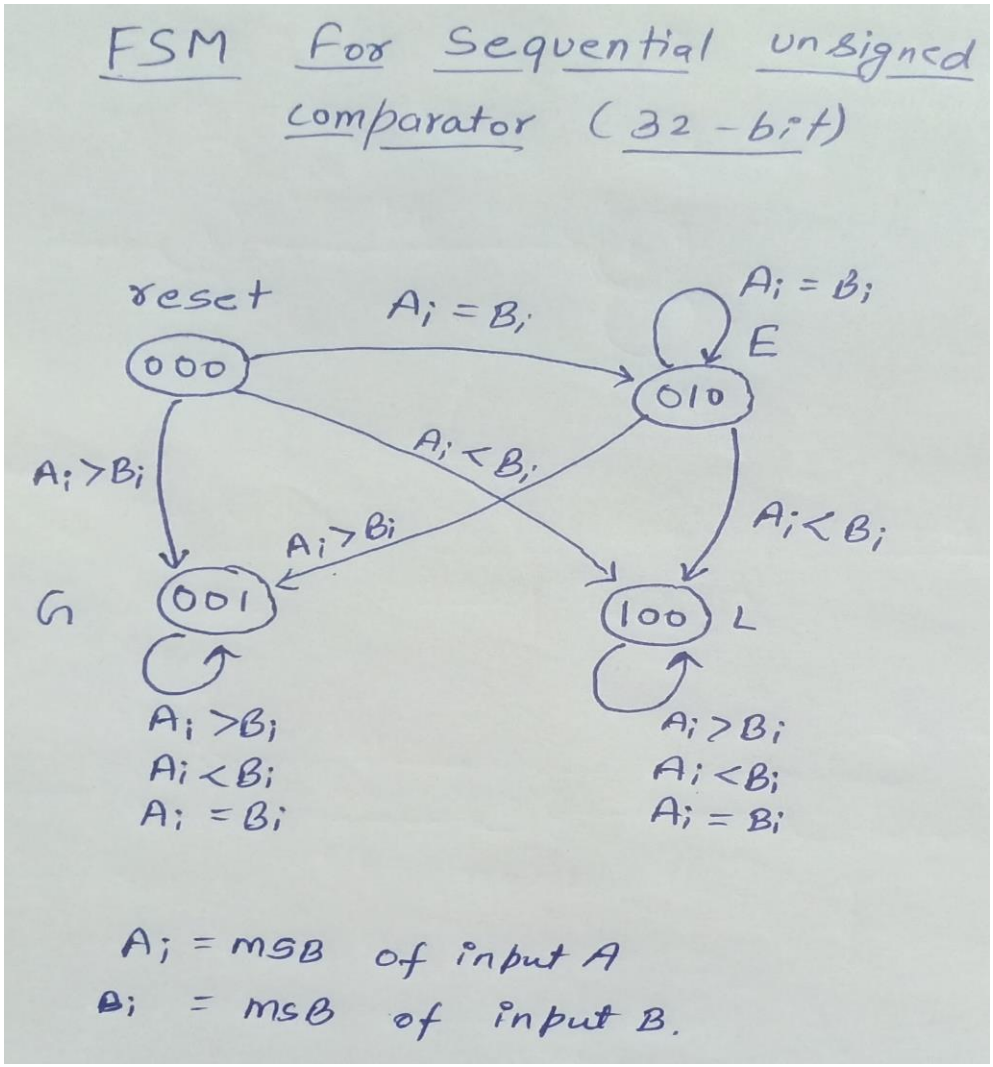

Fig. State Diagram

At each clock cycle, obtain the MSB of both the 32-bit inputs A and B and compare them. If $A_i < B_i$ or $A_i > B_i$, the input control bit 'op' is set to 1 and the comparison process is stopped. If $A_i = B_i$, the bits are shifted to the left and the corresponding MSB's are checked until all 32-bits are covered.

Design Summary

```
Top Level Output File Name         : seq_cmp.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 99
#      GND                         : 1
#      LUT2                        : 2
#      LUT3                        : 62
#      LUT4                        : 3
#      LUT6                        : 17
#      MUXCY                       : 13
#      VCC                         : 1
# FlipFlops/Latches                : 69
#      FD                          : 69
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 69
#      IBUF                        : 65
#      OBUF                        : 4

Device utilization summary:
---------------------------

Selected Device : 7a100tcsg324-1


Slice Logic Utilization:
 Number of Slice Registers:              69  out of  126800     0%
 Number of Slice LUTs:                   84  out of  63400      0%
    Number used as Logic:                84  out of  63400      0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     86
   Number with an unused Flip Flop:      17  out of     86     19%
   Number with an unused LUT:             2  out of     86      2%
   Number of fully used LUT-FF pairs:    67  out of     86     77%
   Number of unique control sets:         1

IO Utilization:
 Number of IOs:                          70
 Number of bonded IOBs:                  70  out of    210     33%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     32      3%
```

Timing Report

- Timing analysis when the FSM is active

```
Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 3.422ns (frequency: 292.205MHz)
  Total number of paths / destination ports: 339 / 67
-------------------------------------------------------------------------
Delay:               3.422ns (Levels of Logic = 13)
  Source:            tempA_17 (FF)
  Destination:       leg_1 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: tempA_17 to leg_1
                            Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q               1   0.478   0.421  tempA_17 (tempA_17)
     LUT3:I2->O            2   0.124   0.945  Mmux_tempA[31]_A[31]_mux_3_OUT91 (tempA[31]_A[31]_mux_3_OUT<17>)
     LUT6:I0->O            1   0.124   0.000  tempA[31]_tempB[31]_AND_1_o_wg_lut<1> (tempA[31]_tempB[31]_AND_1_o_wg_lut<1>)
     MUXCY:S->O            1   0.472   0.000  tempA[31]_tempB[31]_AND_1_o_wg_cy<1> (tempA[31]_tempB[31]_AND_1_o_wg_cy<1>)
     MUXCY:CI->O           1   0.029   0.000  tempA[31]_tempB[31]_AND_1_o_wg_cy<2> (tempA[31]_tempB[31]_AND_1_o_wg_cy<2>)
     MUXCY:CI->O           1   0.029   0.000  tempA[31]_tempB[31]_AND_1_o_wg_cy<3> (tempA[31]_tempB[31]_AND_1_o_wg_cy<3>)
     MUXCY:CI->O           1   0.029   0.000  tempA[31]_tempB[31]_AND_1_o_wg_cy<4> (tempA[31]_tempB[31]_AND_1_o_wg_cy<4>)
     MUXCY:CI->O           1   0.029   0.000  tempA[31]_tempB[31]_AND_1_o_wg_cy<5> (tempA[31]_tempB[31]_AND_1_o_wg_cy<5>)
     MUXCY:CI->O           1   0.029   0.000  tempA[31]_tempB[31]_AND_1_o_wg_cy<6> (tempA[31]_tempB[31]_AND_1_o_wg_cy<6>)
     MUXCY:CI->O           1   0.029   0.000  tempA[31]_tempB[31]_AND_1_o_wg_cy<7> (tempA[31]_tempB[31]_AND_1_o_wg_cy<7>)
     MUXCY:CI->O           1   0.029   0.000  tempA[31]_tempB[31]_AND_1_o_wg_cy<8> (tempA[31]_tempB[31]_AND_1_o_wg_cy<8>)
     MUXCY:CI->O           1   0.029   0.000  tempA[31]_tempB[31]_AND_1_o_wg_cy<9> (tempA[31]_tempB[31]_AND_1_o_wg_cy<9>)
     MUXCY:CI->O           4   0.029   0.441  tempA[31]_tempB[31]_AND_1_o_wg_cy<10> (tempA[31]_tempB[31]_AND_1_o)
     LUT6:I5->O            1   0.124   0.000  _n0050<1>1 (_n0050<1>)
     FD:D                      0.030          leg_1
    ----------------------------------------
    Total                      3.422ns (1.615ns logic, 1.807ns route)
                                       (47.2% logic, 52.8% route)
```

The delay associated with the critical path is 3.422 ns.