University of California, Irvine Fall 2016

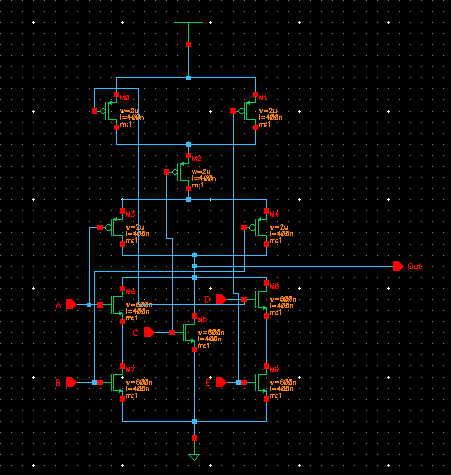
## **EECS 119 Introduction to VLSI Design**

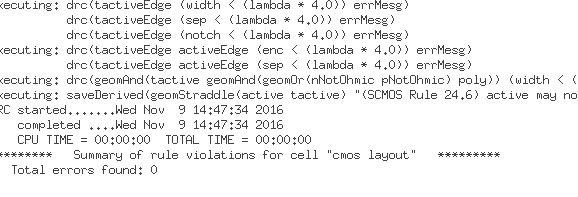
**Design Project #2**

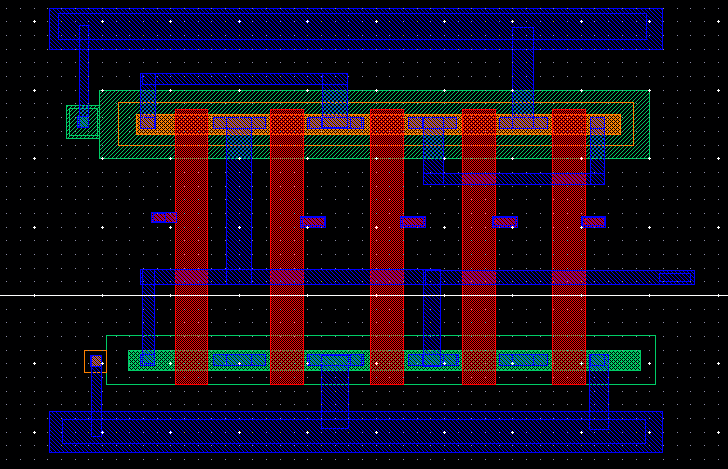
Design a static CMOS logic gate that implements the following logic function.

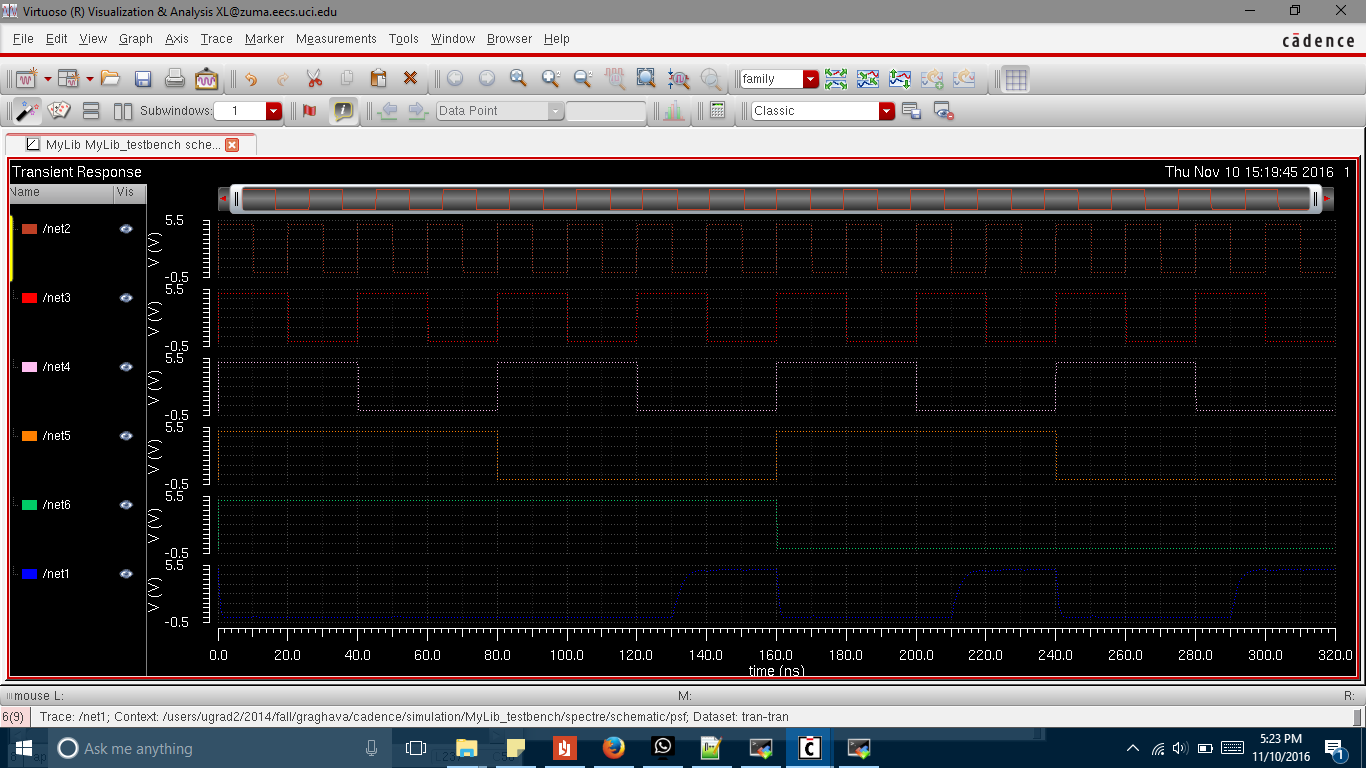
F = ((A.B) + C + (D.E))’



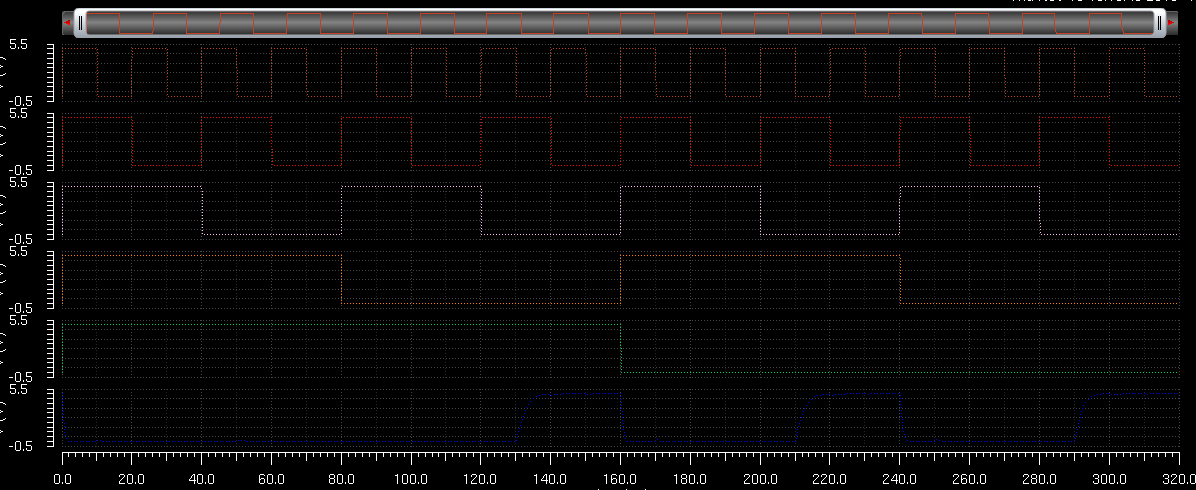
***Circuit Diagram***

  
Verifying the layout to find no errors





Output realization:



Verified result.