**EECS 119**

**Project #4**

**BCD Counter**

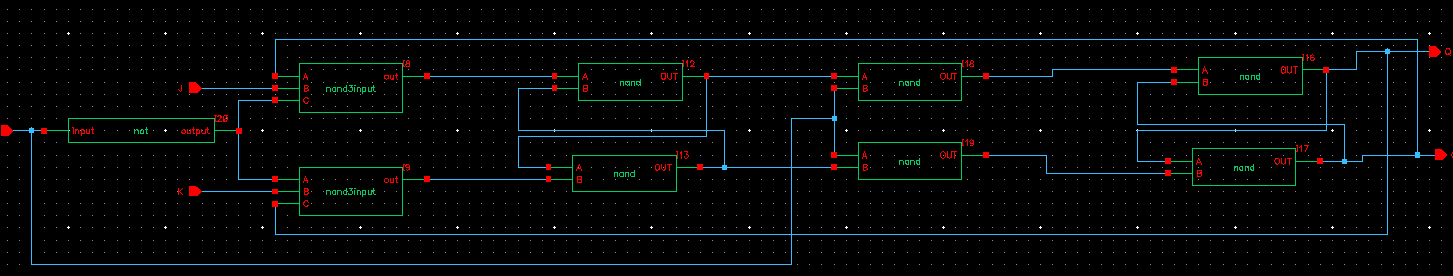
Design a 4 bit BCD up/down counter which will count in a loop, up or down, (0→1→2→3→4→5→6→7→8→9→0 or 0→9→8→7→6→5→4→3→2→1→0) depending upon the value of up/down bit.

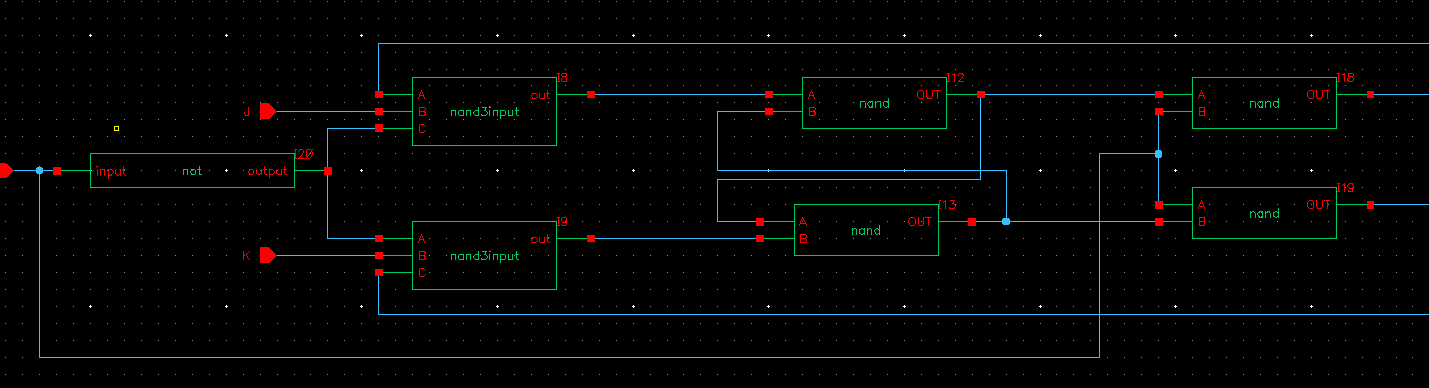
1. Design the circuit.
2. Obtain the layout.
3. Simulate the **layout** and plot each of the four outputs and the clock input to verify that the counter counts in correct sequence.
4. Demonstrate layout simulation.

In order to make a 4 bit BCD up/down counter we will need 4 JK flip flops and a few XOR, NOT, 2to1 MUX and also an 3 input NAND.

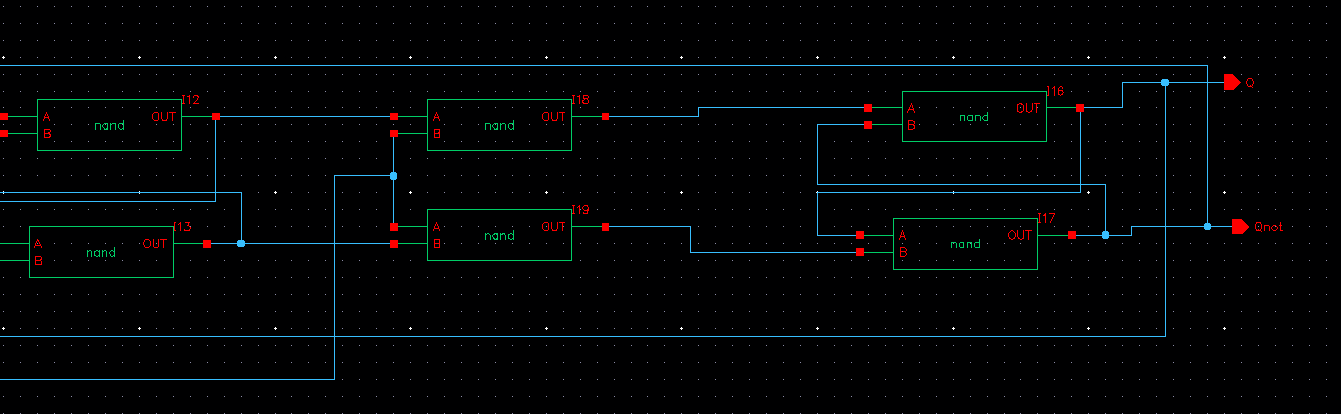
Let us start with a JK flip FLOP. We will not dive into how an NAND gate is built but how we use the NAND gate to make a Flip Flop(also since we did in the last assignment.)

**Flip Flop:**



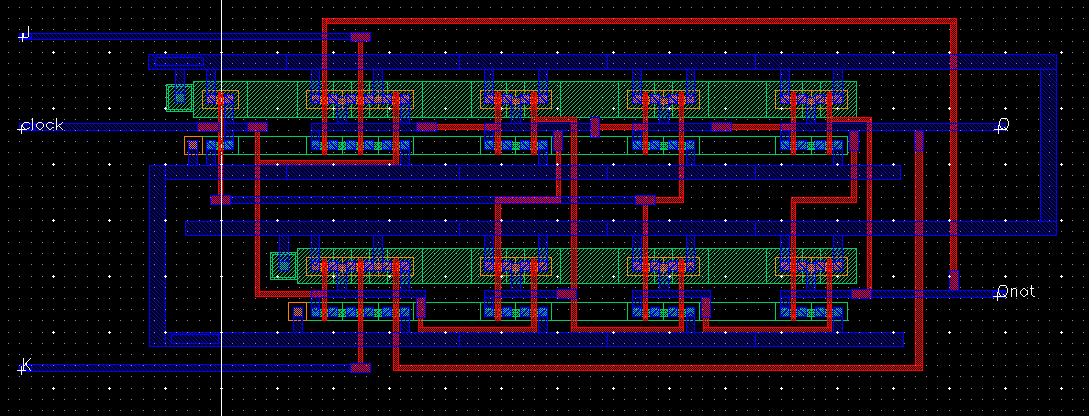


*Part1*

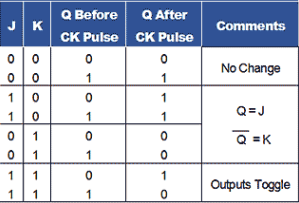


*Part2*

**Layout**

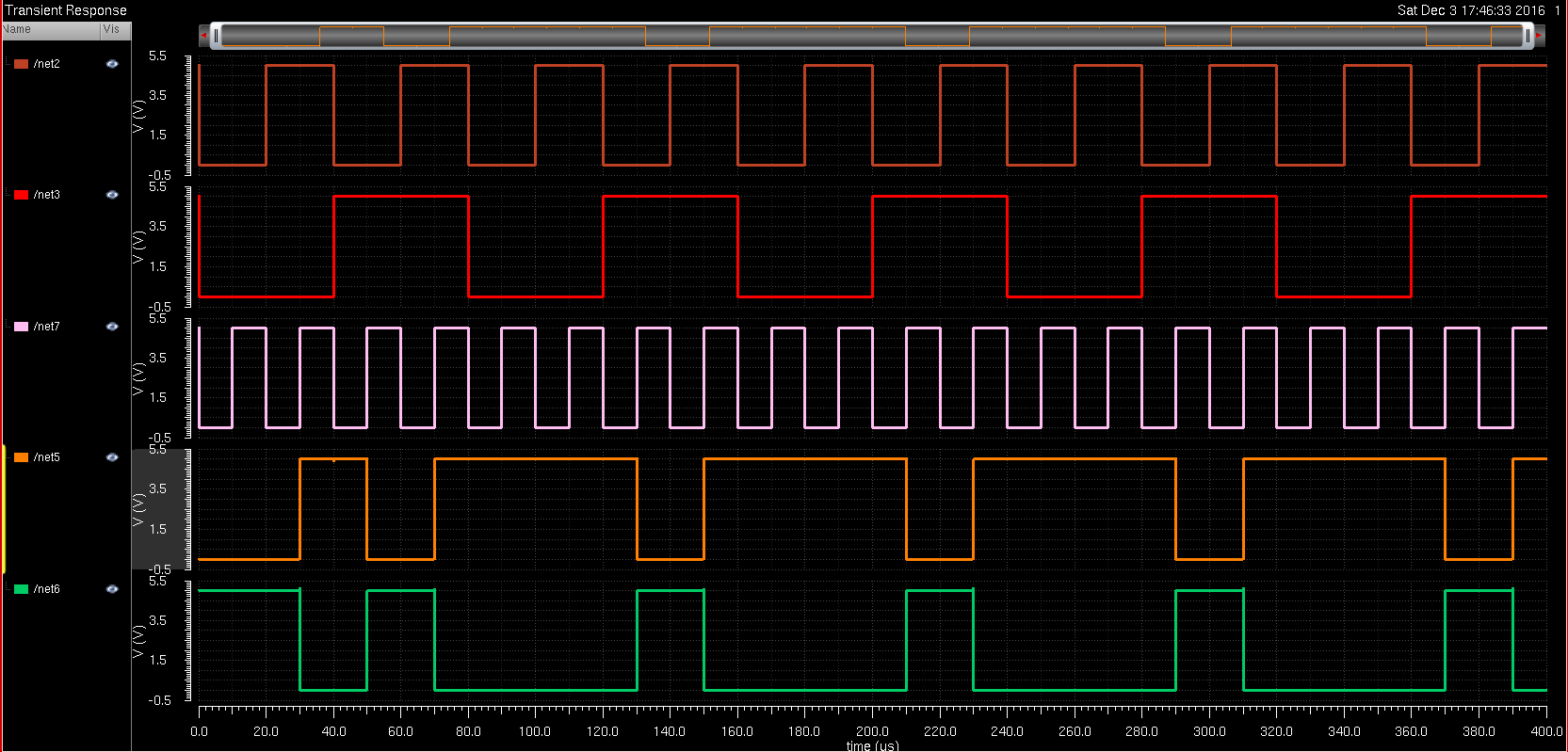


The **truth table** of a FF is as follows



Layout of the Flip Flop is as follows:

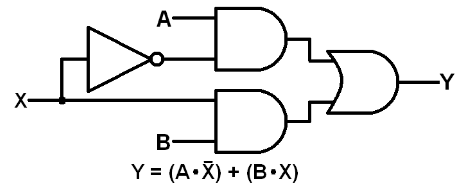
Upon simulation we get the following output which meets the truth table.



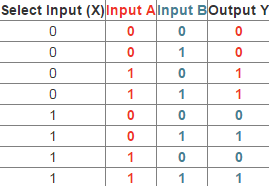
The order of the graph is as follows:

J,K,Clock,Q, Qnot

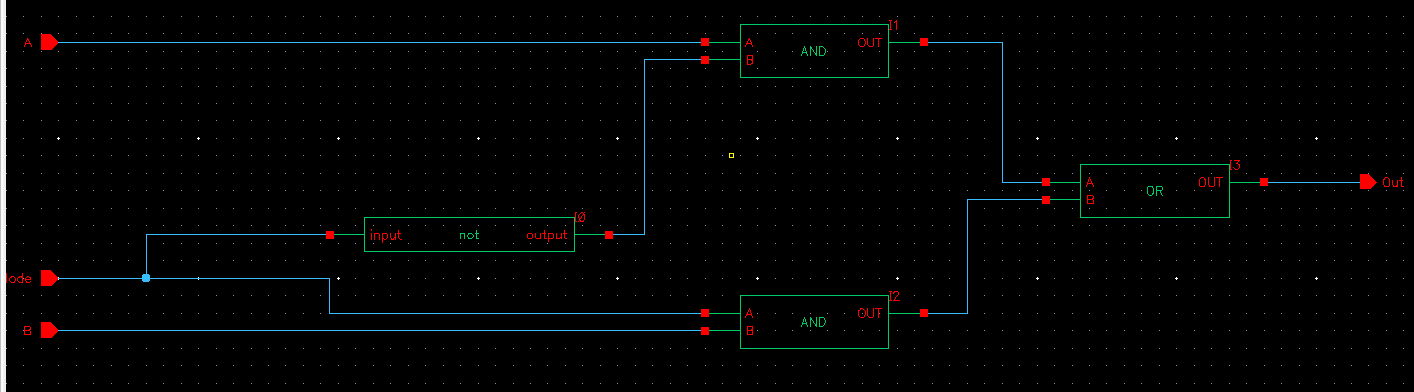
**2to1 Mux**



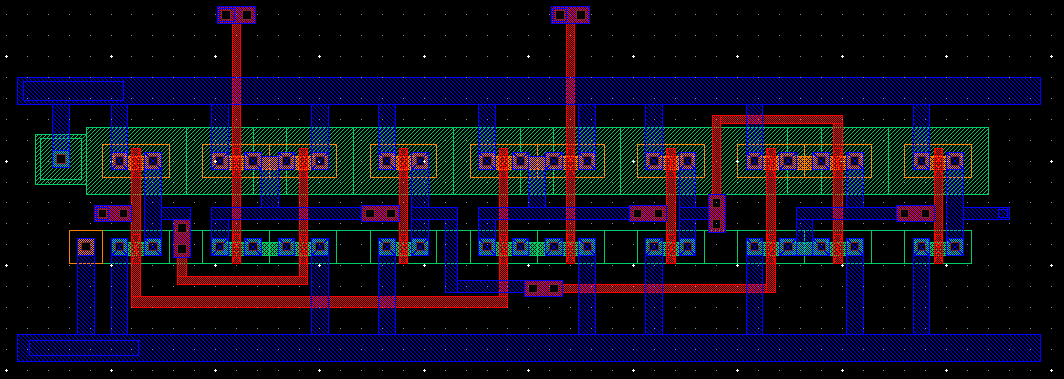
**Truth table:**



**Schematic:**

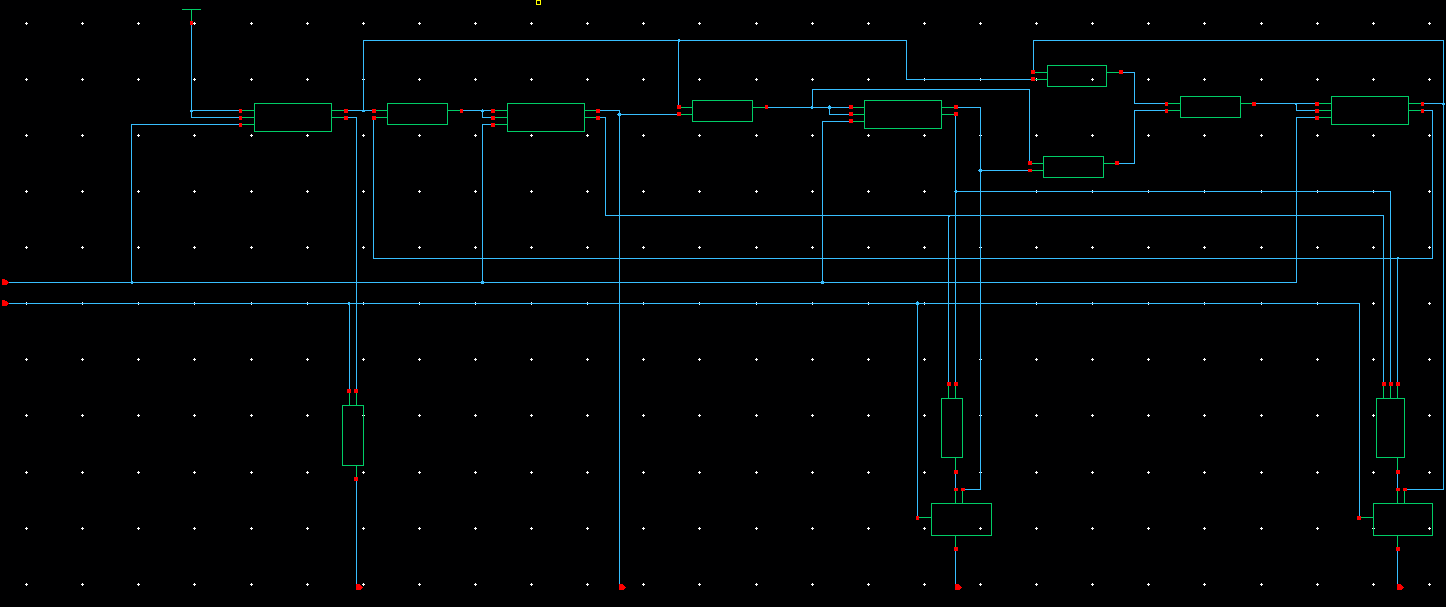


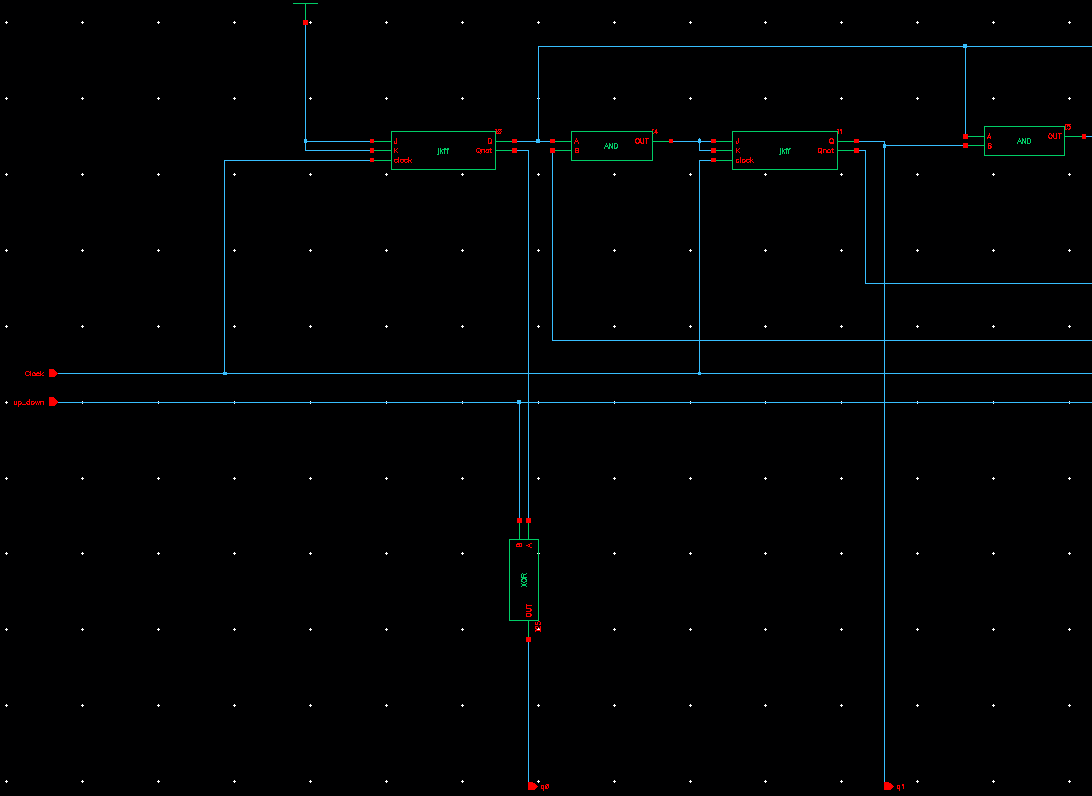
**Layout:**



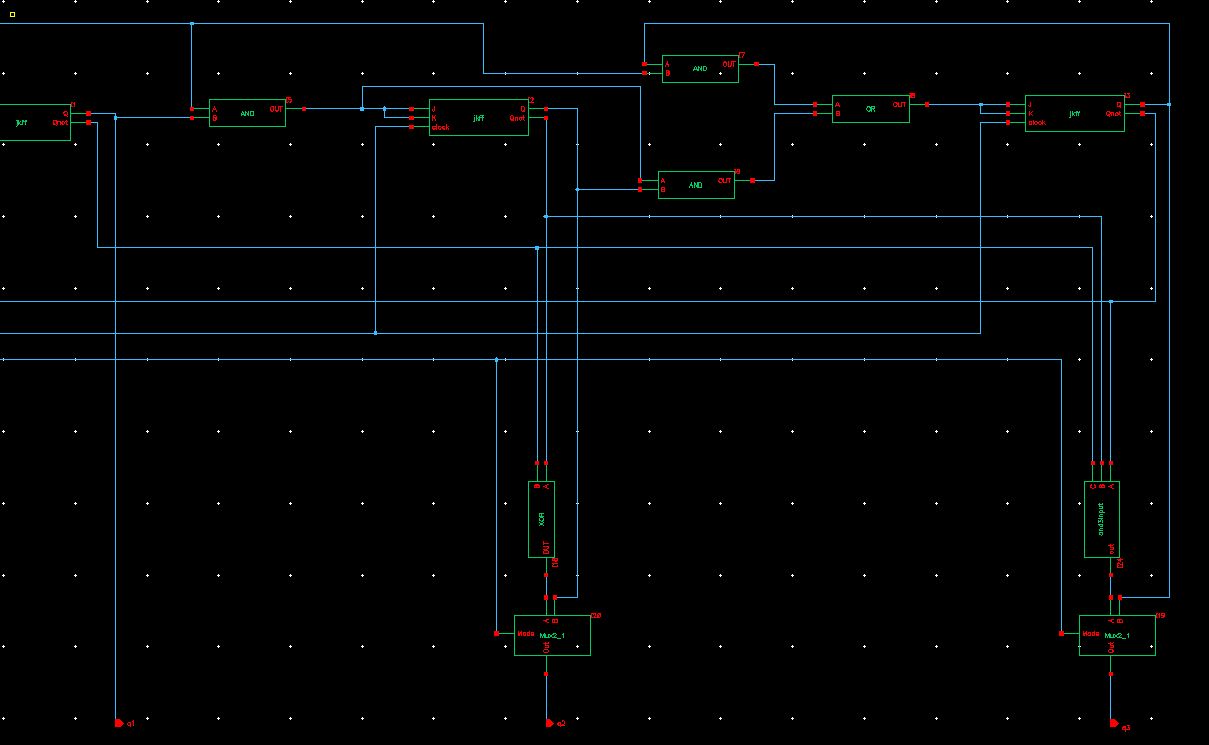
**UP down Counter Circuit:**

The top half of the graph does the computations and the bottom half of the circuit chooses between the mode of up and down. We have chosen by convention to keep Up as 1 to count upwards whereas we are going to make the counting down as mode 0.



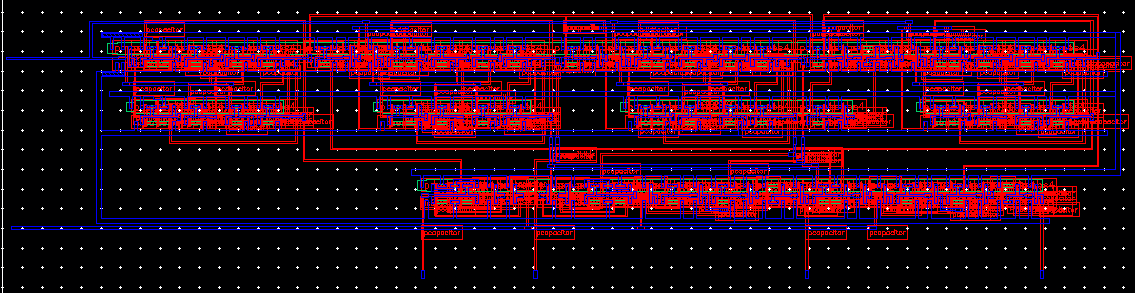


*Part1*



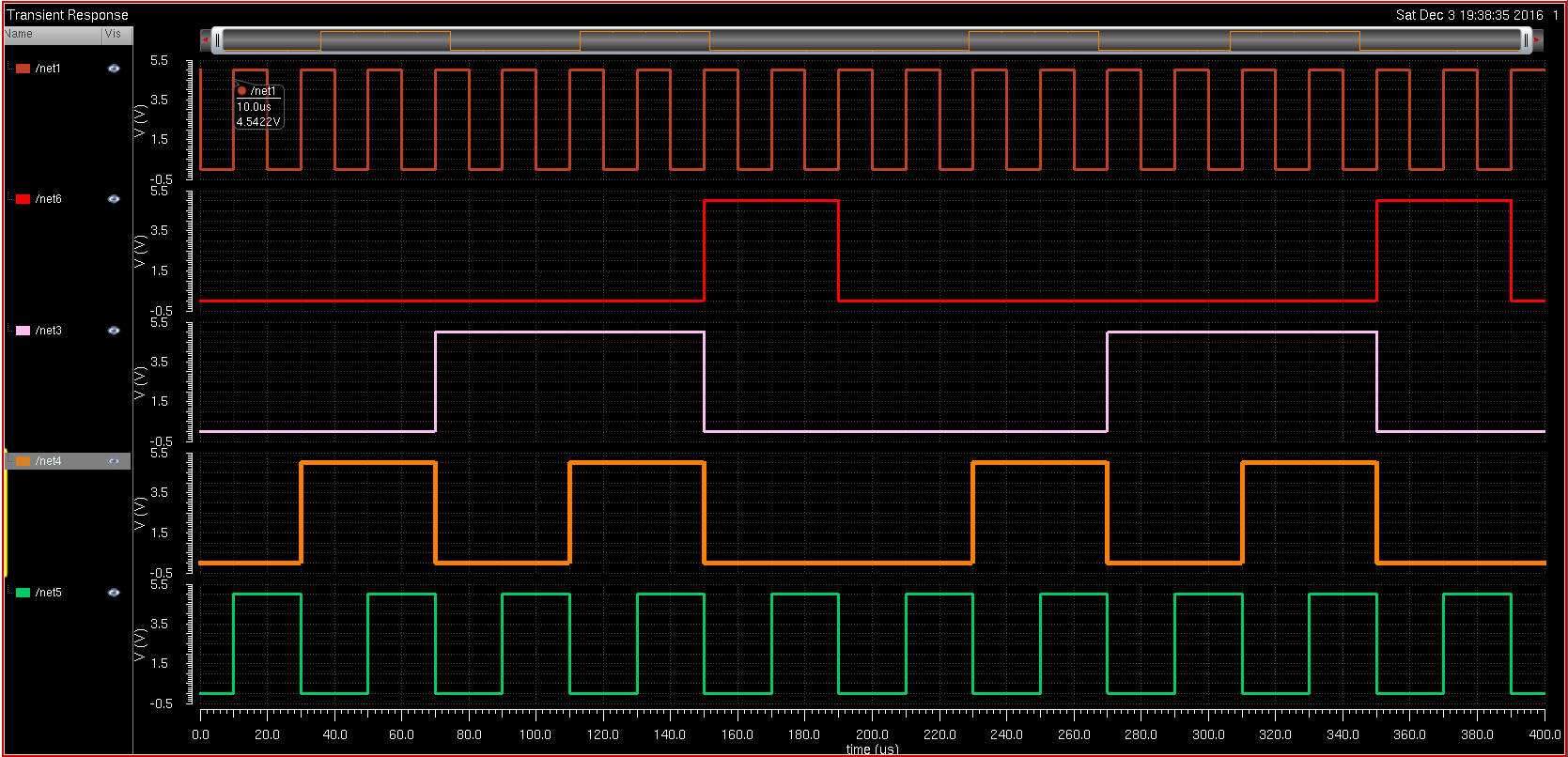
*Part2*

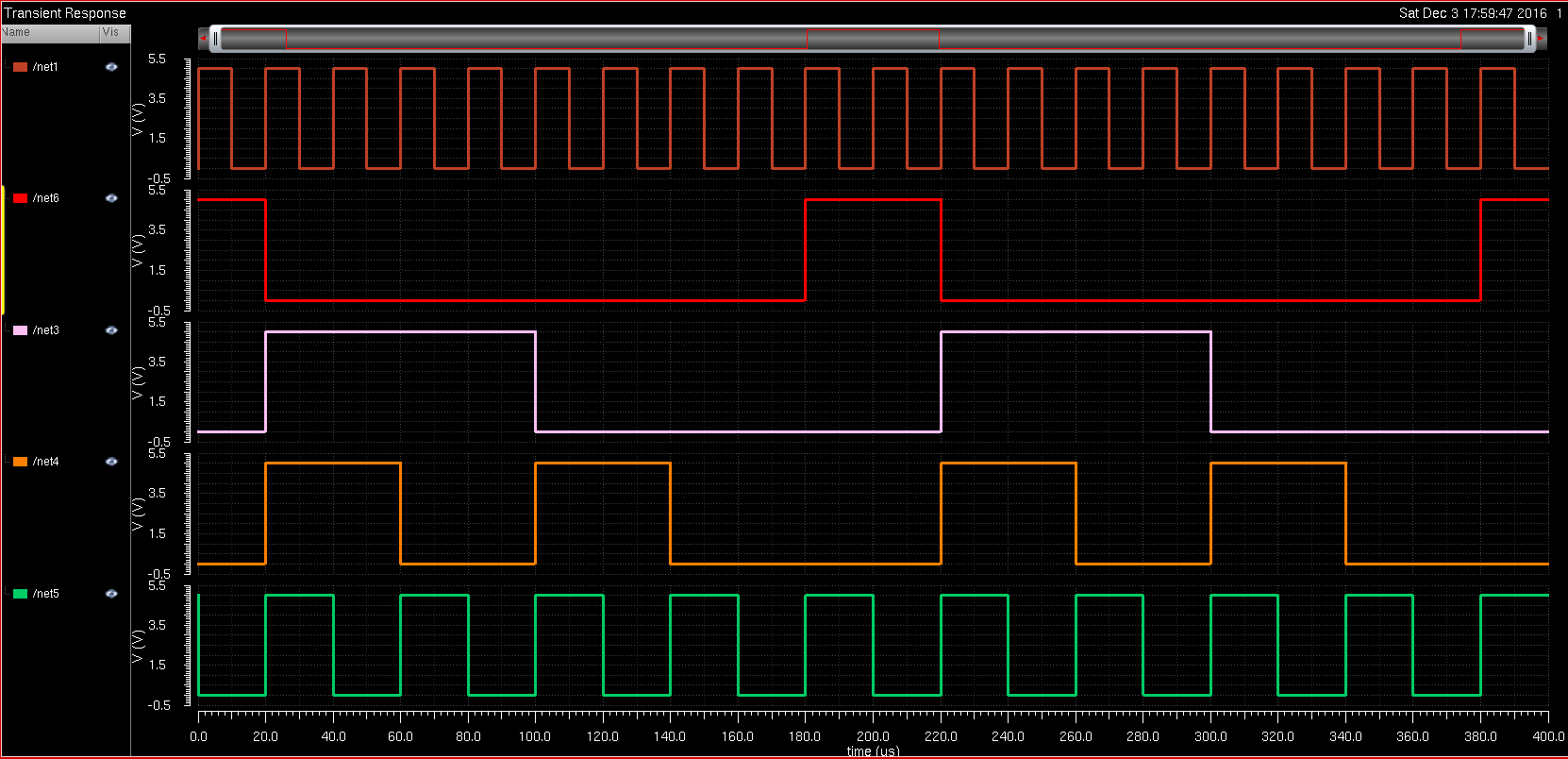
**Layout of the Up Down counter**



**Upon simulation we can look at our results:**

**Up counter:**



**Down Counter:**

It starts of at 1000 but we simulated it for longer to show that it goes the full loop.  
The middle of the graph u shall see 1001->1000 and so on so going from 9->8 and so on to 0.