

Experiment 3: *8x3 Encoder and 3x8 Decoder Implementation in VHDL.*

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Aim: Experiment-4: To implement 8x3 Encoder and 3x8 Decoder in VHDL.

❖ 8x3 Encoder:

The 8 to 3 Encoder or octal to Binary encoder consists of **8 inputs** : Y7 to Y0 and **3 outputs** : A2, A1 & A0. Each input line corresponds to each octal digit and three outputs generate corresponding binary code. The figure below shows the logic symbol of octal to binary encoder:



The truth table for 8 to 3 encoder is as follows :

INPUTS								OUTPUTS		
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	A2	A1	A0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

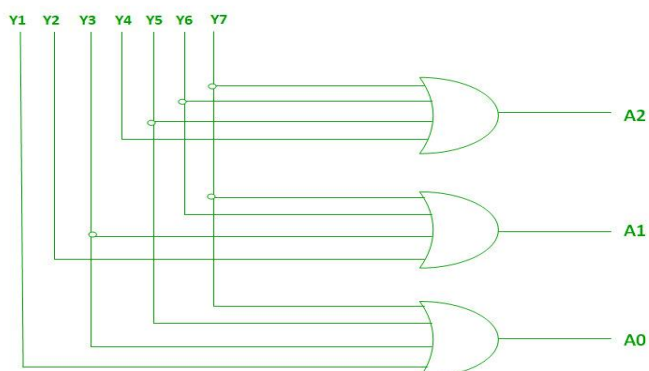
Logical expression for A2, A1 and A0 :

$$A2 = Y7 + Y6 + Y5 + Y4$$

$$A1 = Y7 + Y6 + Y3 + Y2$$

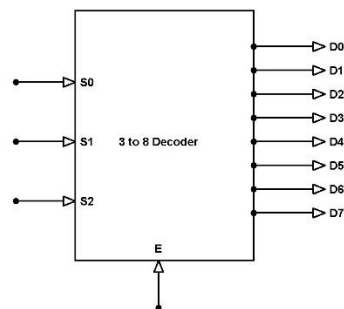
$$A0 = Y7 + Y5 + Y3 + Y1$$

The above two Boolean functions A2, A1 and A0 can be implemented using four input OR gates :



❖ 3x8 Decoder:

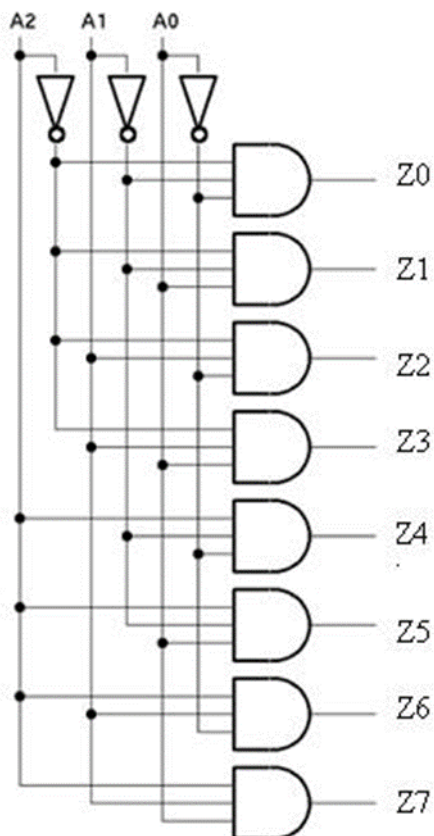
This decoder circuit gives 8 logic outputs for 3 inputs and has a enable pin. The circuit is designed with AND and NAND logic gates. It takes 3 binary inputs and activates one of the eight outputs. 3 to 8 line decoder circuit is also called as binary to an octal decoder.



3x8 Decoder Block Diagram

The decoder circuit works only when the Enable pin (E) is high. S0, S1 and S2 are three different inputs and D0, D1, D2, D3, D4, D5, D6, D7 are the eight outputs.

Circuit Diagram



3x8 Line Decoder Truth Table

The below table gives the truth table of 3 to 8 line decoder.

S0	S1	S2	E	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	0	0	0	1	0
0	1	0	1	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	1	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0

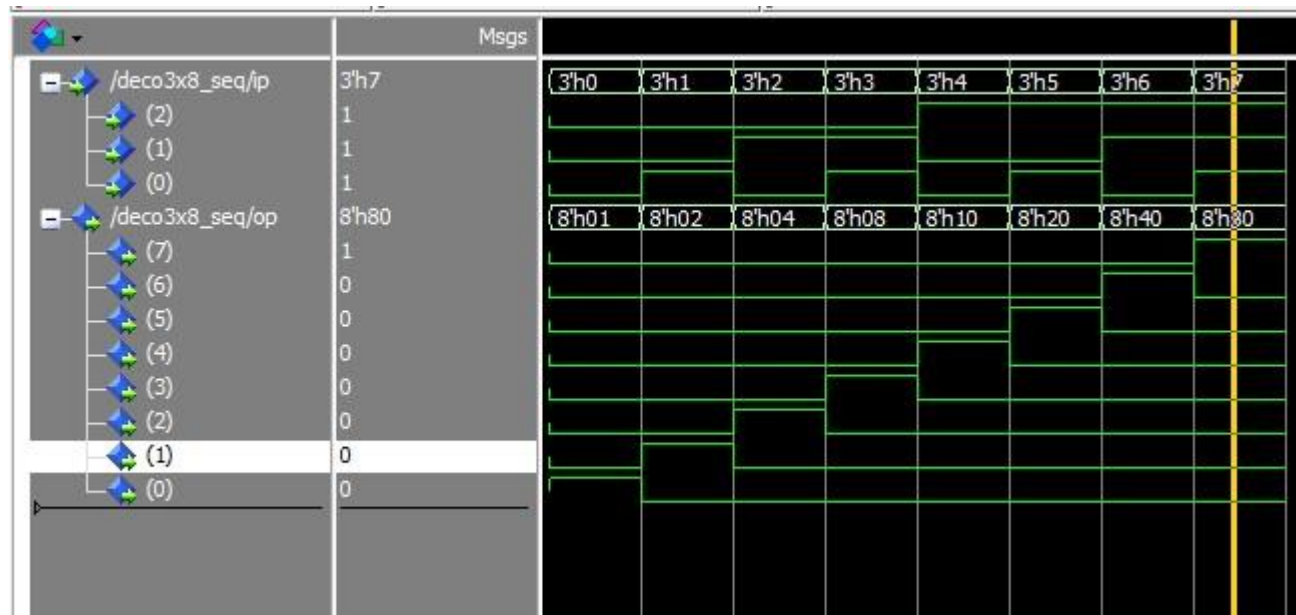
1	0	1	1	0	0	1	0	0	0	0	0
1	1	0	1	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

When the Enable pin (E) is low all the output pins are low.

❖ Waveform of 8x3 Encoder:



❖ Waveform of 3x8 Decoder:



❖ Result:

After performing the experiment, we understood the behaviour of 8x3 Encoder and 3x8 Decoder by digitally using VHDL code to run various operations, and with this behaviour we are able to draw the waveforms of the both 8x3 Encoder and 3x8 Decoder respectively.