Experiment 2: Half adder and Full adder Implementation in VHDL.

Digital Systems Design Lab

INDIAN INSTITUTE OF INFORMATION TECHNOLOGY SONEPAT

भारतीय सूचना प्रौद्योगिकी संस्थान, सोनीपत

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Submitted To:
Dr. Rajiv Verma
Assistant Professor
IIIT Sonepat

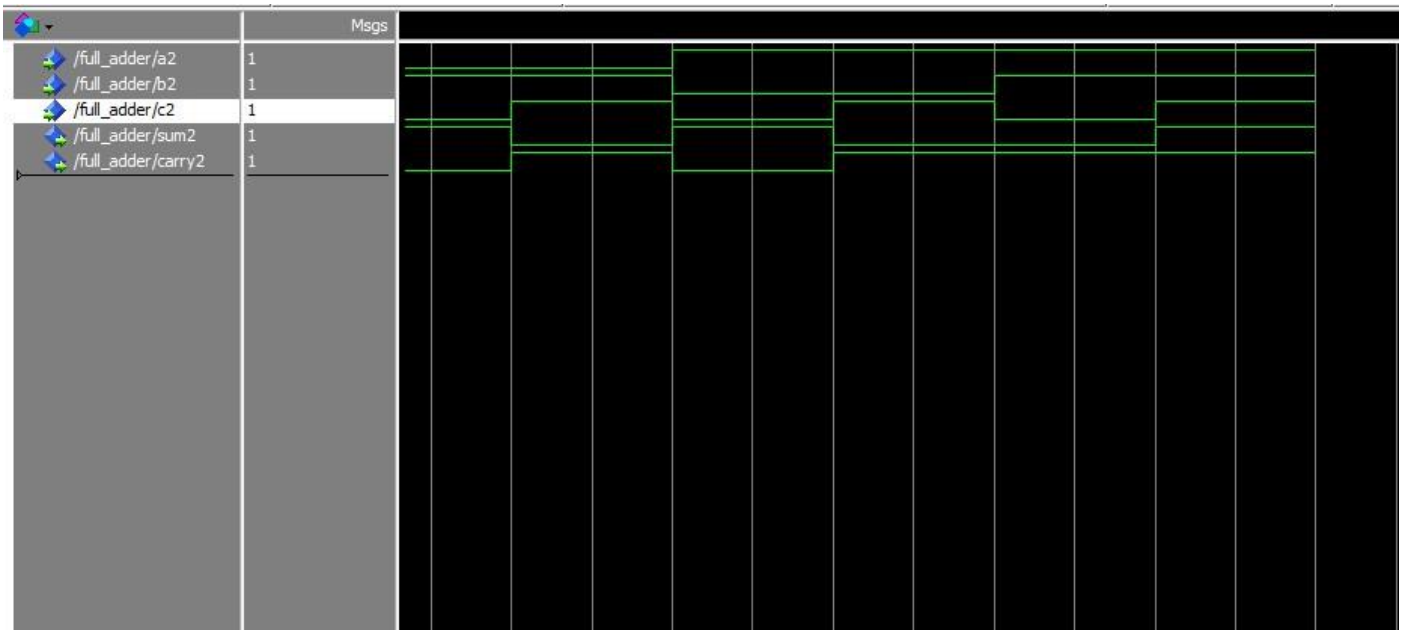
Submitted By:
Gaurav Yadav
CSE
11911038

❖VHDL Source Code for Half Adder and Full Adder:

```
--BY Gaurav Yadav | 11911038 | CSE
Library ieee;
use ieee.std_logic_1164.all;

entity half_adder is
  port(a1,b1:in bit;
       sum1,carry1:out bit);
end half_adder;
entity full_adder is
 port(a2,b2,c2:in bit;
          sum2,carry2:out bit);
end full_adder;

architecture data of full_adder is
begin
  sum2<= a2 xor b2 xor c2;
  carry2 <= ((a2 and b2) or (b2 and c2) or (a2 and c2));
end data;

architecture data of half_adder is
begin
  sum1<= a1 xor b1;
  carry1 <= a1 and b1;
end data;
```

❖Output Waveform of Half Adder:

❖ Output Waveform of Full Adder:



❖Result:

With the help of this experiment, we are able to understand the behaviour of half adder and full adder digitally.