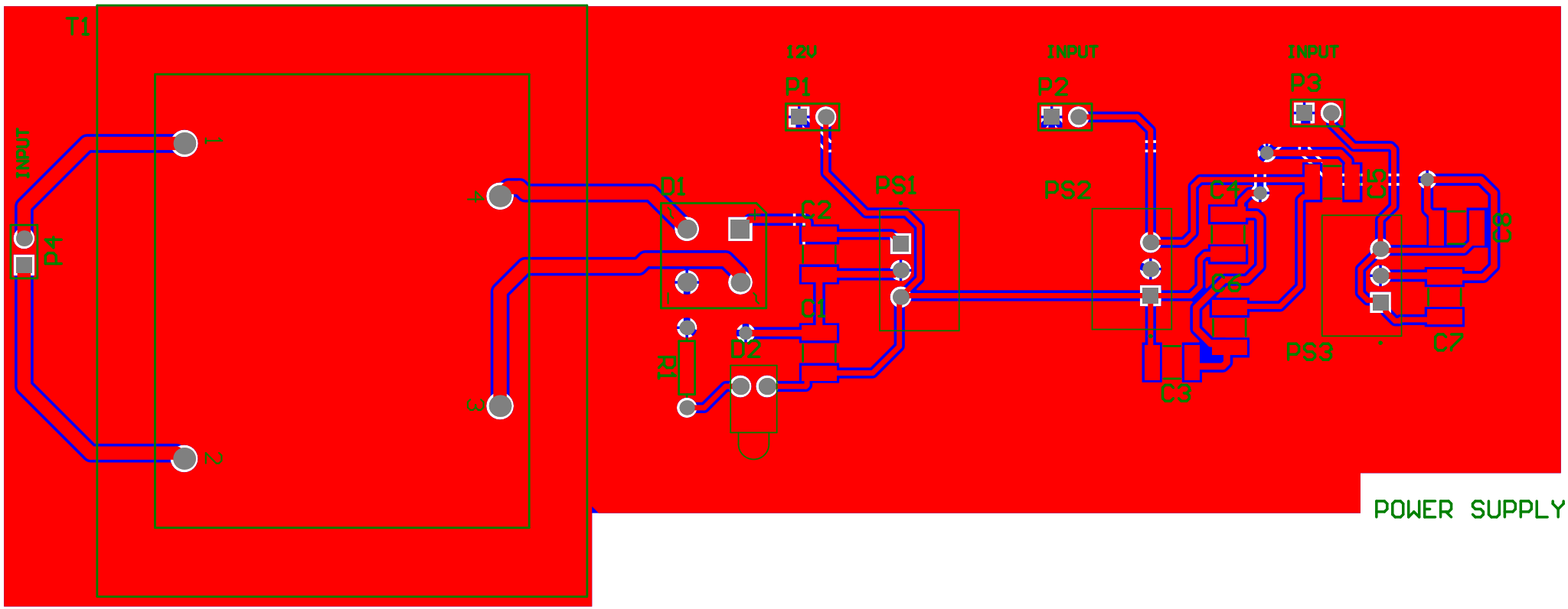
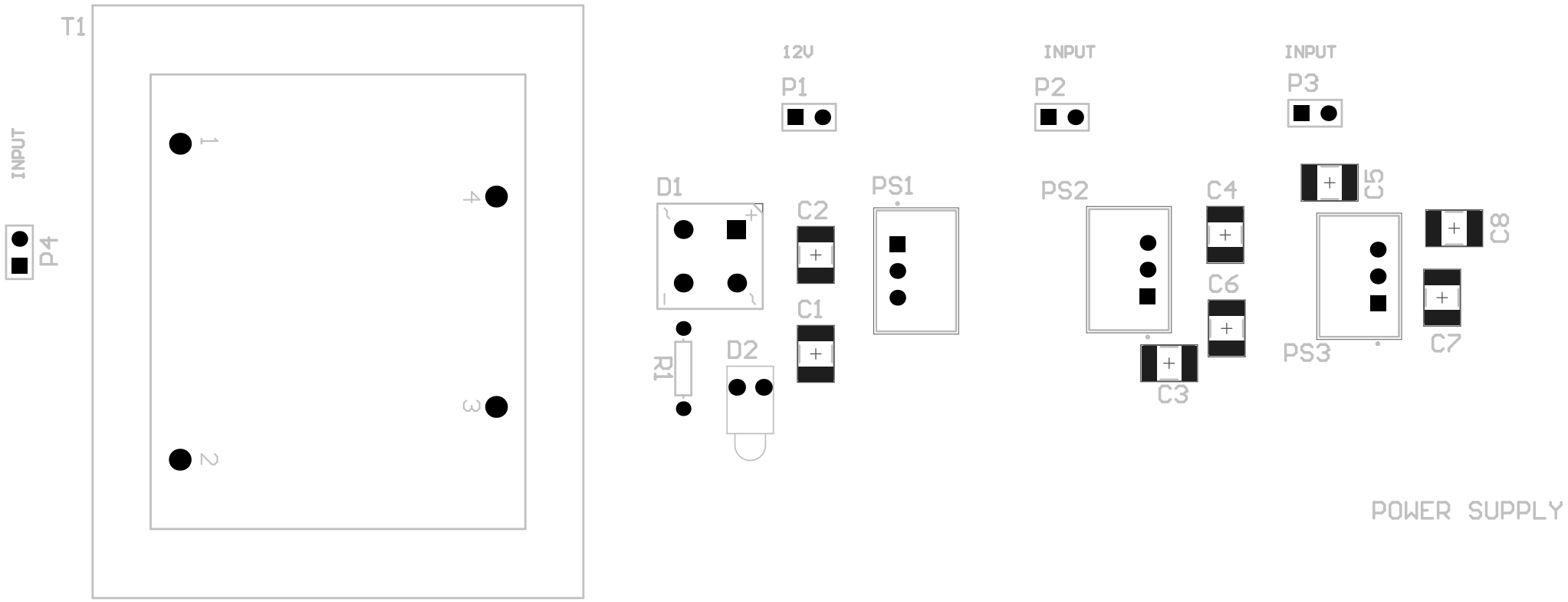

T1
INPUT
P4
1
2
3
4
12V
P1
D1
C2
PS1
D2
R1
INPUT
P2
PS2
C4
C5
C3
INPUT
P3
C6
C8
C7
PS3
POWER SUPPLY


T1
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P1
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P2
PS2
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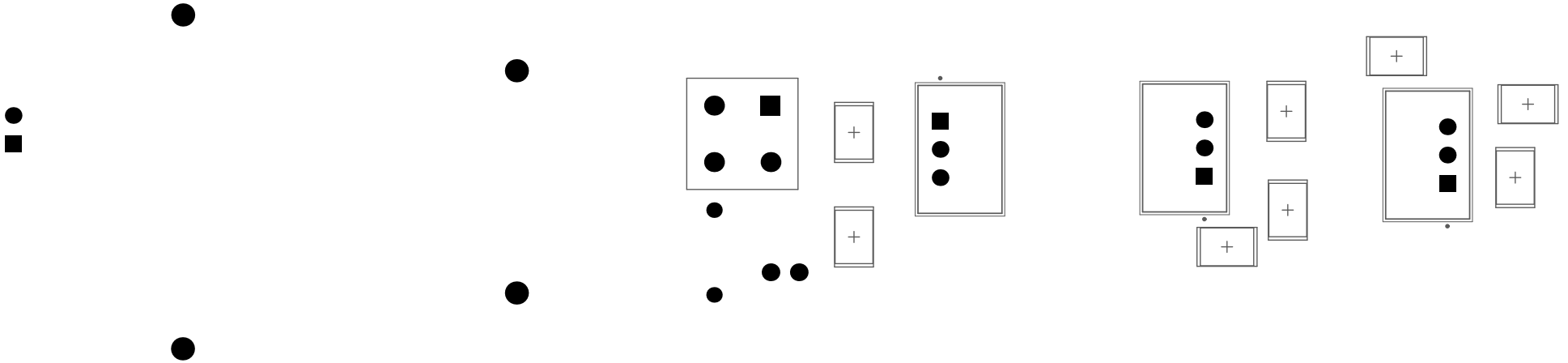
C6
C3
INPUT
P3
C5
C8
C7
PS3
POWER SUPPLY



# Component list

**Bill of Materials for Project [PCB 12-5-3v3.PrjPcb] (No PCB Document Selected)**

**Source Data From:** PCB 12-5-3v3.PrjPcb
**Project:** PCB 12-5-3v3.PrjPcb
**Variant:** None

Report Date: 11/10/2021 5:18 PM
Print Date: 11-Oct-21 5:18:27 PM

| Description | Footprint | Quantity | Designator | n Name Error:' Supplier Ord | olumn Name Error:' Manufacture | n Name Error:' Manufacturer Part N | n Name Error:' Supplier Unit | n Name Error:' Supplier Subtotal per | n Name Error:' Supplier Ord | n Name Error:' Manufa | n Name Error:' Manufacturer Part N | n Name Error:' Supplier Unit | n Name Error:' Supplier Cur | Total Price |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Polarized Capacitor (Surface Mount) | 1812 | 8 | C1, C2, C3, C4, C5, C6, C7, C8 | | | | | | | | | | | 0 |
| Full Wave Diode Bridge | D-38 | 1 | D1 | | | | | | | | | | | 0 |
| Typical RED GaAs LED | LED-1 | 1 | D2 | | | | | | | | | | | 0 |
| Header, 2-Pin | HDR1X2 | 1 | P1 | | | | | | | | | | | 0 |
| Header, 2-Pin | HDR1X2 | 1 | P2 | | | | | | | | | | | 0 |
| Header, 2-Pin | HDR1X2 | 1 | P3 | | | | | | | | | | | 0 |
| Header, 2-Pin | HDR1X2 | 1 | P4 | | | | | | | | | | | 0 |
| 0.5A DC/DC-Converter 'INNOLINE' SIP3 reg | CONV_R-7812-0.5 | 1 | PS1 | | | | | | | | | | | 0 |
| 0.5A DC/DC-Converter 'INNOLINE' SIP3 reg | CONV_R-7812-0.5 | 1 | PS2 | | | | | | | | | | | 0 |
| 0.5A DC/DC-Converter 'INNOLINE' SIP3 reg | CONV_R-7812-0.5 | 1 | PS3 | | | | | | | | | | | 0 |
| Resistor | AXIAL-0.3 | 1 | R1 | | | | | | | | | | | 0 |
| Transformer (ideal) | TRF_4 | 1 | T1 | | | | | | | | | | | 0 |

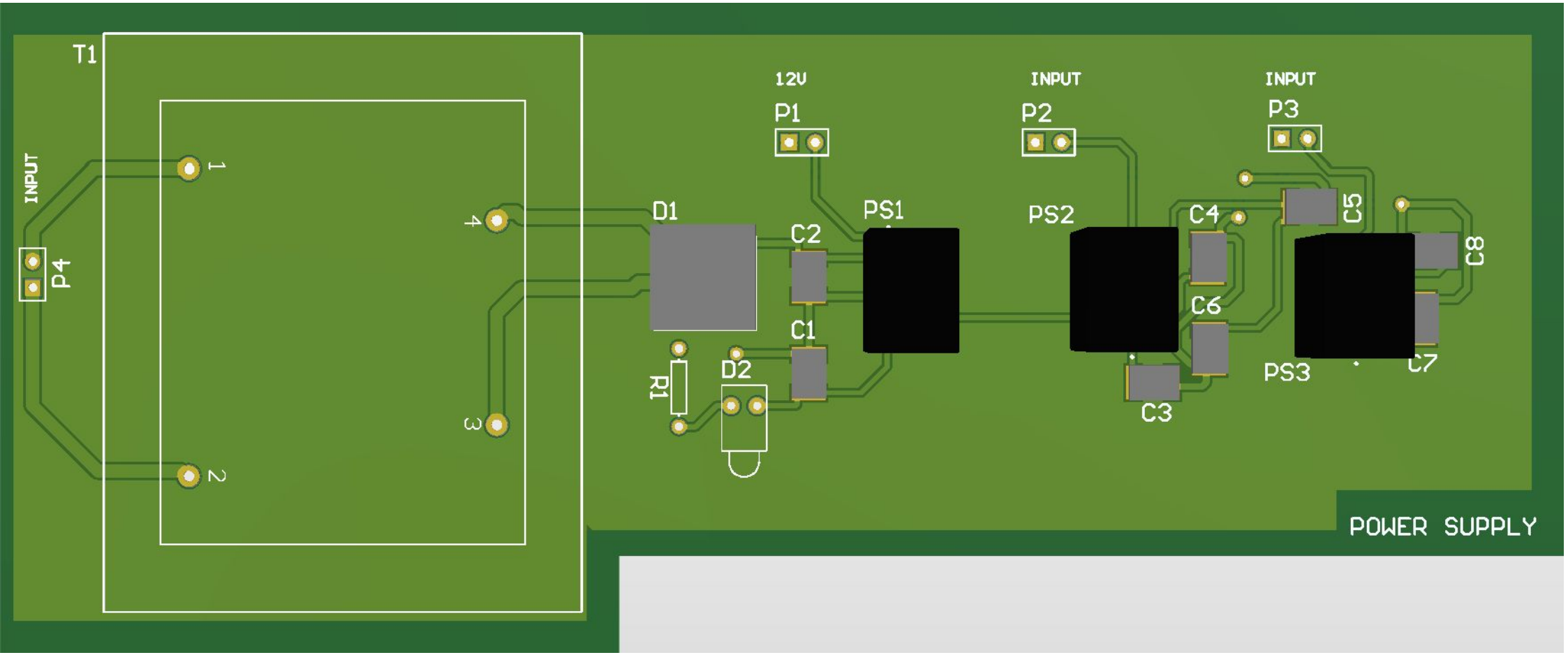
# Design Rules Verification Report

Filename : G:\Altium\Projects\MIssion_altium\PCB 12-5-3v3\PCB 12-5-3v3.PcbDoc

Warnings 0
Rule Violations 0

| Warnings | |
|---|---|
| Total | 0 |

| Rule Violations | |
|---|---|
| Clearance Constraint (Gap=10mil) (All),(All) | 0 |
| Short-Circuit Constraint (Allowed=No) (All),(All) | 0 |
| Un-Routed Net Constraint ( (All) ) | 0 |
| Modified Polygon (Allow modified: No), (Allow shelved: No) | 0 |
| Width Constraint (Min=10mil) (Max=50mil) (Preferred=40mil) (All) | 0 |
| Width Constraint (Min=10mil) (Max=50mil) (Preferred=30mil) (All) | 0 |
| Power Plane Connect Rule(Relief Connect )(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4) | 0 |
| Hole Size Constraint (Min=1mil) (Max=100mil) (All) | 0 |
| Hole To Hole Clearance (Gap=10mil) (All),(All) | 0 |
| Minimum Solder Mask Sliver (Gap=1mil) (All),(All) | 0 |
| Silk To Solder Mask (Clearance=1mil) (IsPad),(All) | 0 |
| Silk to Silk (Clearance=5mil) (All),(All) | 0 |
| Net Antennae (Tolerance=0mil) (All) | 0 |
| Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All) | 0 |
| Total | 0 |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PS2
C4
C6
C3
INPUT
P3
C5
C8
PS3
C7
POWER SUPPLY