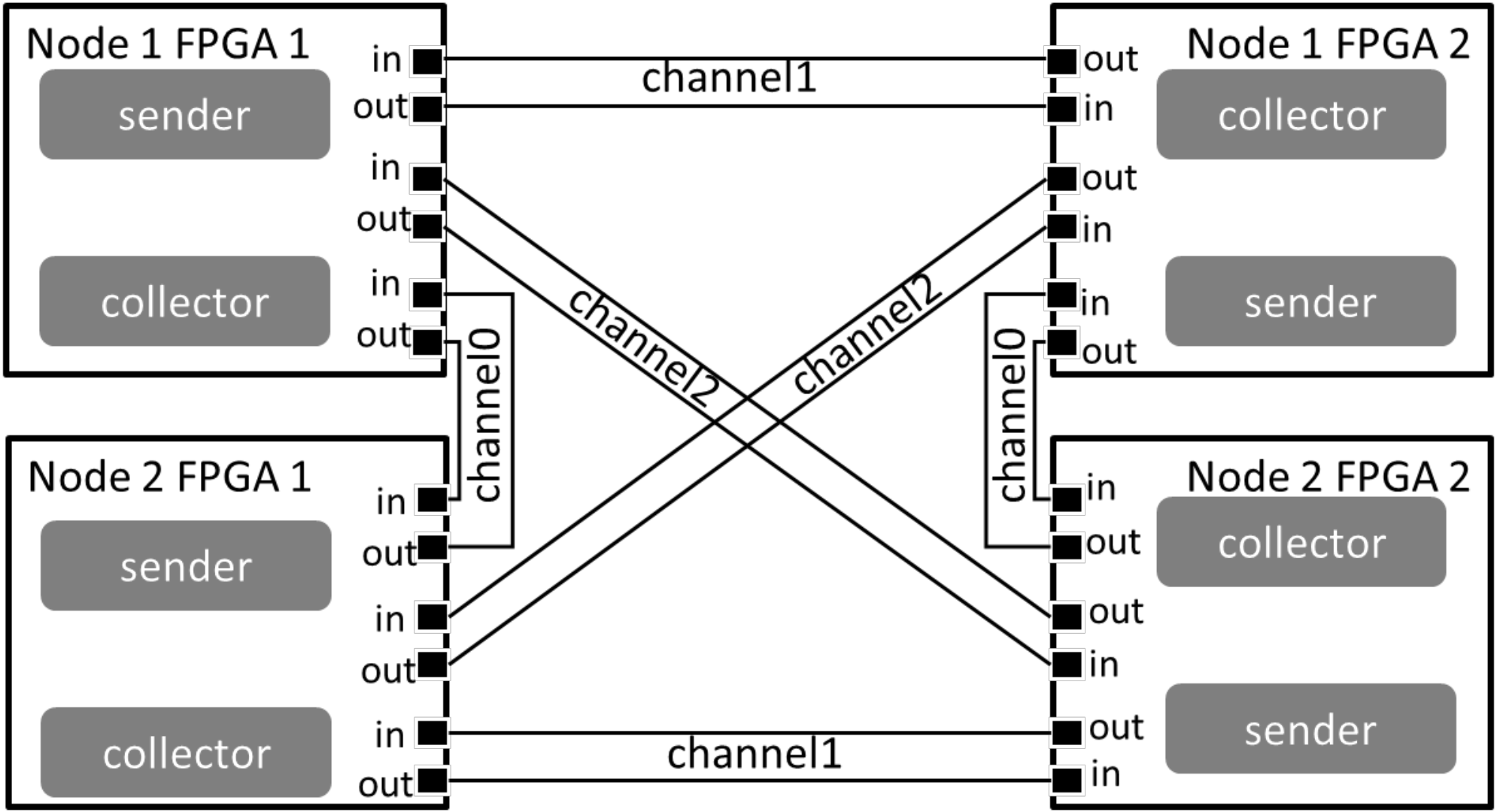
Node 1 FPGA 1
sender
collector
in
out
in
out
in
out
channel1
channel2
channel0
Node 1 FPGA 2
collector
sender
out
in
out
in
in
out
Node 2 FPGA 1
sender
collector
in
out
in
out
in
out
channel1
Node 2 FPGA 2
collector
sender
in
out
out
in
out
in