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What optimizations can be added to improve performance?

Removing the functionality of JAL instruction where it stores the PC+4 in a Register, I saw that other architectures simply change the PC with a MUX, bypassing any other operations through ALU, Register File, etc. This could be a massive speed up.

Additionally, the addition hardcoded control bits, for example, the BNE instruction uses the funct3 to differentiate between BNE and BEQ, I noticed that we could possibly input more parts of the instruction into the Control unit, and then we could have simple logic gates (NOT) to switch between BNE and BEQ, combined with a control bit specifically to trigger the BNE logic. Passing some of the logic to simpler components, could mean a potential speedup.