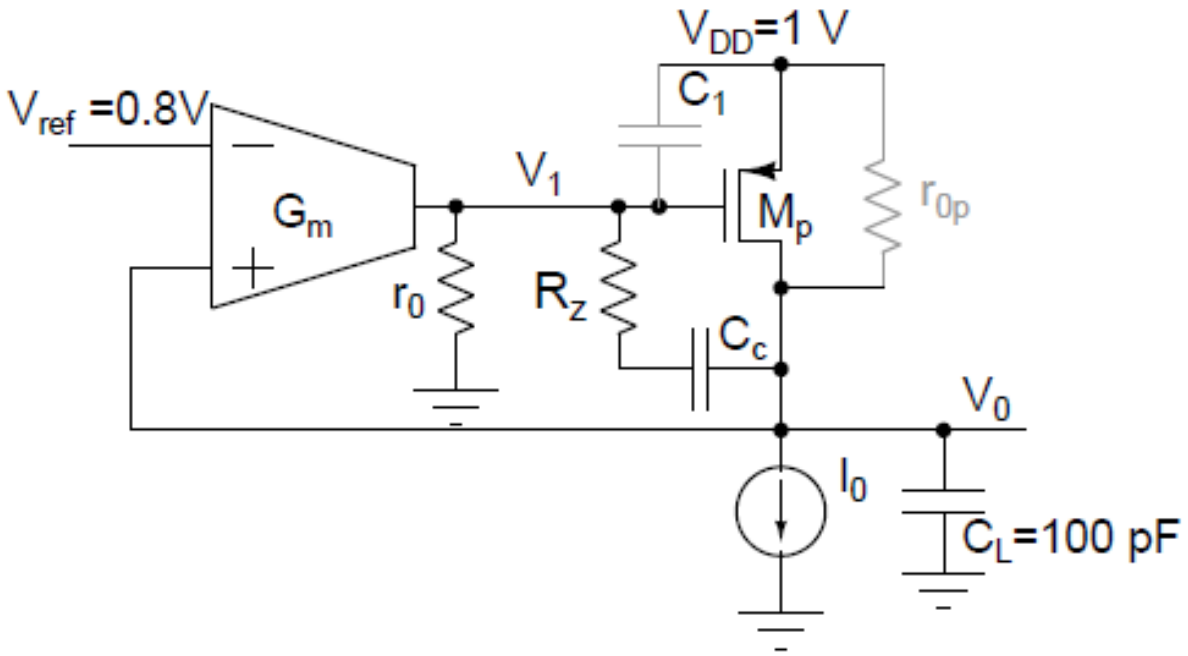
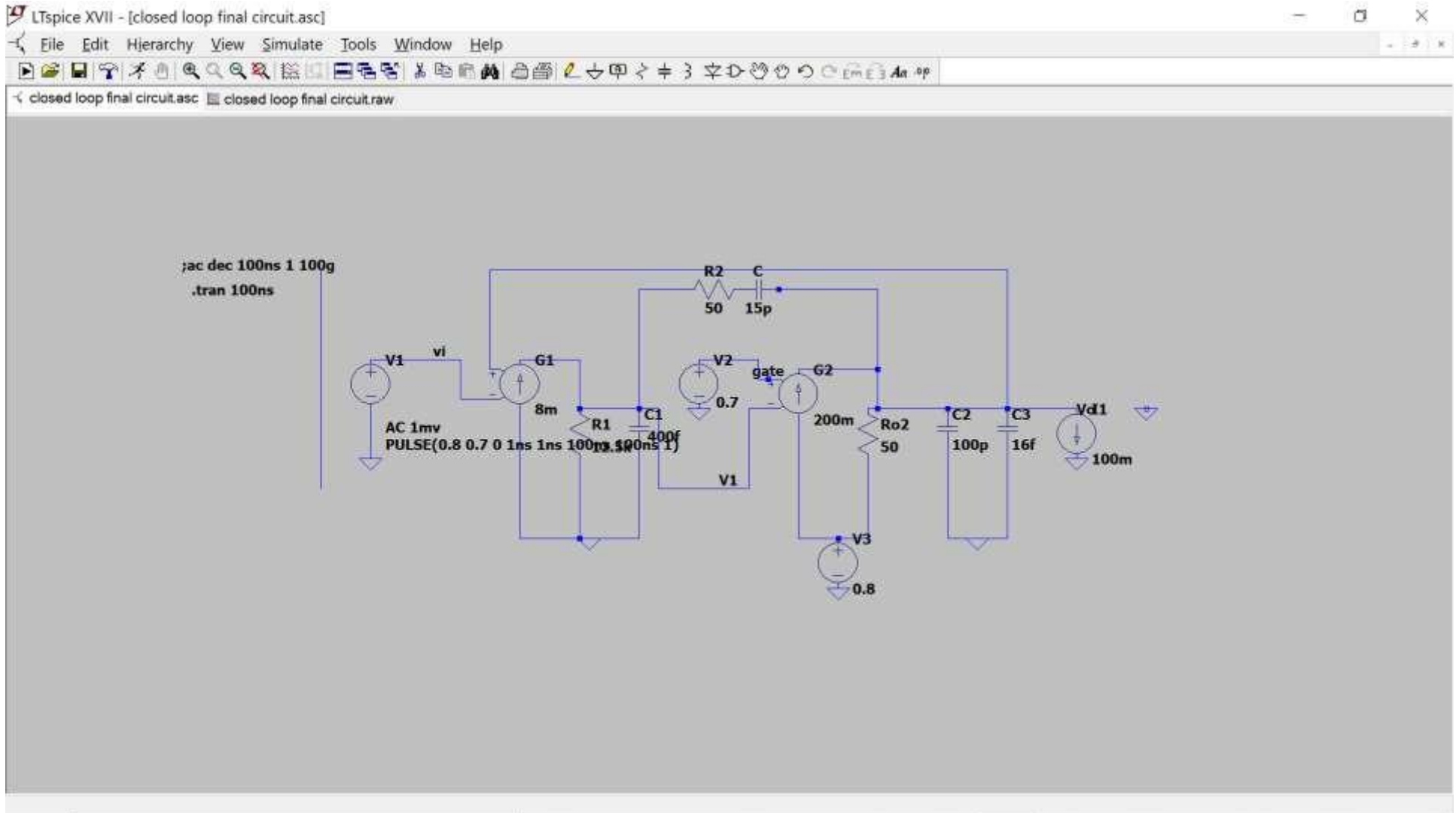
Low-drop-out (LDO) voltage regulator

Gaurav Pandey
MVLSI
Department of Electrical Engineering
Indian Institute of Technology, Kanpur

Block Diagram



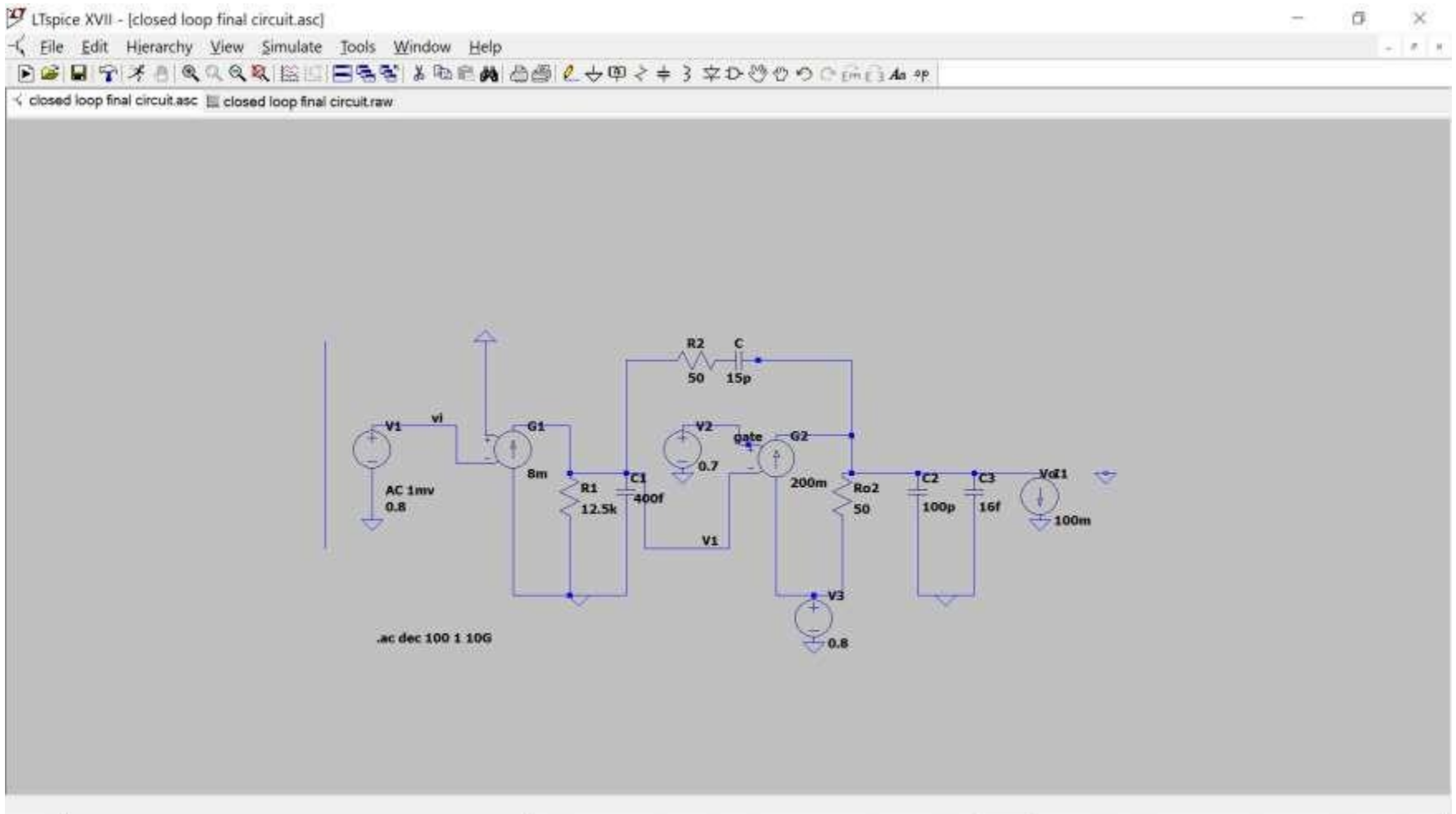
Q1. A step response

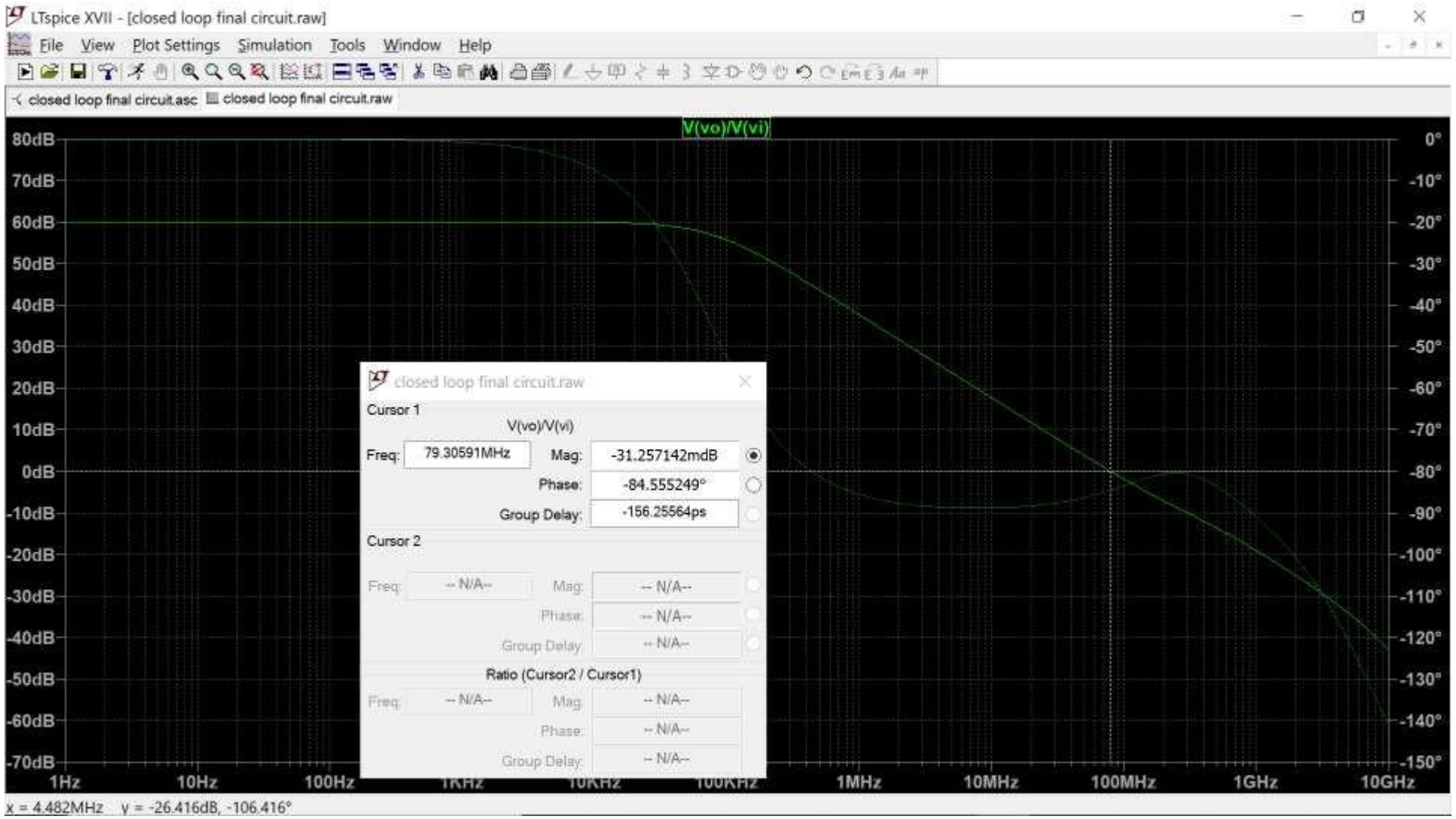



LTspice XVII - [closed loop final circuit.raw]
File View Plot Settings Simulation Tools Window Help
closed loop final circuit.asc
closed loop final circuit.raw
V(v1)
228mV
225mV
222mV
219mV
216mV
213mV
210mV
207mV
204mV
201mV
198mV
V(vo)
V(vi)
810mV
800mV
790mV
780mV
770mV
760mV
750mV
740mV
730mV
720mV
710mV
700mV
690mV
0ns
10ns
20ns
30ns
40ns
50ns
60ns
70ns
80ns
90ns
100ns
x = 28.06ns y = 212.20mV

B.

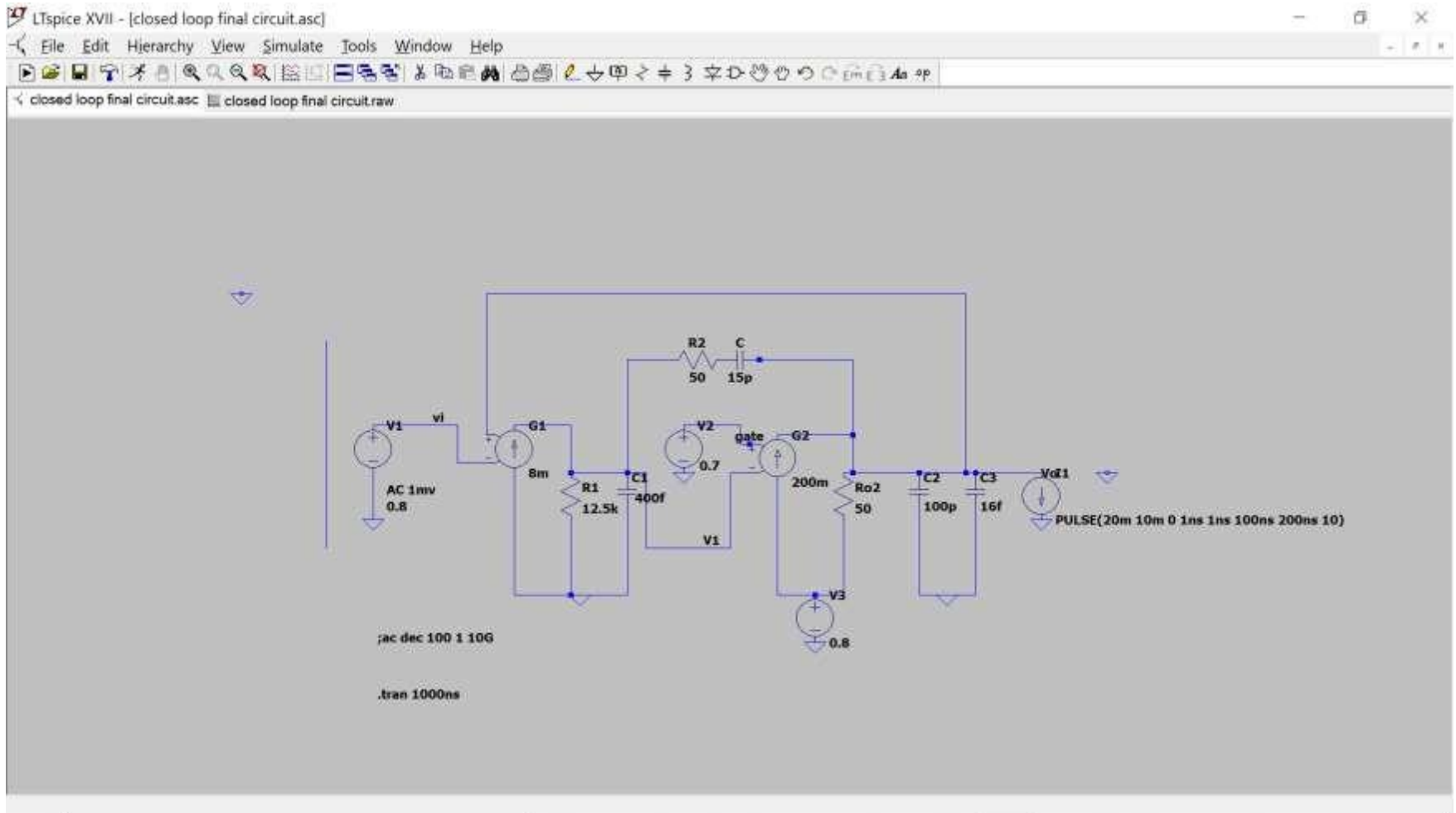
Frequency response




LTspice XVII - [closed loop final circuit.raw]
File View Plot Settings Simulation Tools Window Help
closed loop final circuit.asc
closed loop final circuit.raw
V(vo)/V(vi)
80dB 70dB 60dB 50dB 40dB 30dB 20dB 10dB 0dB -10dB -20dB -30dB -40dB -50dB -60dB -70dB
0° -10° -20° -30° -40° -50° -60° -70° -80° -90° -100° -110° -120° -130° -140° -150°
1Hz 10Hz 100Hz 1KHz 10KHz 100KHz 1MHz 10MHz 100MHz 1GHz 10GHz
closed loop final circuit.raw
Cursor 1
V(vo)/V(vi)
Freq: 79.30591MHz
Mag: -31.257142mdB
Phase: -84.555249°
Group Delay: -156.25564ps
Cursor 2
Freq: -- N/A--
Mag: -- N/A--
Phase: -- N/A--
Group Delay: -- N/A--
Ratio (Cursor2 / Cursor1)
Freq: -- N/A--
Mag: -- N/A--
Phase: -- N/A--
Group Delay: -- N/A--
x = 4.482MHz y = -26.416dB, -106.416°

c.

Pulse response

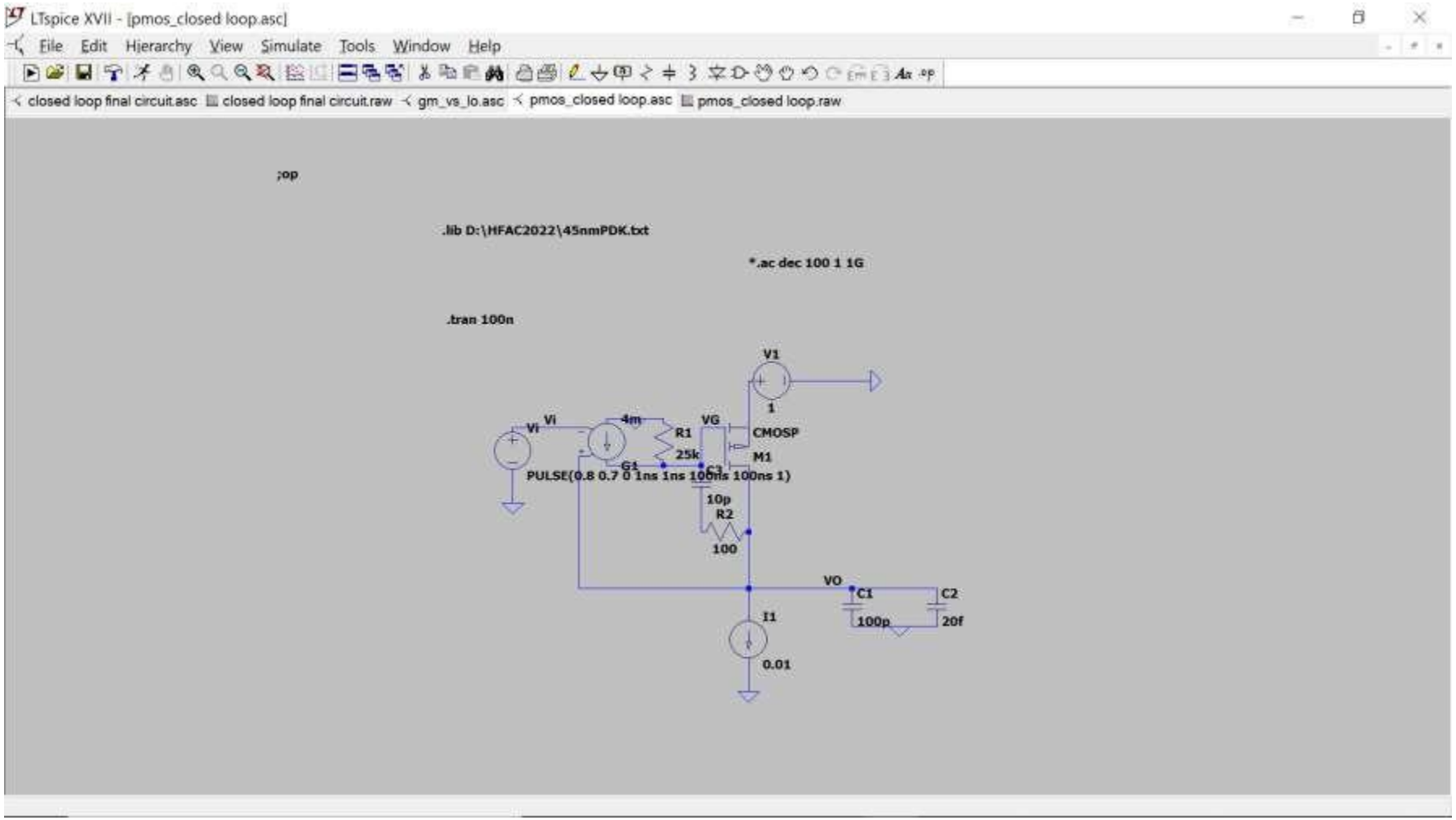


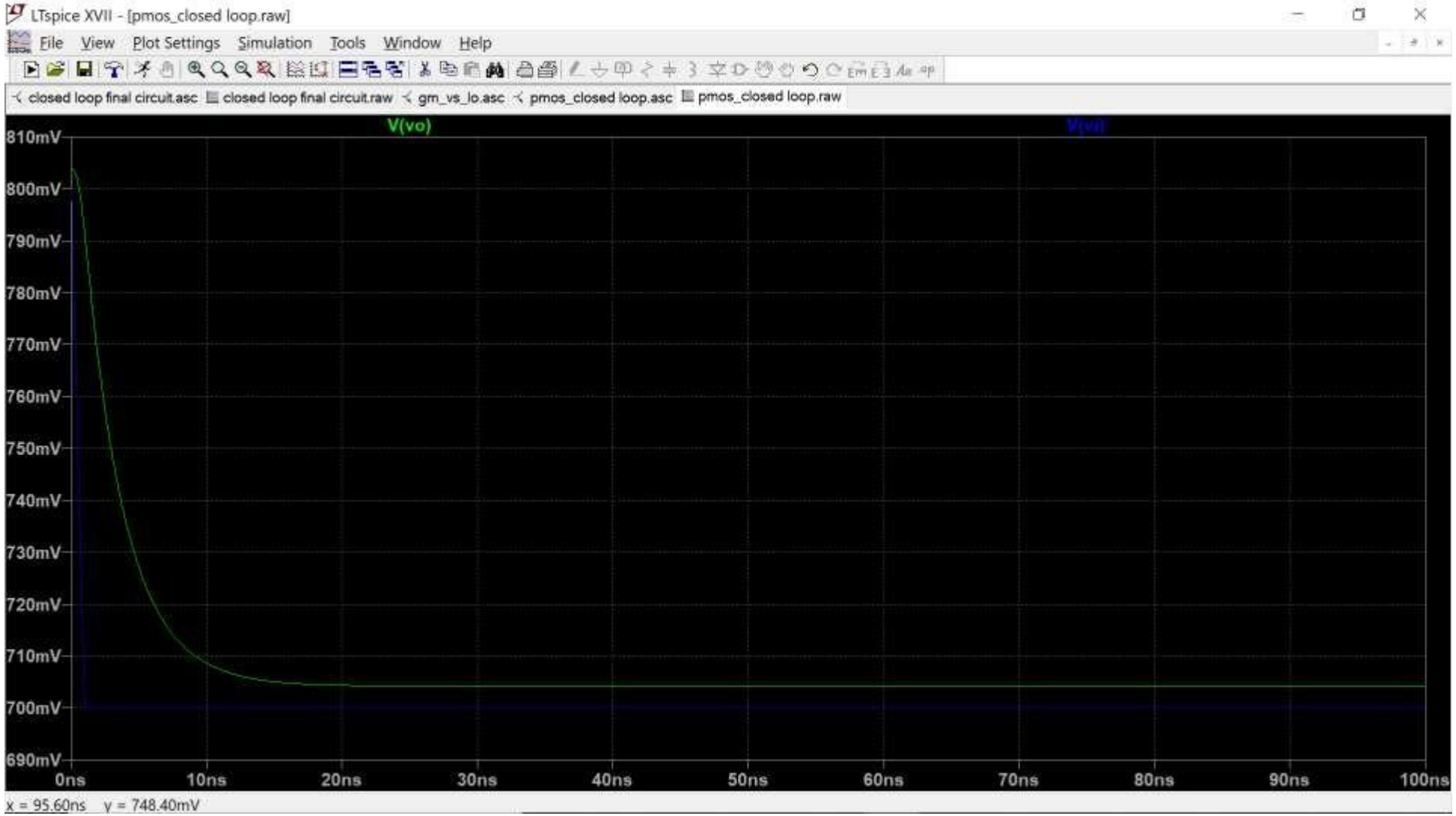

LTspice XVII - [closed loop final circuit.raw]
File View Plot Settings Simulation Tools Window Help
closed loop final circuit.asc
closed loop final circuit.raw
V(vo)
I(I1)
835mV
830mV
825mV
820mV
815mV
810mV
805mV
800mV
795mV
790mV
785mV
780mV
775mV
20mA
19mA
18mA
17mA
16mA
15mA
14mA
13mA
12mA
11mA
10mA
9mA
0.0µs
0.1µs
0.2µs
0.3µs
0.4µs
0.5µs
0.6µs
0.7µs
0.8µs
0.9µs
1.0µs
x = 0.862µs y = 817.20mV, 17.44mA

Q2. A step response

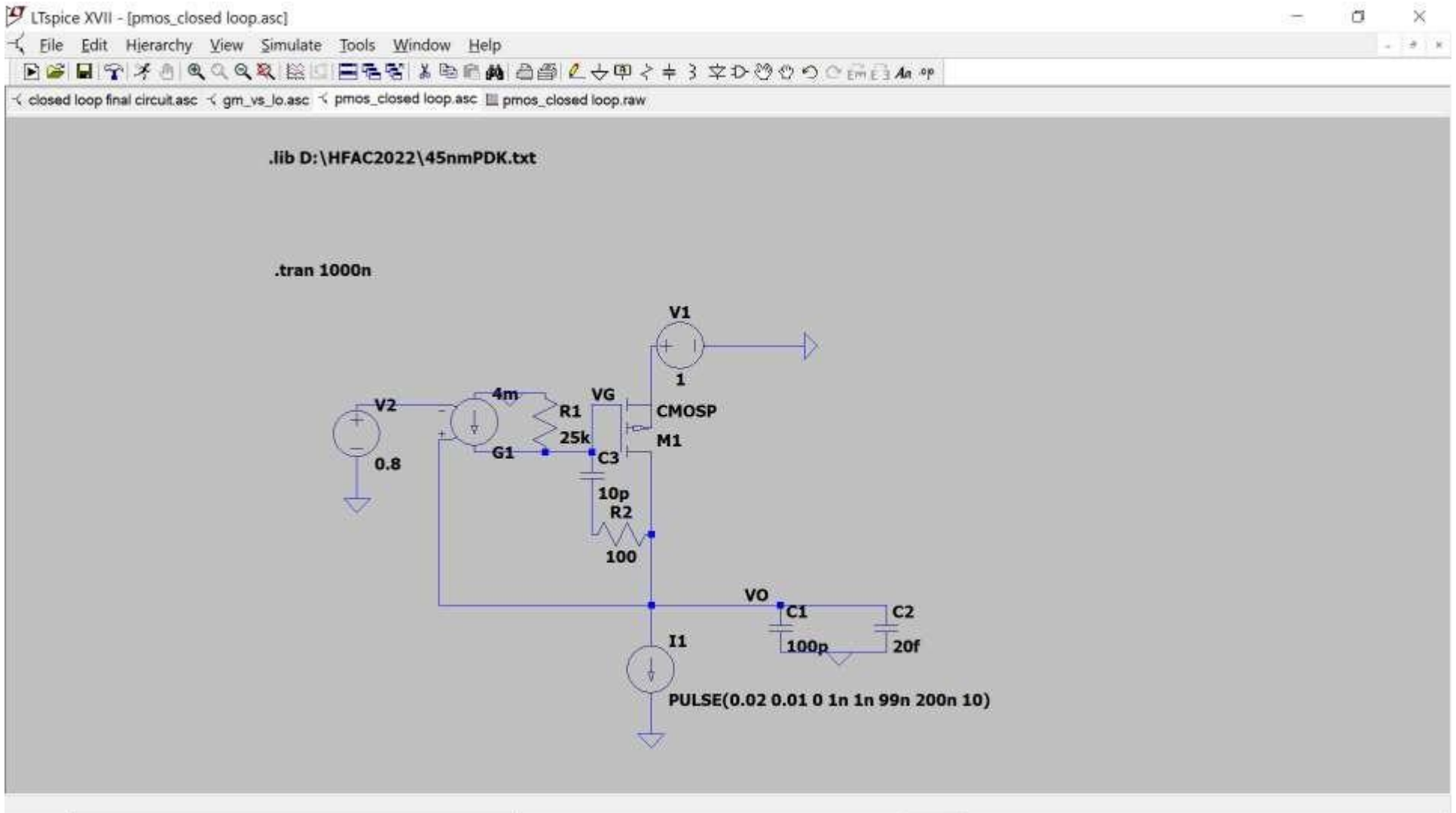
pmos width =400u

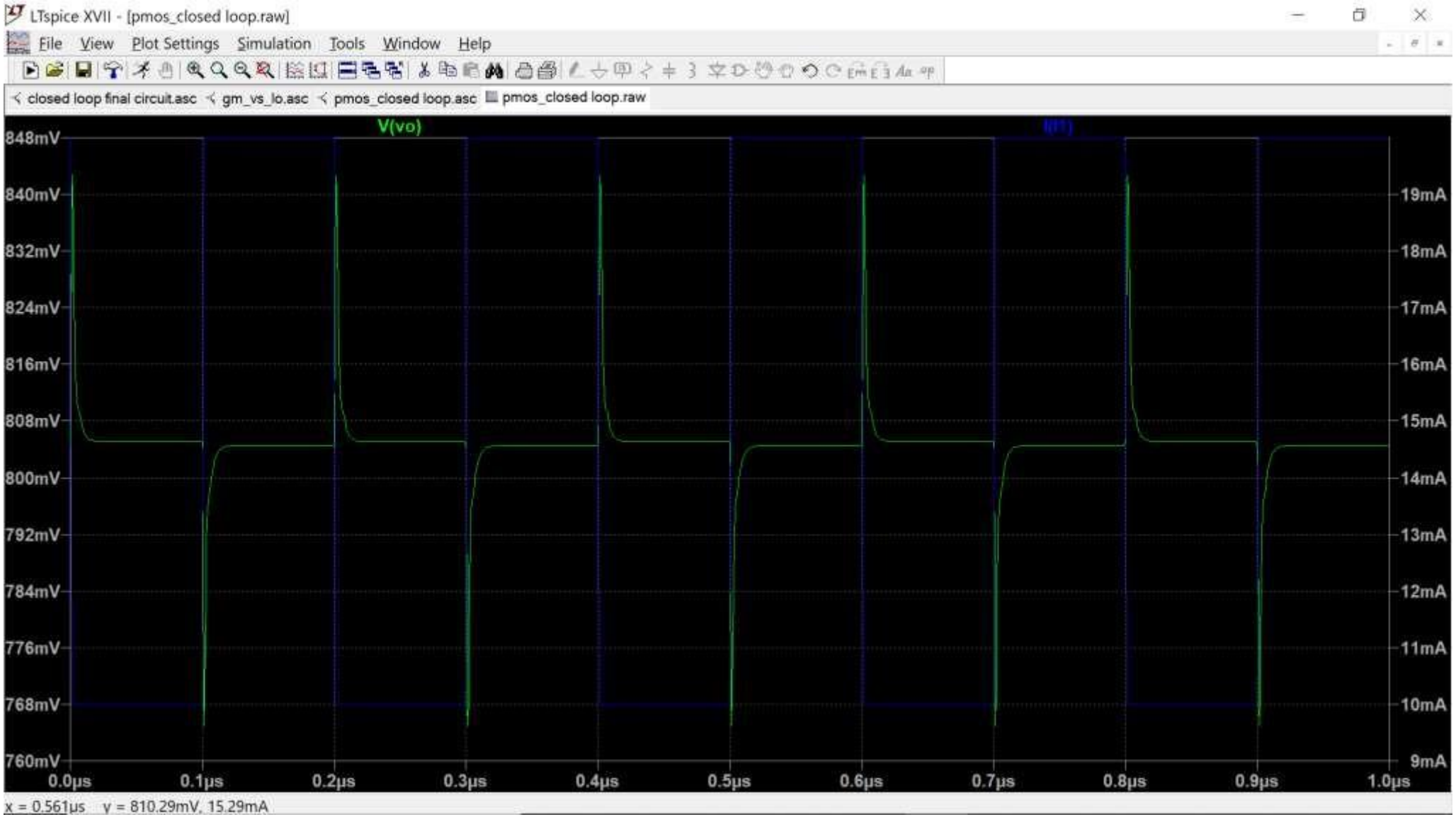
gm=355mS



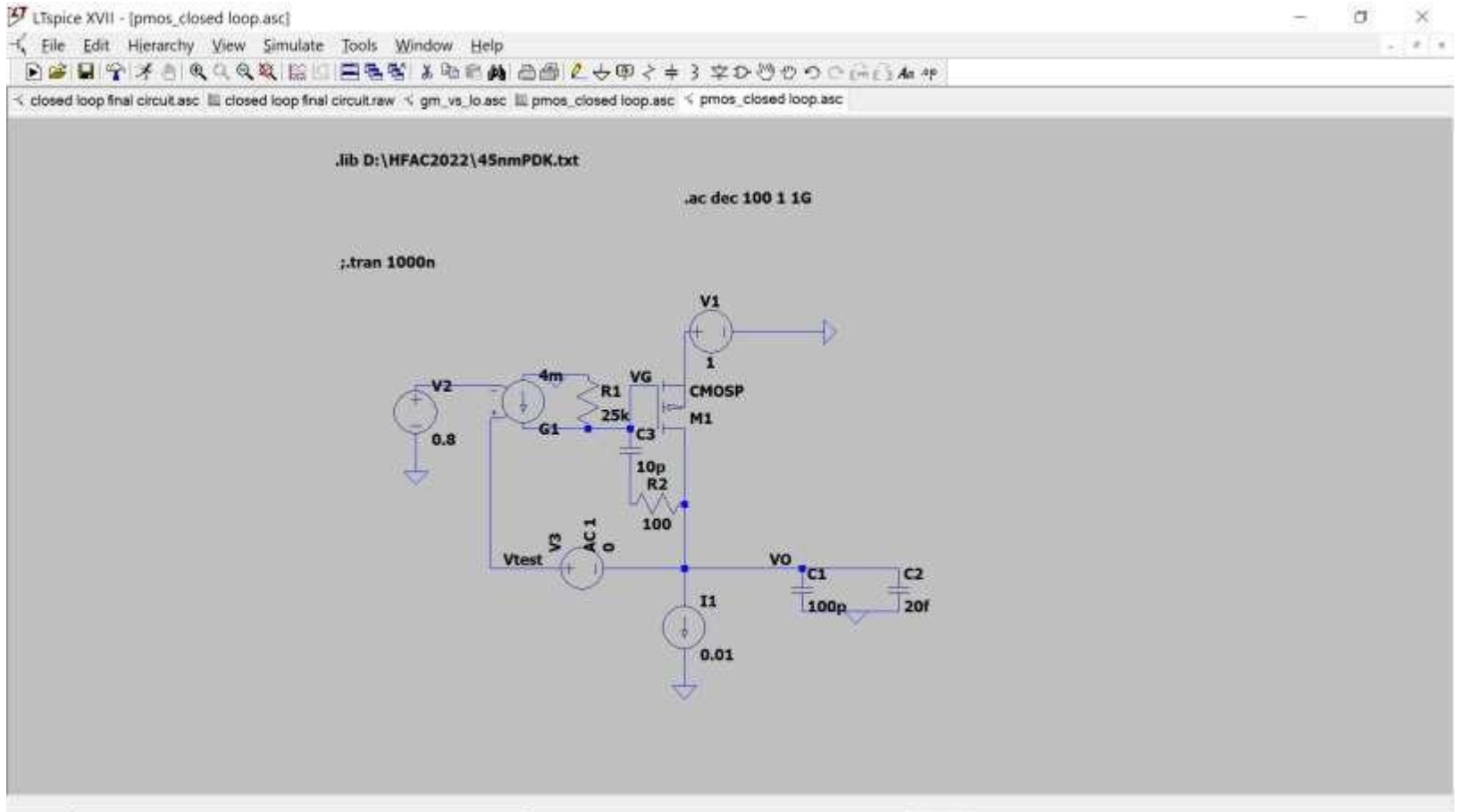

LTspice XVII - [pmos_closed loop.raw]
File View Plot Settings Simulation Tools Window Help
closed loop final circuit.asc
closed loop final circuit.raw
gm_vs_Io.asc
pmos_closed loop.asc
pmos_closed loop.raw
V(vo)
V(vin)
810mV
800mV
790mV
780mV
770mV
760mV
750mV
740mV
730mV
720mV
710mV
700mV
690mV
0ns
10ns
20ns
30ns
40ns
50ns
60ns
70ns
80ns
90ns
100ns
x = 95.60ns y = 748.40mV

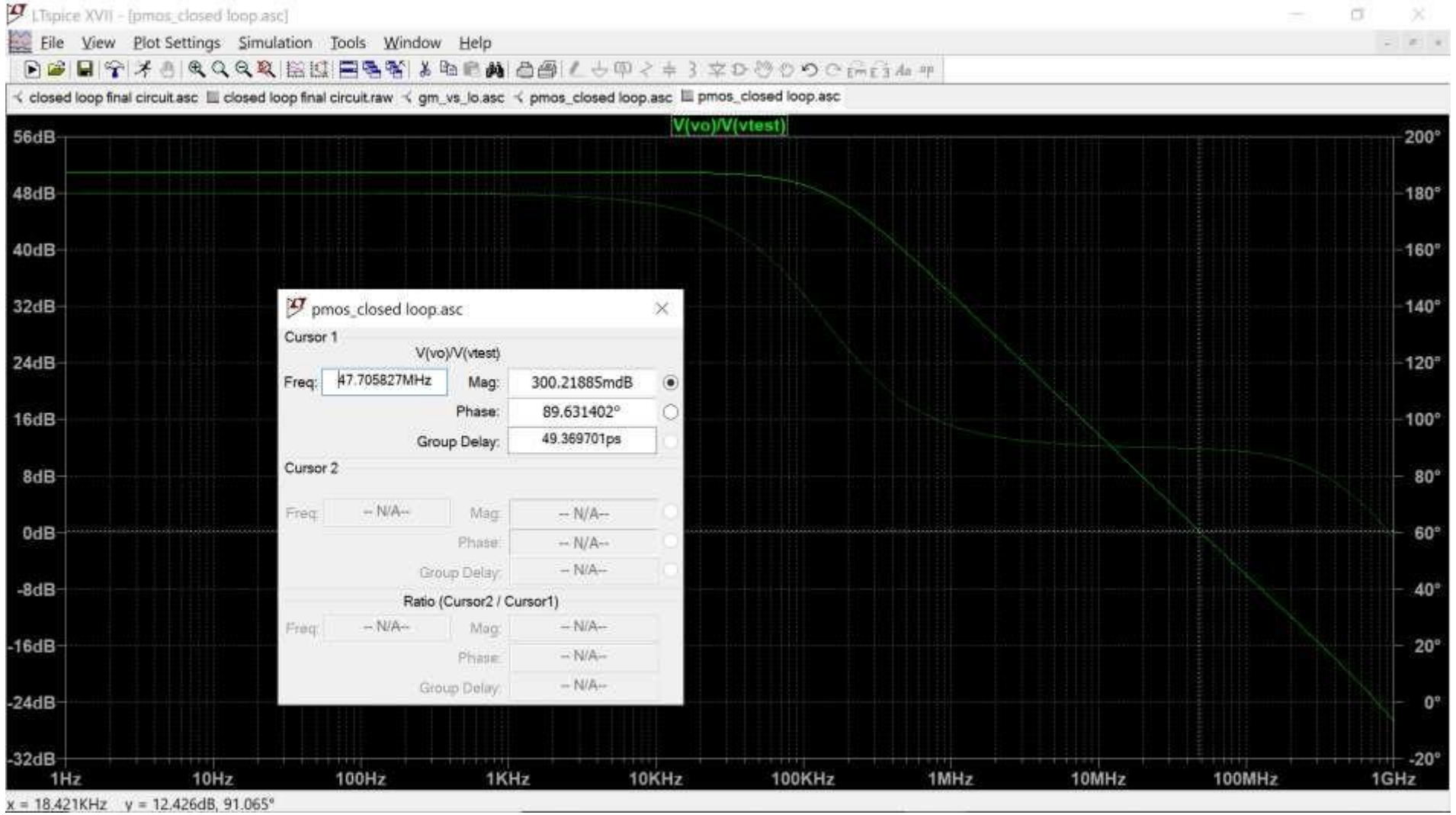
B. Pulse response




LTspice XVII - [pmos_closed loop.raw]
File View Plot Settings Simulation Tools Window Help
closed loop final circuit.asc
gm_vs_Io.asc
pmos_closed loop.asc
pmos_closed loop.raw
V(vo)
I(I1)
848mV
840mV
832mV
824mV
816mV
808mV
800mV
792mV
784mV
776mV
768mV
760mV
19mA
18mA
17mA
16mA
15mA
14mA
13mA
12mA
11mA
10mA
9mA
0.0µs
0.1µs
0.2µs
0.3µs
0.4µs
0.5µs
0.6µs
0.7µs
0.8µs
0.9µs
1.0µs
x = 0.561µs y = 810.29mV, 15.29mA

c. Frequency response




LTspice XVII - [pmos_closed loop.asc]
File View Plot Settings Simulation Tools Window Help
closed loop final circuit.asc
closed loop final circuit.raw
gm_vs_lo.asc
pmos_closed loop.asc
pmos_closed loop.asc
V(vo)/V(vtest)
56dB
48dB
40dB
32dB
24dB
16dB
8dB
0dB
-8dB
-16dB
-24dB
-32dB
200°
180°
160°
140°
120°
100°
80°
60°
40°
20°
0°
-20°
1Hz
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz
10MHz
100MHz
1GHz
pmos_closed loop.asc
Cursor 1
V(vo)/V(vtest)
Freq: 47.705827MHz
Mag: 300.21885mdB
Phase: 89.631402°
Group Delay: 49.369701ps
Cursor 2
Freq: -- N/A--
Mag: -- N/A--
Phase: -- N/A--
Group Delay: -- N/A--
Ratio (Cursor2 / Cursor1)
Freq: -- N/A--
Mag: -- N/A--
Phase: -- N/A--
Group Delay: -- N/A--
x = 18.421KHz y = 12.426dB, 91.065°