Guidelines regarding the Design Assignment for Pilani campus

1. The teams are expected to make a complete design on a chart paper which is physically realizable i.e. it has only existing components available in market. (**Note: Do not join A4 sheets**)

2. More emphasis will be given to this design i.e. its correctness, etc and its simulation in Proteus. If there are serious flaws in this design, it will earn minimal marks even if Proteus simulation is working well with some imaginary or unsuitable components.

3. The report should have following in this order.
Cover page
Problem Statement with specifications.
Assumptions made if any
List of the components used
Complete address Mapping of memory and I/O devices
IVT table if used
Flow chart of the software
Code with proper comments
Complete Circuit Diagram including clock generator, sensors, actuators, motor driver, ADC, etc.
References of any components used e.g. datasheets of the sensors or special ICs used , etc.

4. Method of Uploading to gmail account
1. Create a zipped file containing .asm file, design file(.dsn) and report in PDF format.
2. The name of the zipped file should be PXX_GYYY.zip. For example if your problem no. is 30 and the group number is 2, the zipped file should be P30_G002.zip
3. One of the team member should send the zipped file to respective instructor who will be conducting your viva before 12th noon of 25th April 2019. Any mails sent after this will not be entertained.

5. The team should bring the circuit diagram on a chart paper while coming for viva.

6. Every member should know the entire design regardless of what he/she is contributing in the project.

7. The evaluation is based on correctness of the design which decides the threshold of marks to be awarded.

8. The evaluation will be followed by testing the ability of each candidate to design a system around 8086 and it's peripherals through a viva.

9.The student must be thorough with his/her design as he/she will not be given more than two minutes to answer a particular question during the viva.

10. Proteus tries to emulate the design. For example if a particular sensor is not available, use a switch or resistor divider for verification/testing of the design.

Viva Date: Tentatively last week of April & it will be completed within one day.