# EDA Basics

* **History**
  + Automation begins in mid-70's
  + Introduction to VLSI systems by Carver Mead and Lynn Conway
    - Ground-breaking text
    - Advocated programming languages that compiled directly to silicon
    - Led to increase in complexity of chips
    - Specify desired behavior in a textual programming language and let the tools derive the detailed physical design
  + Early Tools
    - Berkeley VLSI Tools Tarball: A set of UNIX utilities used to design early VLSI systems.
    - Espresso heuristic logic minimizer and Magic : still used
  + MOSIS (Metal Oxide Semiconductor Implementation Service)
  + 1981 : birth of commercial EDA
    - Daisy Systems, Mentor Graphics, and Valid Logic Systems (DMV) founded around this time,
    - US Department of Defense funds VHDL
  + 1986: Verilog developed by Gateway Design Automation (Company owned by Prabhu Goel)
    - Designed by Phil Moorby
      * Became chief designer of Verilog-XL
  + 1989: Verilog-XL acquired by Cadence

* **Design Flow**
  + **System Specification**
  + **High level synthesis**: high level description --> RTL
  + **Functional Design (RTL)**
  + **Logic synthesis:** RTL design description --> discrete netlist (logic gates)
  + **Logic Design (gates/flip flops)**
  + **Schematic capture**
  + **Circuit design**
  + **Layout**
  + **Physical Design**
    - Netlist --> HW
    - Circuit description --> geometric description
    - Steps
      1. Partitioning, floorplanning, placement
      2. Routing
      3. Static timing Analysis
      4. Signal Integrity and crosstalk analysis
      5. Physical verification and signoff
  + **Design Verification**
  + **Fabrication**
  + **Packaging, testing, debugging**

* **Design Styles**
  + **Programmable Logic Devices**
    - **FPGA**
      * User/Field Programmability
      * Array of logic cells connected via routing channel (both programmable)
      * Different type of cells:
        + Special I/O cells
        + Logic Cells : Lookup Tables (LUT) with associated registers
      * Interconnection b/w cells:
        + Using SRAM based switches

Memories that store switch status

* + - * + Using anti-fuse elements

Connection made by flowing high current (fusing)

* + - * I/O Blocks, Configurable Logic Blocks (CLB)
      * CLB consists of:
        + Input function generators: implemented using Lookup Tables (LUT) using RAM (by matching output to truth table)

Can be used as memory

* + - * + Registers: can be configured as flip-flop or latch

Independent clock polarity

Synchronous and asynchronous set/reset

* + - * Area/delay tradeoff
      * Routing
        + Fast Direct Interconnect : CLB to CLB
        + General Purpose Interconnect using switch matrix
      * Logic, interconnection and I/O blocks all are programmable
      * Design Flow
        + Design Entry: Verilog or VHDL
        + Implementation

Placement and Routing (partitioning)

Partition into sub-circuit with max 4x1 LUTs

LUTs placed in CLBs

Bitstream generation

Analyze timing, view layout, simulation, etc

* + - * + Download to device
    - **Gate Array**
      * In between FPGA and ASIC (closer to FPGA)
      * Implementation is 2-step manufacturing (unlike FPGA which is all by user)
        + First phase (independent of function)

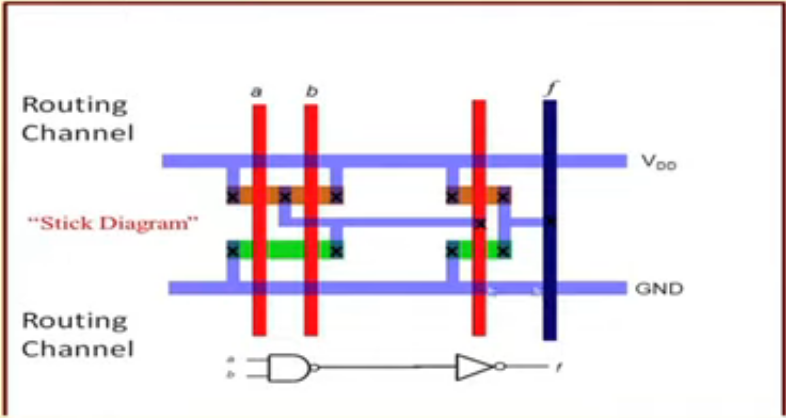
Based on generic masks

Fabrication of large number of uncommitted transistors

Reduces fab cost

* + - * + Second phase (Customization. Design-specific)

The uncommitted chips are customized by defining interconnects

* + - * Chip utilization factor is much higher than FPGA (working at lower level: transistor level)er than FPGA (working at lower level at t
      * Higher Speed than FPGA
      * Can implement millions of logic gates per chip
  + **Standard Cell Based (Semi-Custom Design)**
    - Standard Cell Based Design (Semi Custom)
      * One way of implementing ASIC
      * Using pre-designed cells in design (stored in a library: Standard Cell Library) which can be placed directly on silicon
      * Standard Cells
        + Same height, different widths
        + Placed in well defined rows and cells placed next to each other
        + Routing, floorplanning etc is simpler
        + Power and GND rails run parallel to upper and lower boundaries of a cell
        + 

Blue: metal connections

Red: poly-silicon connections

Green/Brown: diffusions

Black X: interconnections

* If need to connect two non adjacent rows: Use special cells called “Through Cells”
* Requries developing full custom mask set required for fabrication
* **Full-Custom Design**
  + Other ASIC implementation
  + Designing everything from scratch
  + Longer time to design
  + Blocks can be of any arbitrary size and complexity
  + Placement much more challenging (to make routing work)
  + Entire mask design done anew w/o using any library
  + Impractical
  + Memory Cell can use full custom design (layout is repetitive)
* Design and reuse philosophy more popular/practical today (IP)
* **Which style to use? Tradeoff**
  + HW Cost
  + Circuit Delay
  + Time required

* **Simulation**
  + **Transistor Simulation:** low-level transistor-simulation of a schematic/layout's behavior, accurate at device-level
  + **Logic Simulation:**  digital-simulation of an RTL or gate-netlist's digital (boolean 0/1) behavior, accurate at boolean-level
  + **Behavioural Simulation:** high-level simulation of a design's architectural operation, accurate at cycle-level or interface-level
  + **Hardware Emulation:**   Use of special purpose hardware to emulate the logic of a proposed design. Can sometimes be plugged into a system in place of a yet-to-be-built chip; this is called *in-circuit emulation*
  + **Technology CAD:** Simulate and analyze the underlying process technology. Electrical properties of devices are derived directly from device physics
  + **Electromagnetic Field Solvers/ Field Solvers:** Solve Maxwell's equations directly for cases of interest in IC and PCB design. They are known for being slower but more accurate than the layout extraction above

* **Analysis and verification** 
  + **Functional verification:**
  + **Clock domain crossing verification (CDC check):** 
    - Similar to linting
    - Specialise in detecting and reporting potential issues like data loss, meta-stability due to use of multiple clock domains in the design
  + **Formal verification, Model Checking:**
    - Prove, by mathematical methods, that the system has certain desired properties, and that certain undesired effects (such as deadlock) cannot occur
  + **Equivalence checking:** 
    - Algorithmic comparison between a chip's RTL-description and synthesized gate-netlist, to ensure functional equivalence at the logical level
  + **Static Timing Analysis:** 
    - Analysis of the timing of a circuit in an input-independent manner, hence finding a worst case over all possible inputs
  + **Physical verification:** 
    - Checking if a design is physically manufacturable, and that the resulting chips will not have any function-preventing physical defects, and will meet original specifications.

* **Manufacturing preparation**
  + **Mask data preparation, MDP:** Generation of actual lithography photomask used to physically manufacture the chip
  + **Resolution enhancement techniques, RET:** Methods of increasing the quality of final photomask
  + **Optical proximity correction, OPC:** Up-front compensation for diffraction and interference effects occurring later when chip is manufactured using this mask
  + **Mask generation:** Generation of flat mask image from hierarchical design
  + **Automatic test pattern generation, ATPG:** Generates pattern-data to systematically exercise as many logic-gates, and other components, as possible
  + **Built-in self-test, or BIST:** Installs self-contained test-controllers to automatically test a logic (or memory) structure in the design

* **Challenges**
  + Physics constantly changes
  + Short unforgiving design cycle, market driven by consumer
  + Huge scale: several billion active parts
  + Very expensive ($10-100M for a typical chip, $1B for state-of-the-art microprocessor)
    - Product revenues must be at least 10 times cost of development
  + Expected work on the first attempt

* **Risk Management**
  + Bulk of design time and tool investment
  + Design is expensive to tape-out and build (takes months)
    - Huge amounts of simulation, verification before tape-out, wait several months for results (enormous cost)
  + Verification is 3/4 of the design cost
* **Further reading**
  + *Electronic Design Automation For Integrated Circuits Handbook*, by Lavagno, Martin, and Scheffer, [ISBN](https://en.wikipedia.org/wiki/ISBN_(identifier)) [0-8493-3096-3](https://en.wikipedia.org/wiki/Special:BookSources/0-8493-3096-3) A survey of the field of electronic design automation, one of the main enablers of modern IC design.
  + IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems

[https://en.wikipedia.org/wiki/](https://en.wikipedia.org/wiki/Comparison_of_EDA_software)

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