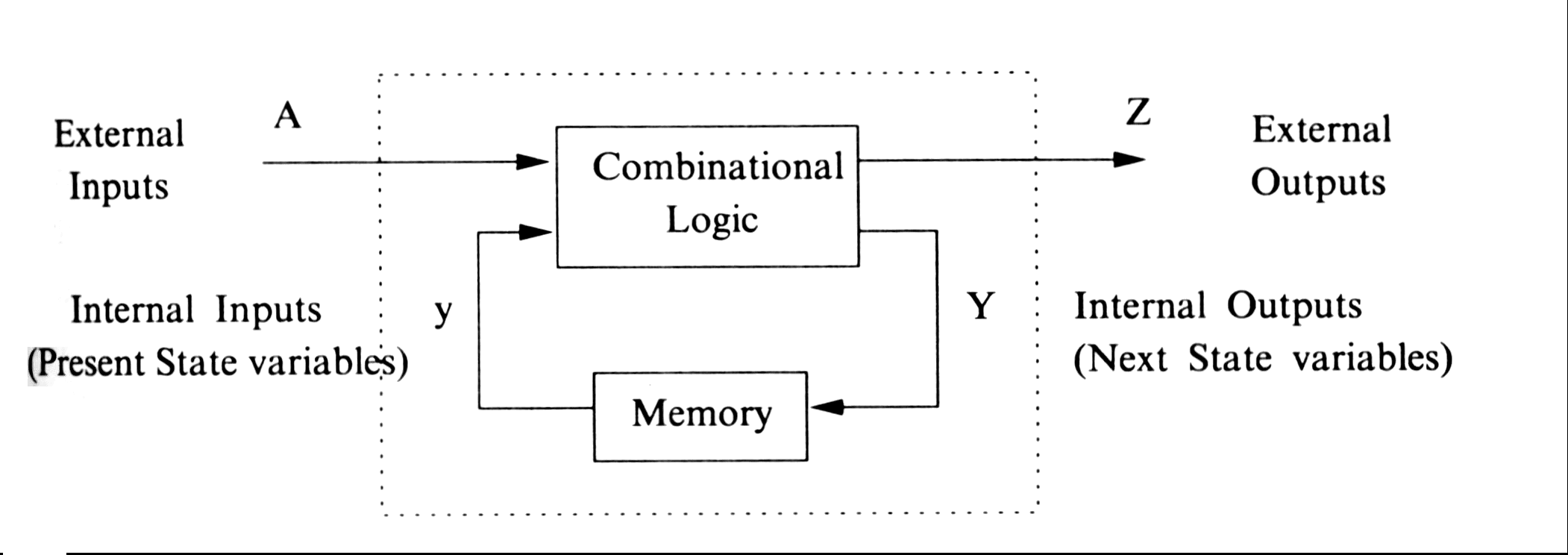
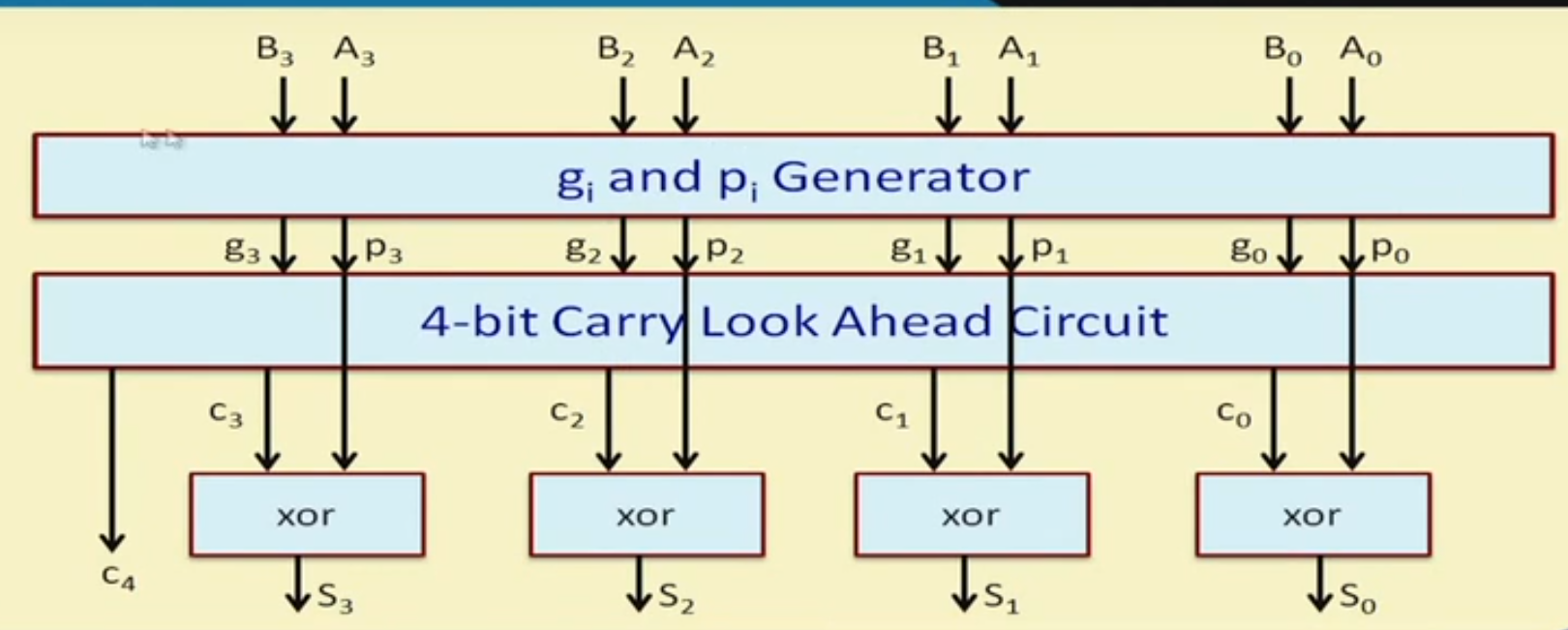
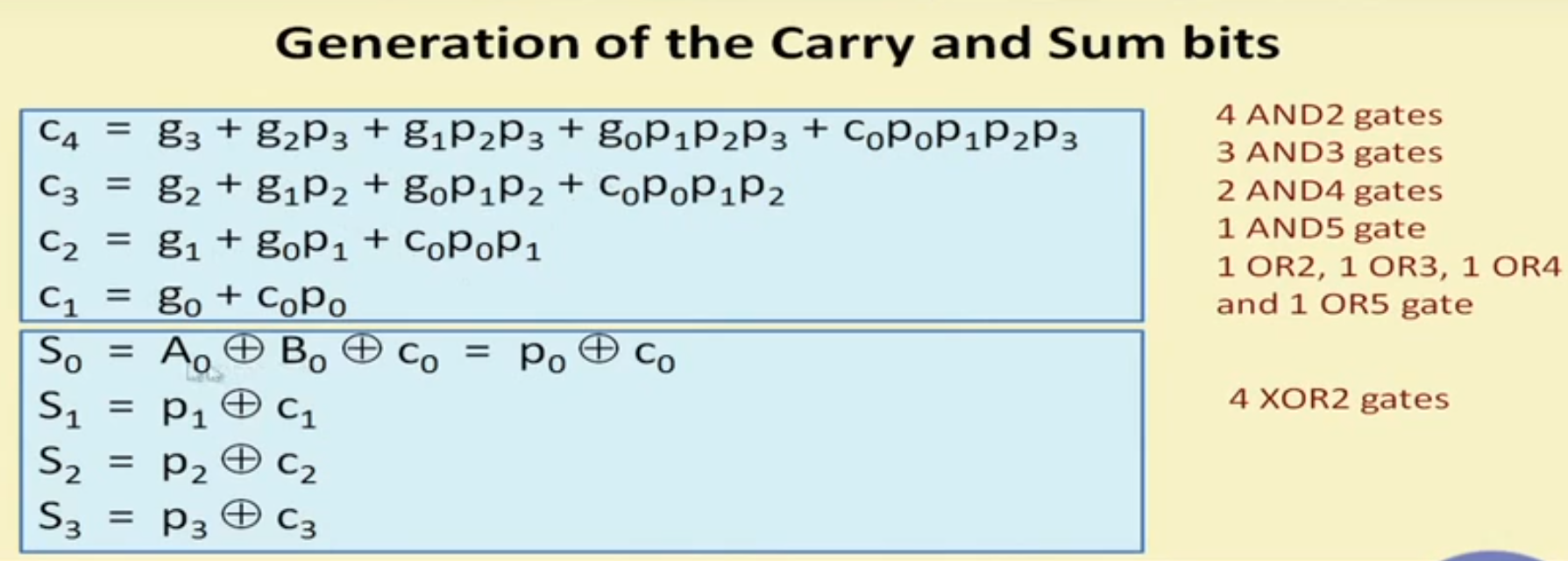
# Digital Design

Combinational circuits

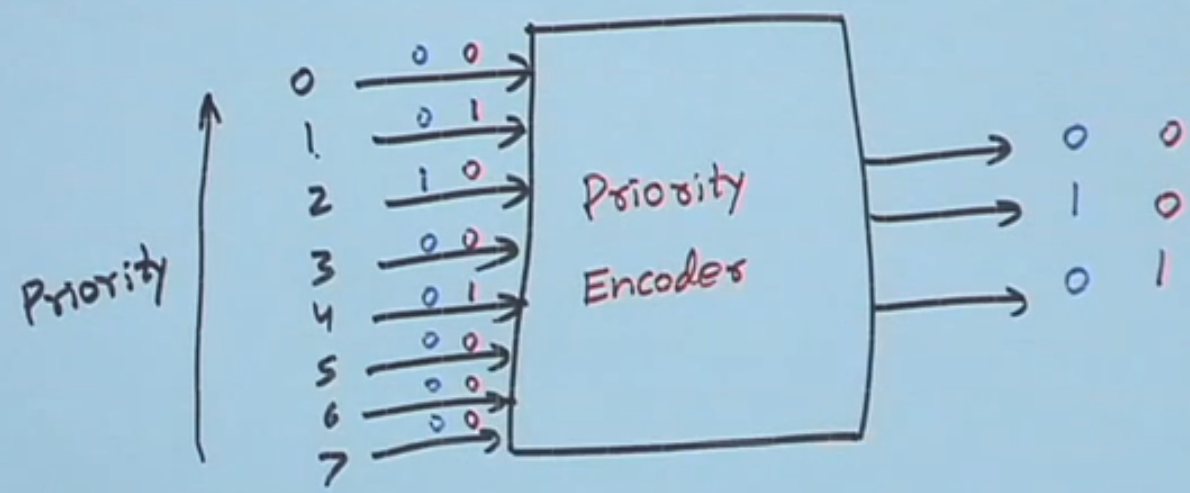
* + Output depends on current value of inputs only
  + No memory
* Sequential circuits
  + Output depends on past inputs, output
  + Have memory



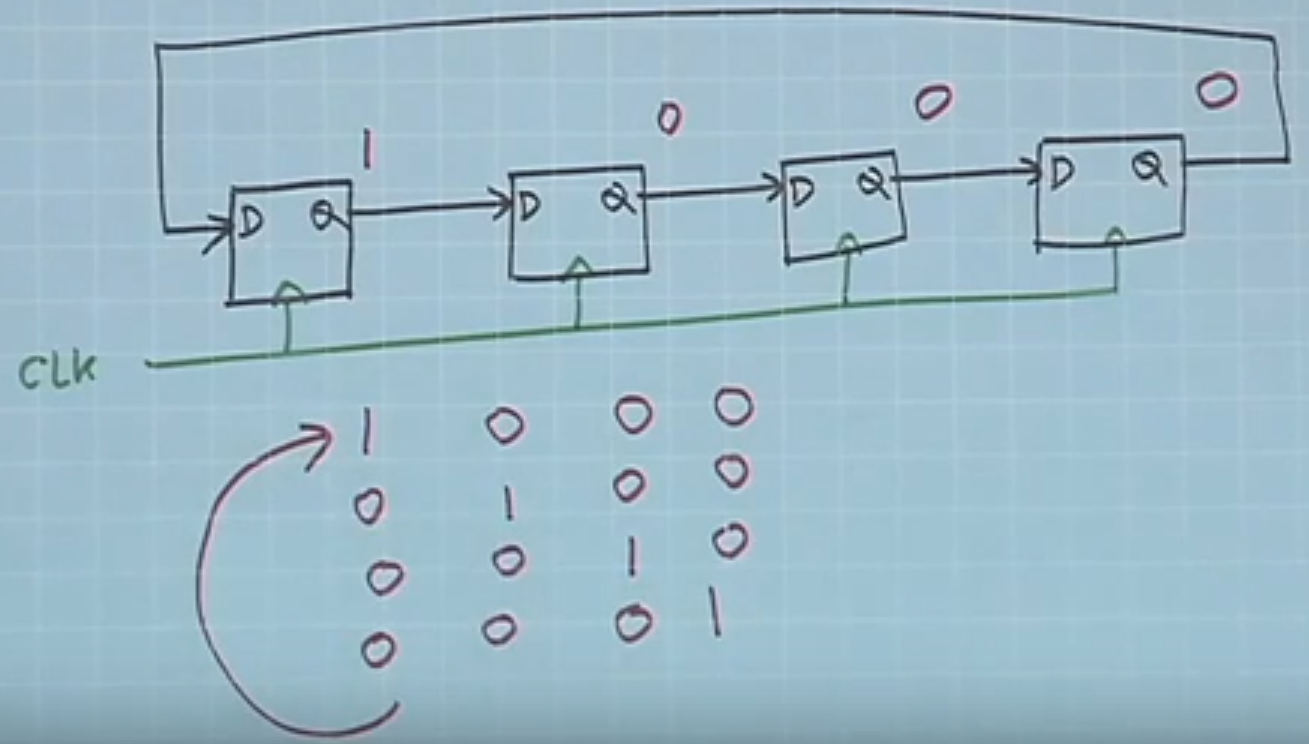
* **Carry Lookahead Adder (CLA)**
  + Propagation delay of n-bit ripple carry adder = O(n)
  + With CLA, time complexity = O(1)
  + HW complexity also rapidly increases
  + Define functions *carry generate* and *carry propagate*g\_i = A\_i & B\_i  
    p\_i = A\_i ^ B\_i  
      
    g\_i = 1 => carry generated in stage independent of other stages  
    p\_i = 1 => input carry c\_i propagated to output carry c\_i+1  
      
    therefore: c\_i+1 = g\_i | (p\_i & c\_i)  
    => all carry's can be got with 2 level and/or gates
  + 

* 

* **Priority Encoder**



* **Ring Counter**
  + Shift register comprising of several D flip-flops
  + Eg: 4 bit ring counter:  
    Typically initialized to 1000



* JK FlipFLop