Property Specification Language (PSL)

Formal specification of electronic system behaviour

* Captured as *properties*, executed as *assertions*
* Used to describe *temporal properties* of a design (temporal logic)
* 2 ways of using
  + In a Simulation Environment
    - aka *Assertion Based Verification (ABV)*
    - Assertions: used as inbuilt checkers that fire as soon as a behaviour is identified that is not in conformance with the specification as encapsulated in a PSL property
  + With Static or Formal Verification Tools
    - Tool attempts to find any way that the property can be violated
    - More exhaustive than ABV
* Somewhat language independent: takes flavour of the HDL
* Defined in 4 layers
  + Boolean
    - Used for describing the current state of the design
    - Phrased using an HDL
  + Temporal
    - Uses temporal operators to describe scenarios that span over time
  + Modelling
    - Used to describe auxiliary state machines in a procedural manner
  + Verification
    - Uses directives to a verification tool
    - Eg: assert that a given property is correct
* Example usage:  
  Assert (always req -> next (ack until grant)) @clk
  + "after the req signal becomes active, then on the next clk edge, ack must be active and stay active until the grant signal is active"