

**DEPT. OF ELECTRICAL & ELECTRONICS ENGINEERING**  
**SRM INSTITUTE OF SCIENCE AND TECHNOLOGY, Kattankulathur – 603203.**

Title of Experiment	: Study of 8051 microcontroller
Name of the candidate	: GAUTAM NAG
Register Number	: RA1811005010278
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<b>S.NO :</b>	<b>MARKS SPLIT UP</b>	<b>MAXIMUM MARKS (50)</b>	<b>MARKS OBTAINED</b>
1	PRE LAB	5	
2	PROGRAM	25	
3	EXECUTION	15	
4	POST LAB	5	
TOTAL		50	

**Staff Signature**

## **PRE LAB QUESTION & ANSWERS**

### **1. What is microprocessor?**

A microprocessor is a computer processor where the data processing logic and control is included on a single integrated circuit, or a small number of integrated circuits.

### **2. What is the function of program counter?**

PROGRAM COUNTER. The program counter, PC, is a special-purpose register that is used by the processor to hold the address of the next instruction to be executed. The PLA automatically updates the PC to point to the next instruction during the op-code decode cycle.

### **3. What is the function of stack pointer?**

The Stack Pointer (SP) register is used to indicate the location of the last item put onto the stack. When you PUT something ONTO the stack (PUSH onto the stack), the SP is decremented before the item is placed on the stack.

### **4. What is an operating system?**

An operating system is system software that manages computer hardware, software resources, and provides common services for computer programs.

### **5. What is the function of ALE, and S0, S1 pin?**

These are output status signals used to give information of operation performed by microprocessor. The S0 and S1 lines specify 4 different conditions of 8085 machine cycles.

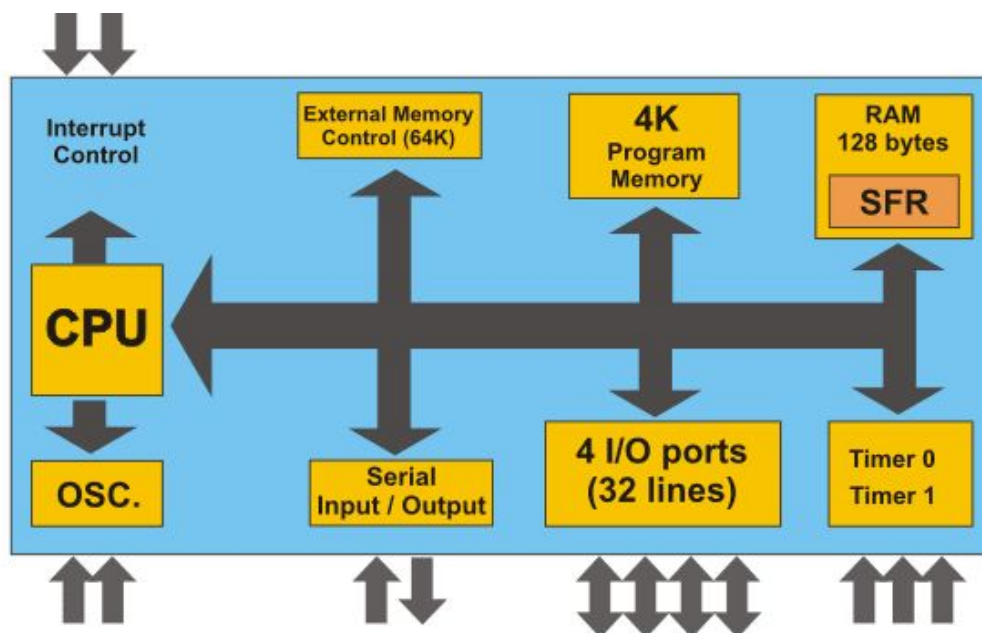
Read: This is an active low output control signal used to read data from memory or an I/O device.

## 1. STUDY OF 8051 MICROCONTROLLER

### Aim

To study the microcontroller 8051

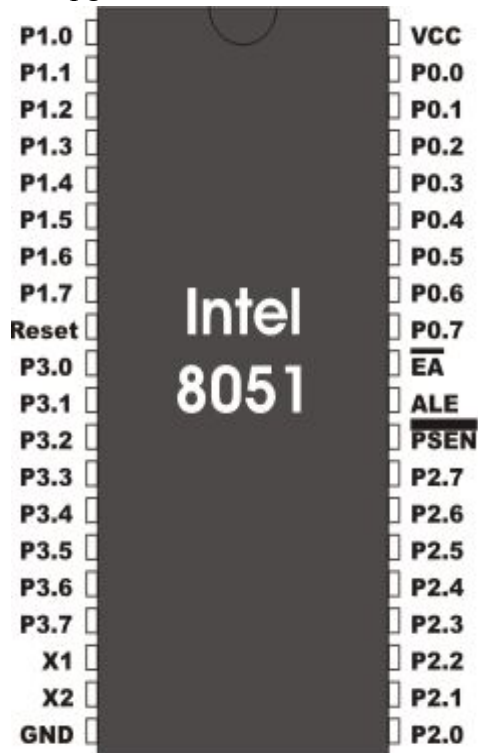
### Architecture of 8051 Microcontroller



Architecture of 8051 microcontroller has following features

- 4 Kb of ROM is not much at all.
- 128 bytes of RAM (including SFRs) satisfies the user's basic needs.
- 4 ports having in total of 32 input/output lines are in most cases sufficient to make all necessary connections to peripheral environment.

The whole configuration is obviously thought of as to satisfy the needs of most programmers working on development of automation devices. One of its advantages is that nothing is missing and nothing is too much. In other words, it is created exactly in accordance to the average user's taste and needs. Other advantages are RAM organization, the operation of Central Processor Unit (CPU) and ports which completely use all recourses and enable further upgrade.



### Pin out Description

**Pins 1-8: Port 1** each of these pins can be configured as an input or an output.

**Pin 9: RS** A logic one on this pin disables the microcontroller and clears the contents of most registers. In other words, the positive voltage on this pin resets the microcontroller. By applying logic zero to this pin, the program starts execution from the beginning.

**Pins 10-17: Port 3** Similar to port 1, each of these pins can serve as general input or output. Besides, all of them have alternative functions:

**Pin 10: RXD** Serial asynchronous communication input or Serial synchronous communication output.

**Pin 11: TXD** Serial asynchronous communication output or Serial synchronous communication clock output.

**Pin 12: INT0** Interrupt 0 inputs.

**Pin 13: INT1** Interrupt 1 input.

**Pin 14: T0** Counter 0 clock input.

**Pin 15: T1** Counter 1 clock input.

**Pin 16: WR** Write to external (additional) RAM.

**Pin 17: RD** Read from external RAM.

**Pin 18, 19: X2, X1** Internal oscillator input and output. A quartz crystal which specifies operating frequency is usually connected to these pins. Instead of it, miniature ceramics resonators can also be used for frequency stability. Later versions of microcontrollers operate at a frequency of 0 Hz up to over 50 Hz.

**Pin 20: GND** Ground.

**Pin 21-28: Port 2** If there is no intention to use external memory then these port pins are configured as general inputs/outputs. In case external memory is used, the higher address byte, i.e. addresses A8-A15 will appear on this port. Even though memory with capacity of 64Kb is not used, which means that not all eight port bits are used for its addressing, the rest of them are not available as inputs/outputs.

**Pin 29: PSEN** If external ROM is used for storing program then a logic zero (0) appears on it every time the microcontroller reads a byte from memory.

**Pin 30: ALE** Prior to reading from external memory, the microcontroller puts the lower address byte (A0-A7) on P0 and activates the ALE output. After receiving signal from the ALE pin, the external register (usually 74HCT373 or 74HCT375 add-on chip) memorizes the state of P0 and uses it as a memory chip address. Immediately after that, the ALU pin is returned its previous logic state and P0 is now used as a Data Bus. As seen, port data multiplexing is performed by means of only one additional (and cheap) integrated circuit. In other words, this port is used for both data and address transmission.

**Pin 31: EA** By applying logic zero to this pin, P2 and P3 are used for data and address transmission with no regard to whether there is internal memory or not. It means that even there is a program written to the microcontroller, it will not be executed. Instead, the program written to external ROM will be executed. By applying logic one to the EA pin, the microcontroller will use both memories, first internal then external (if exists).

**Pin 32-39: Port 0** Similar to P2, if external memory is not used, these pins can be used as general inputs/outputs. Otherwise, P0 is configured as address output (A0-A7) when the ALE pin is driven high (1) or as data output (Data Bus) when the ALE pin is driven low (0).

**Pin 40: VCC +5V** power supply.

#### **Input/Output Ports (I/O Ports)**

All 8051 microcontrollers have 4 I/O ports each comprising 8 bits which can be configured as inputs or outputs. Accordingly, in total of 32 input/output pins enabling the microcontroller to be connected to peripheral devices are available for use.

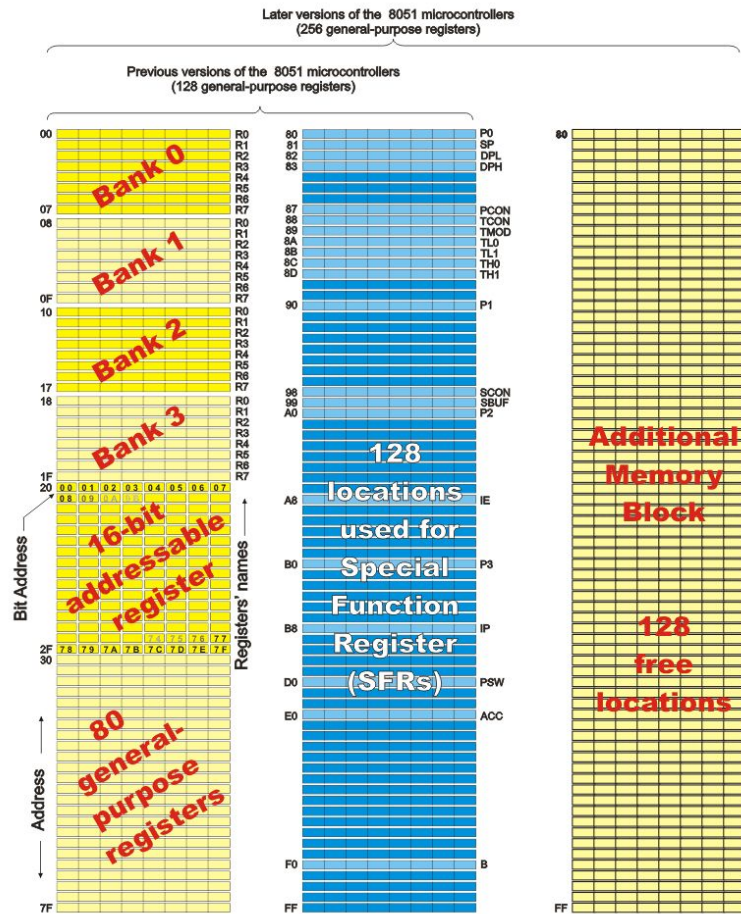
Pin configuration, i.e. whether it is to be configured as an input (1) or an output (0), depends on its logic state. In order to configure a microcontroller pin as an input, it is necessary to apply a logic zero (0) to appropriate I/O port bit. In this case, voltage level on appropriate pin will be 0.

Similarly, in order to configure a microcontroller pin as an input, it is necessary to apply a logic one (1) to appropriate port. In this case, voltage level on appropriate pin will be 5V (as is the case with any TTL input). This may seem confusing but don't lose your patience. It all becomes clear after studying simple electronic circuits connected to an I/O pin.

#### **Memory Organization**

The 8051 has two types of memory and these are Program Memory and Data Memory. Program Memory (ROM) is used to permanently save the program being executed, while Data Memory (RAM) is used for temporarily storing data and intermediate results created and used during the operation of the microcontroller. Depending on the model in use (we are still talking about the 8051 microcontroller family in general) at most a few Kb of ROM and 128 or 256 bytes of RAM is used. However...

All 8051 microcontrollers have a 16-bit addressing bus and are capable of addressing 64 kb memory. It is neither a mistake nor a big ambition of engineers who were working on basic core development. It is a matter of smart memory organization which makes these microcontrollers a real "programmers' goody".



### Special Function Registers (SFRs)

Special Function Registers (SFRs) are a sort of control table used for running and monitoring the operation of the microcontroller. Each of these registers as well as each bit they include, has its name, address in the scope of RAM and precisely defined purpose such as timer control, interrupt control, serial communication control etc. Even though there are 128 memory locations intended to be occupied by them, the basic core, shared by all types of 8051 microcontrollers, has only 21 such registers. Rest of locations is intentionally left unoccupied in order to enable the manufacturers to further develop microcontrollers keeping them compatible with the previous versions. It also enables programs written a long time ago for microcontrollers which are out of production now to be used today.

F8									FF
F0	B								F7
E8									EF
E0	ACC								E7
D8									DF
D0	PSW								D7
C8									CF
C0									C7
B8	IP								BF
B0	P3								B7
A8	IE								AF
A0	P2								A7
98	SCON	SBUF							9F
90	P1								97
88	TCON	TMOD	TL0	TL1	TH0	TH1			8F
80	P0	SP	DPL	DPH				PCON	87

↑  
Bit-addressable Registers

### Program Status Word (PSW) Register

	0	0	0	0	0	0	0	Value after Reset
<b>PSW</b>	CY	AC	F0	RS1	RS0	OV	P	Bit name
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0

PSW register is one of the most important SFRs. It contains several status bits that reflect the current state of the CPU. Besides, this register contains Carry bit, Auxiliary Carry, two register bank select bits, Overflow flag, parity bit and user-definable status flag.

**P - Parity bit.** If a number stored in the accumulator is even then this bit will be automatically set (1), otherwise it will be cleared (0). It is mainly used during data transmit and receive via serial communication.

**- Bit 1.** This bit is intended to be used in the future versions of microcontrollers.

**OV Overflow** occurs when the result of an arithmetical operation is larger than 255 and cannot be stored in one register. Overflow condition causes the OV bit to be set (1). Otherwise, it will be cleared (0).

**RS0, RS1 - Register bank select bits.** These two bits are used to select one of four register banks of RAM. By setting and clearing these bits, registers R0-R7 are stored in one of four banks of RAM.

RS1	RS0	Space in RAM
0	0	Bank0 00h-07h
0	1	Bank1 08h-0Fh
1	0	Bank2 10h-17h



1	1	Bank3 18h-1Fh
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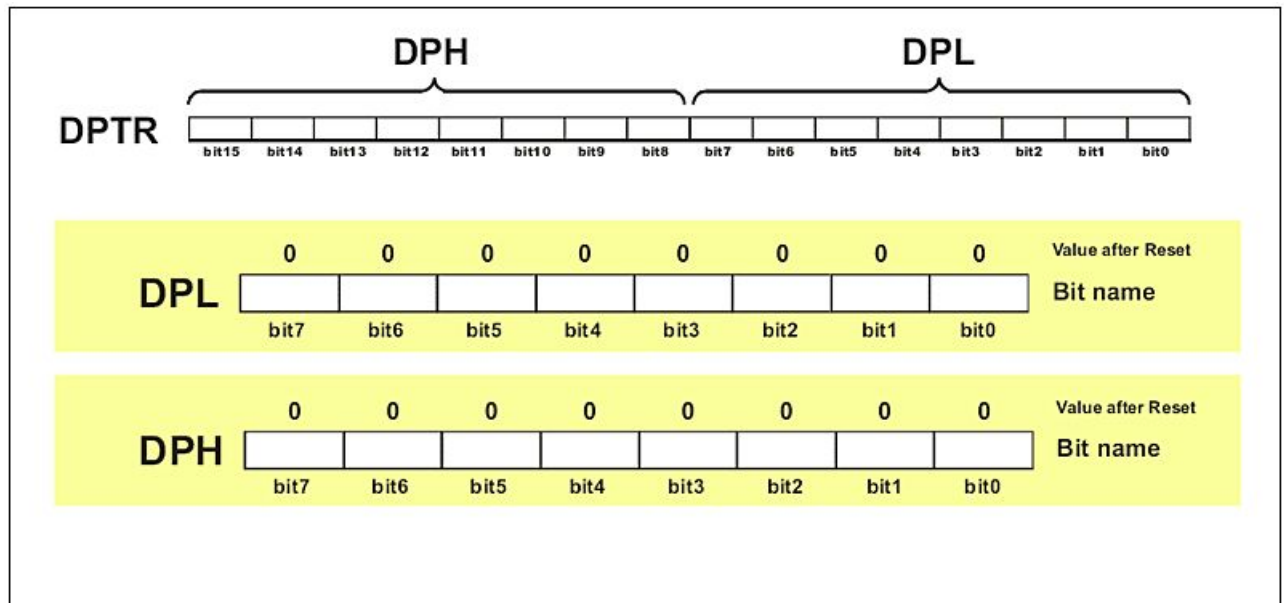
**F0 - Flag 0.** This is a general-purpose bit available for use.

**AC - Auxiliary Carry Flag** is used for BCD operations only.

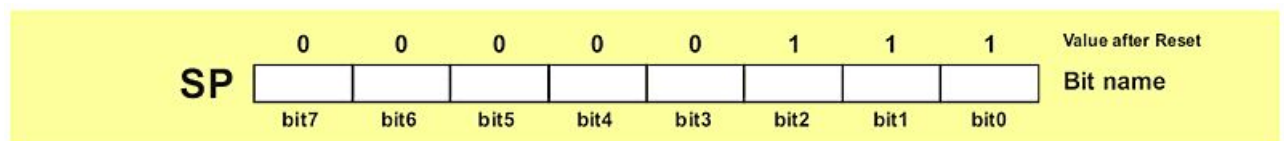
**CY - Carry Flag** is the (ninth) auxiliary bit used for all arithmetical operations and shift instructions.

### Data Pointer Register (DPTR)

DPTR register is not a true one because it doesn't physically exist. It consists of two separate registers: DPH (Data Pointer High) and (Data Pointer Low). For this reason it may be treated as a 16-bit register or as two independent 8-bit registers. Their 16 bits are primarily used for external memory addressing. Besides, the DPTR Register is usually used for storing data and intermediate results.

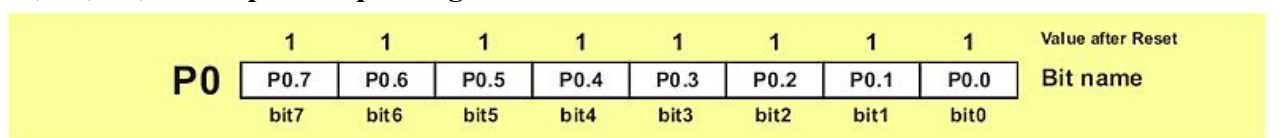


### Stack Pointer (SP) Register



A value stored in the Stack Pointer points to the first free stack address and permits stack availability. Stack pushes increment the value in the Stack Pointer by 1. Likewise, stack pops decrement its value by 1. Upon any reset and power-on, the value 7 is stored in the Stack Pointer, which means that the space of RAM reserved for the stack starts at this location. If another value is written to this register, the entire Stack is moved to the new memory location.

### P0, P1, P2, P3 - Input/Output Registers



If neither external memory nor serial communication system are used then 4 ports with in total of 32 input/output pins are available for connection to peripheral environment. Each bit within these ports affects the state and performance of appropriate pin of the microcontroller.



As mentioned, port bit state affects performance of port pins, i.e. whether they will be configured as inputs or outputs. If a bit is cleared (0), the appropriate pin will be configured as an output, while if it is set (1), the appropriate pin will be configured as an input. Upon reset and power-on, all port bits are set (1), which means that all appropriate pins will be configured as inputs.

As you already know, the microcontroller oscillator uses quartz crystal for its operation. As the frequency of this oscillator is precisely defined and very stable, pulses it generates are always of the same width, which makes them ideal for time measurement. Such crystals are also used in quartz watches. In order to measure time between two events it is sufficient to count up pulses coming from this oscillator. That is exactly what the timer does. If the timer is properly programmed, the value stored in its register will be incremented (or decremented) with each coming pulse, i.e. once per each machine cycle. A single machine-cycle instruction lasts for 12 quartz oscillator periods, which means that by embedding quartz with oscillator frequency of 12MHz, a number stored in the timer register will be changed million times per second, i.e. each microsecond.

## Timer T0

Diagram illustrating the structure of the Timer T0 register. The register is divided into two 8-bit sections: TH0 Register (bits 15 to 8) and TL0 Register (bits 7 to 0). The bits are labeled bit15, bit14, bit13, bit12, bit11, bit10, bit9, bit8, bit7, bit6, bit5, bit4, bit3, bit2, bit1, bit0. The entire register is labeled 'Timer T0' at the bottom.

Value after reset

Bit name

TH0

0 0 0 0 0 0 0 0

bit7 bit6 bit5 bit4 bit3 bit2 bit1 bit0

TL0

0 0 0 0 0 0 0 0

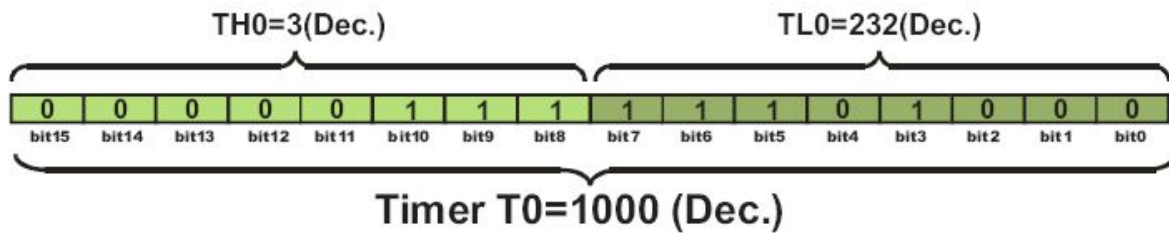
bit7 bit6 bit5 bit4 bit3 bit2 bit1 bit0

Formula used to calculate values in these two registers is very simple:

$$TH0 \times 256 + TL0 = T$$

Matching the previous example it would be as follows:

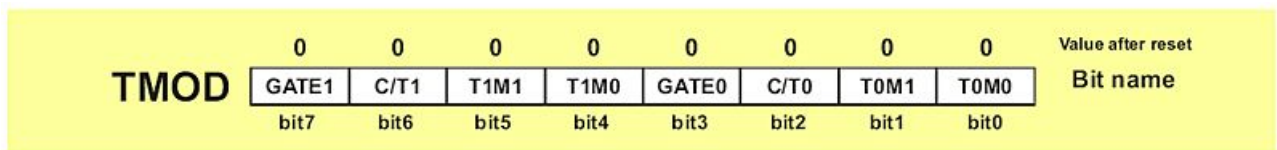
$$3 \times 256 + 232 = 1000$$



Since the timer T0 is virtually 16-bit register, the largest value it can store is 65 535. In case of exceeding this value, the timer will be automatically cleared and counting starts from 0. This condition is called an overflow. Two registers TMOD and TCON are closely connected to this timer and control its operation.

### TMOD Register (Timer Mode)

The TMOD register selects the operational mode of the timers T0 and T1. As seen in figure below, the low 4 bits (bit0 - bit3) refer to the timer 0, while the high 4 bits (bit4 - bit7) refer to the timer 1. There are 4 operational modes and each of them is described herein.



Bits of this register have the following function:

- **GATE1** enables and disables Timer 1 by means of a signal brought to the INT1 pin (P3.3):
  - **1** - Timer 1 operates only if the INT1 bit is set.
  - **0** - Timer 1 operates regardless of the logic state of the INT1 bit.
- **C/T1** selects pulses to be counted up by the timer/counter 1:
  - **1** - Timer counts pulses brought to the T1 pin (P3.5).
  - **0** - Timer counts pulses from internal oscillator.
- **T1M1, T1M0** These two bits select the operational mode of the Timer 1.

T1M1	T1M0	Mode	Description
0	0	0	13-bit timer
0	1	1	16-bit timer
1	0	2	8-bit auto-reload
1	1	3	Split mode

- **GATE0** enables and disables Timer 0 using a signal brought to the INT0 pin (P3.2):
  - **1** - Timer 0 operates only if the INT0 bit is set.
  - **0** - Timer 0 operates regardless of the logic state of the INT0 bit.
- **C/T0** selects pulses to be counted up by the timer/counter 0:

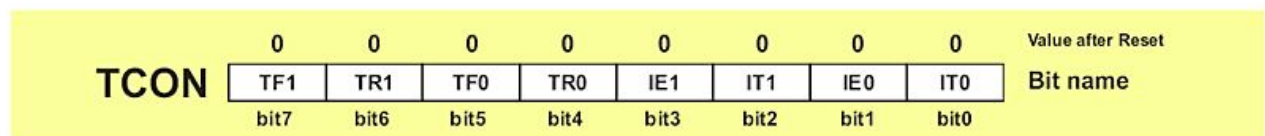
- **1** - Timer counts pulses brought to the T0 pin (P3.4).
- **0** - Timer counts pulses from internal oscillator.
- **T0M1,T0M0** These two bits select the operational mode of the Timer 0.

T0M1	T0M0	Mode	Description
0	0	0	13-bit timer
0	1	1	16-bit timer
1	0	2	8-bit auto-reload
1	1	3	Split mode

### Timer Control (TCON) Register

TCON register is also one of the registers whose bits are directly in control of timer operation.

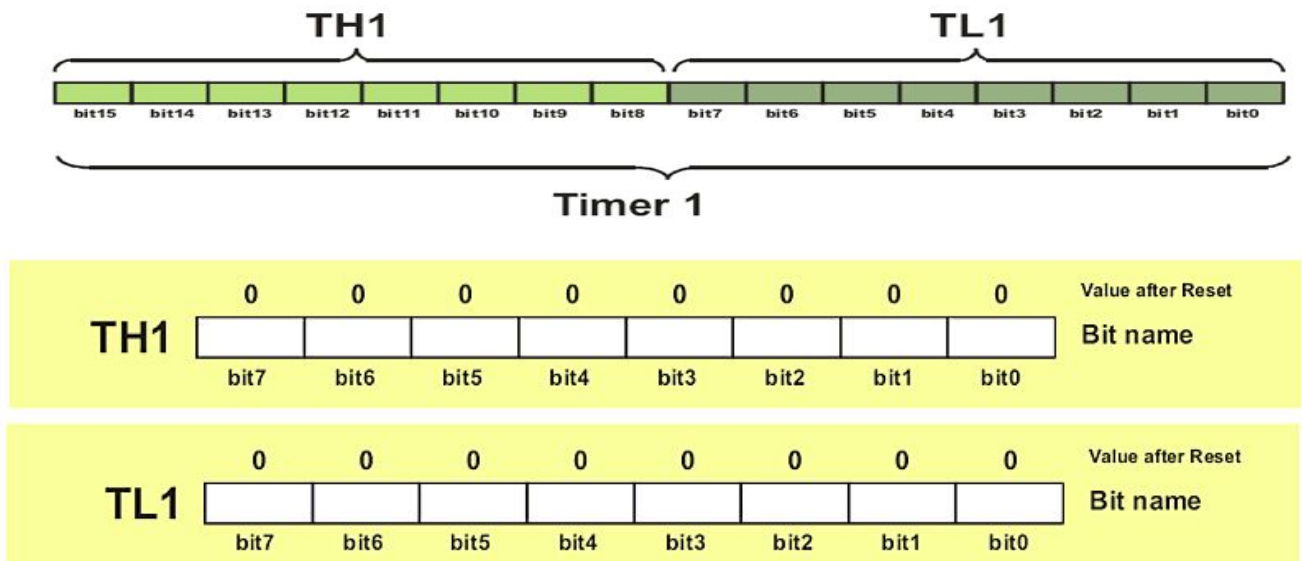
Only 4 bits of this register are used for this purpose, while rest of them is used for interrupt control to be discussed later.



- **TF1** bit is automatically set on the Timer 1 overflow.
- **TR1** bit enables the Timer 1.
  - **1** - Timer 1 is enabled.
  - **0** - Timer 1 is disabled.
- **TF0** bit is automatically set on the Timer 0 overflow.
- **TR0** bit enables the timer 0.
  - **1** - Timer 0 is enabled.
  - **0** - Timer 0 is disabled.

### Timer 1

Timer 1 is identical to timer 0, except for mode 3 which is a hold-count mode. It means that they have the same function, their operation is controlled by the same registers TMOD and TCON and both of them can operate in one out of 4 different modes.



### Result:

Thus the 8051 Architecture has been studied.

### POST LAB QUESTION & ANSWERS

**1. What are the advantages of an assembly language in comparison with high level language?**

Assembly language can control the machine code better as compared to high level languages. Manipulation of bits is easier in assembly language as compared to high level languages. Assembly language can access any memory but the high level languages can't.

**2. What is the function of HOLD and HLDA signal?**

**HOLD** – This signal indicates that another master is requesting the use of the address and data buses. **HLDA (HOLD Acknowledge)** – It indicates that the CPU has received the HOLD request and it will relinquish the bus in the next clock cycle. HLDA is set to low after the HOLD signal is removed.

**3. What is the function of TRAP, RST7.5, RST6.5, RST5.5 interrupt?**

RST7.5. It is a maskable interrupt, having the second highest priority among all interrupts. When this interrupt is executed, the processor saves the content of the PC register into the stack and branches to 003CH address.

**4. What is the function of timing and control unit?**

It provides timing and control signal to the microprocessor to perform the various operation. It has three control signal. It controls all external and internal circuits. It operates with reference to clock signal. It synchronizes all the data transfers.

**5. What is the function of SID and SOD pin?**

There are 2 serial signals, i.e. SID and SOD and these signals are used for serial communication. SOD (Serial **output** data line) – The **output** SOD is set/reset as specified by the SIM instruction. SID (Serial **input** data line) – The data on this line is loaded into accumulator whenever a RIM instruction is executed.