

CS 211

LAB 8: Datapath Implementation

Name – Gautam Kumar Mahar

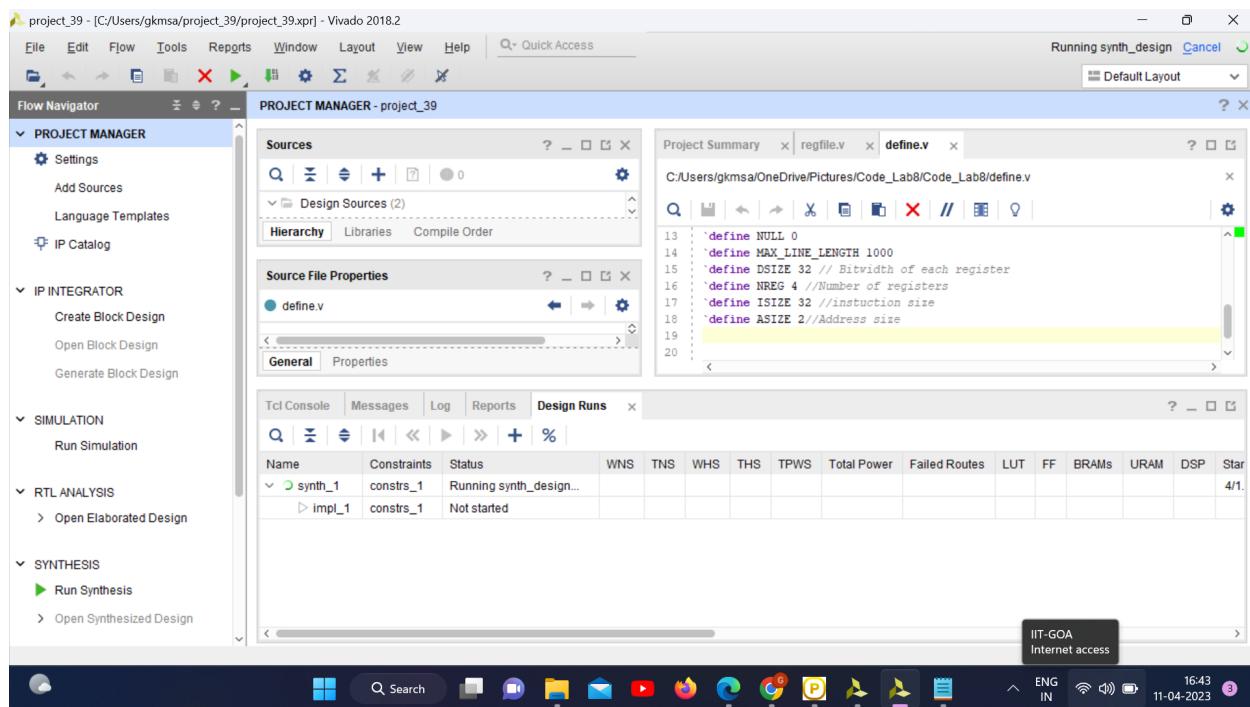
Roll No. – 2103114

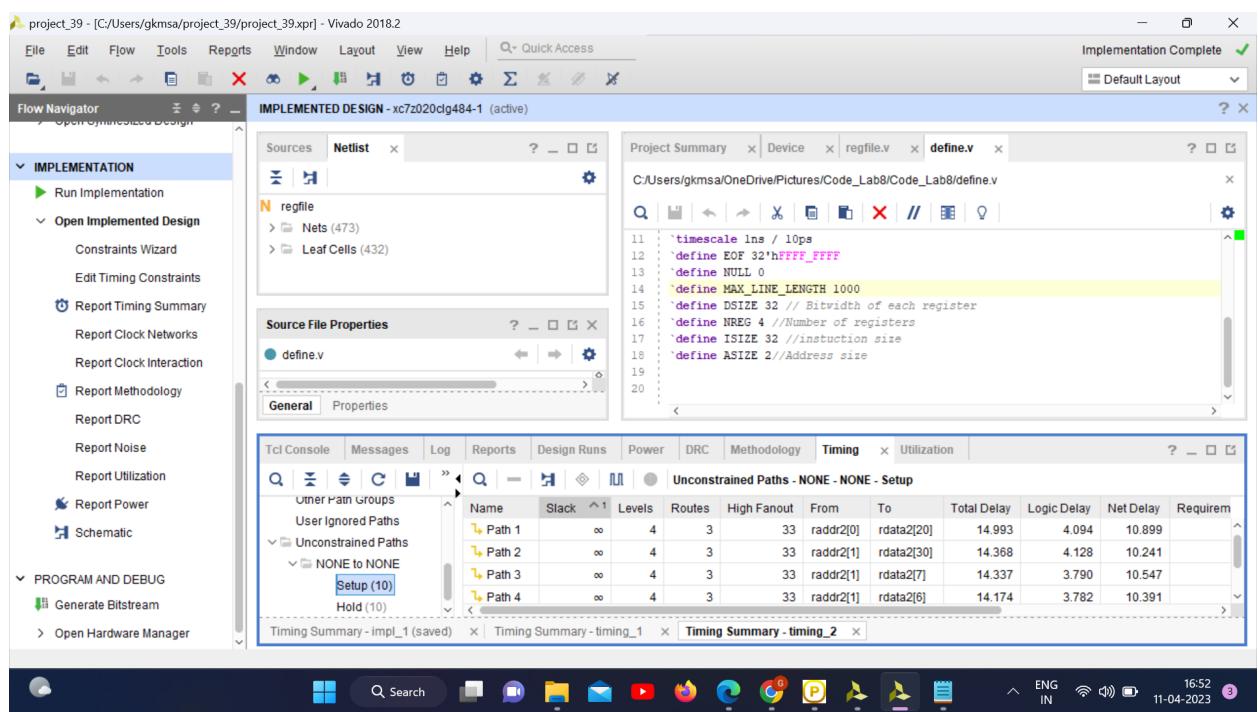
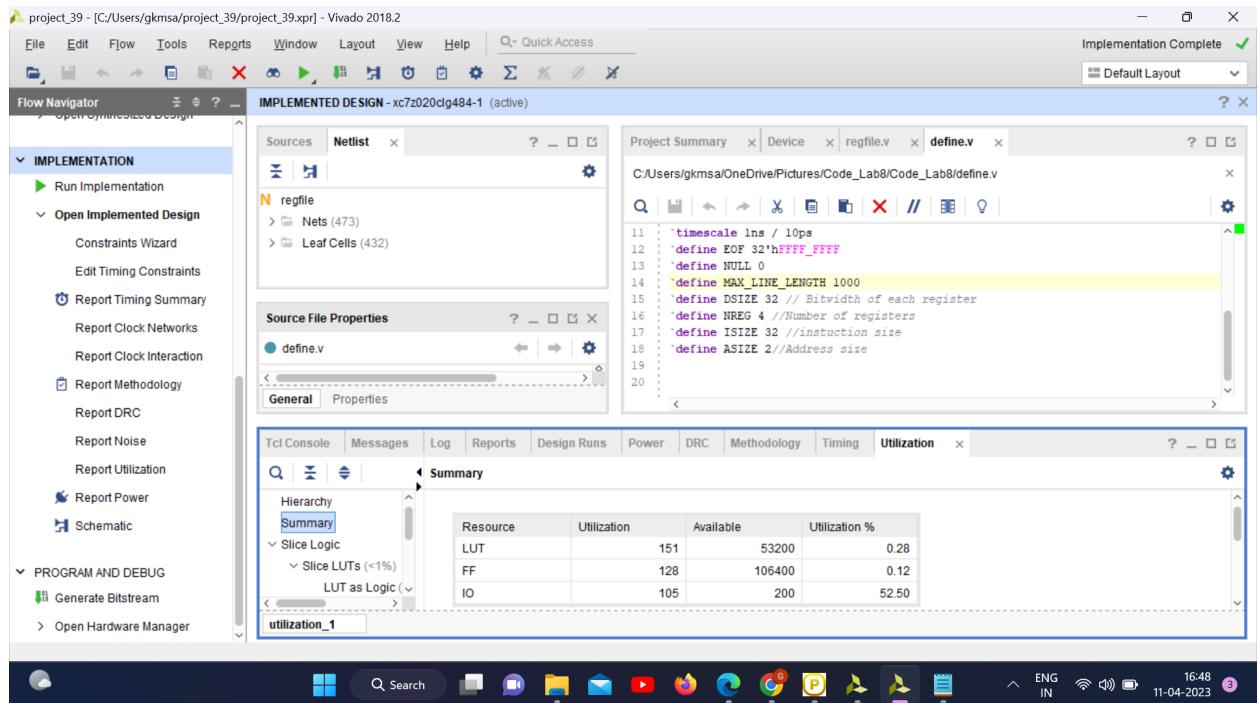
Branch – Computer Science Engineering

Question 1

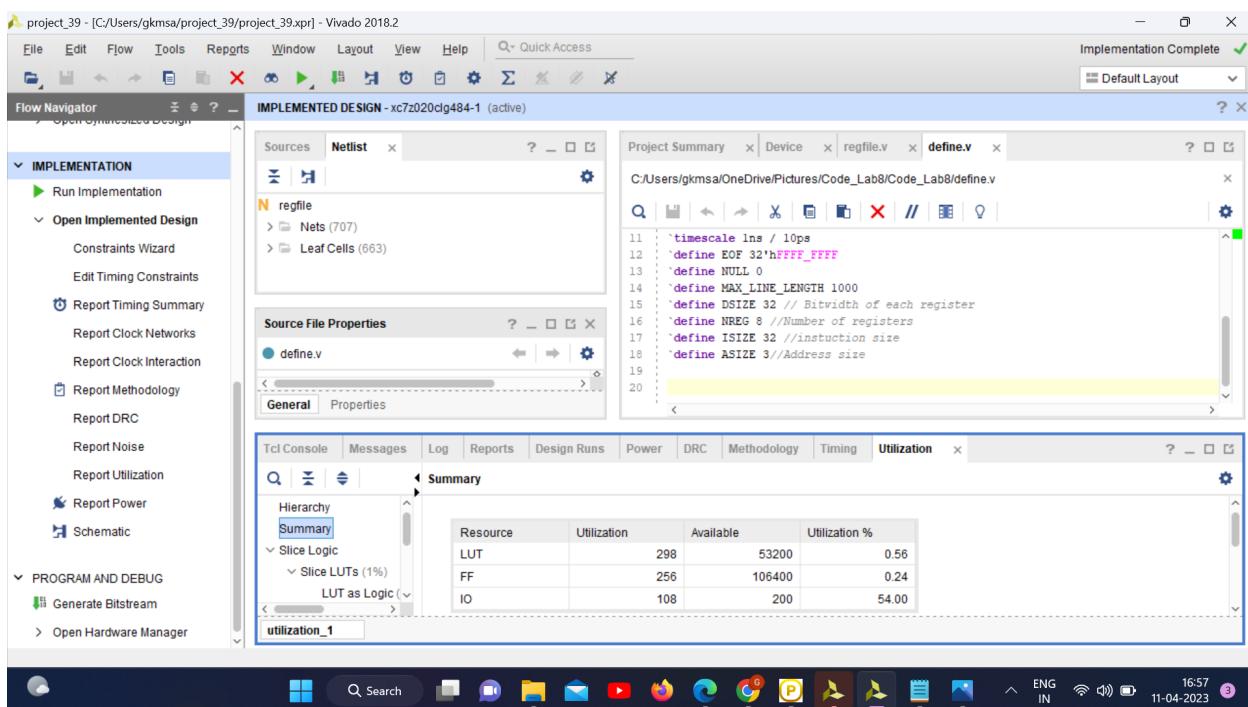
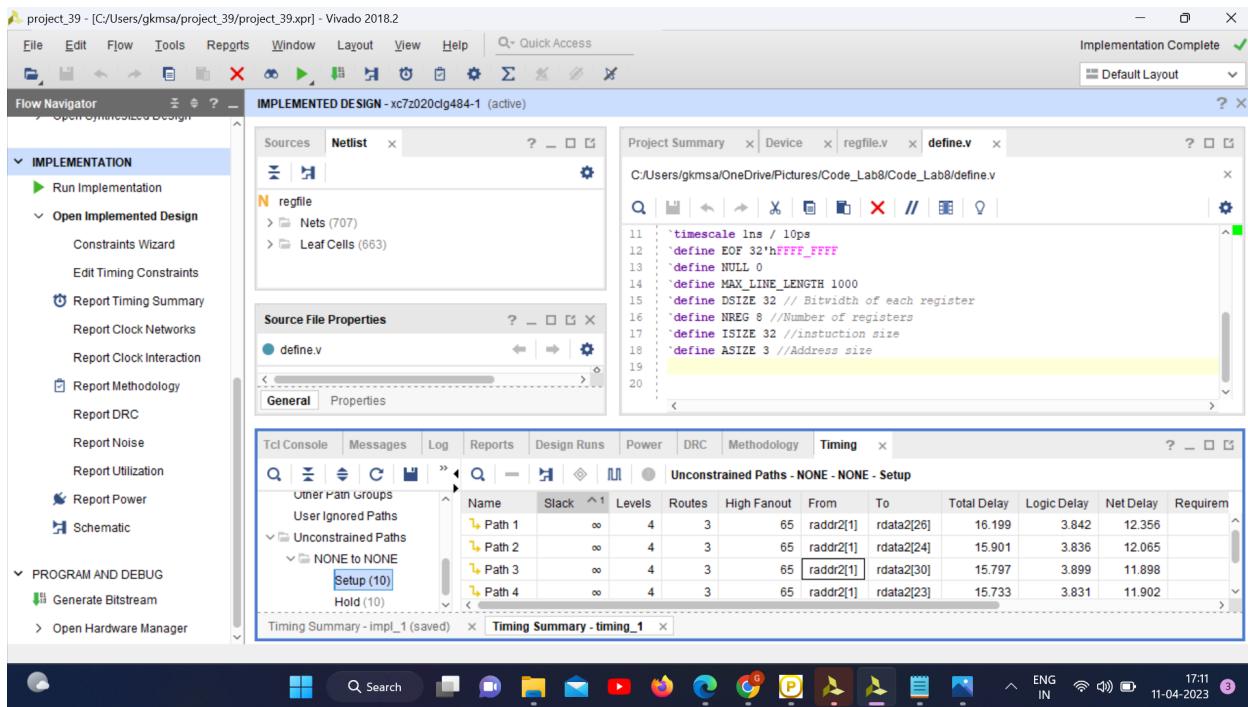
Plot the graph, area in LUT slices (vs) No. of registers (NREG) and a delay (vs) No. of registers (NREG) for the register file module for NREG =4, 8, 16, 32, 64. Set DSIZE (bit-width of each register) = 32.

Start NREG = 4

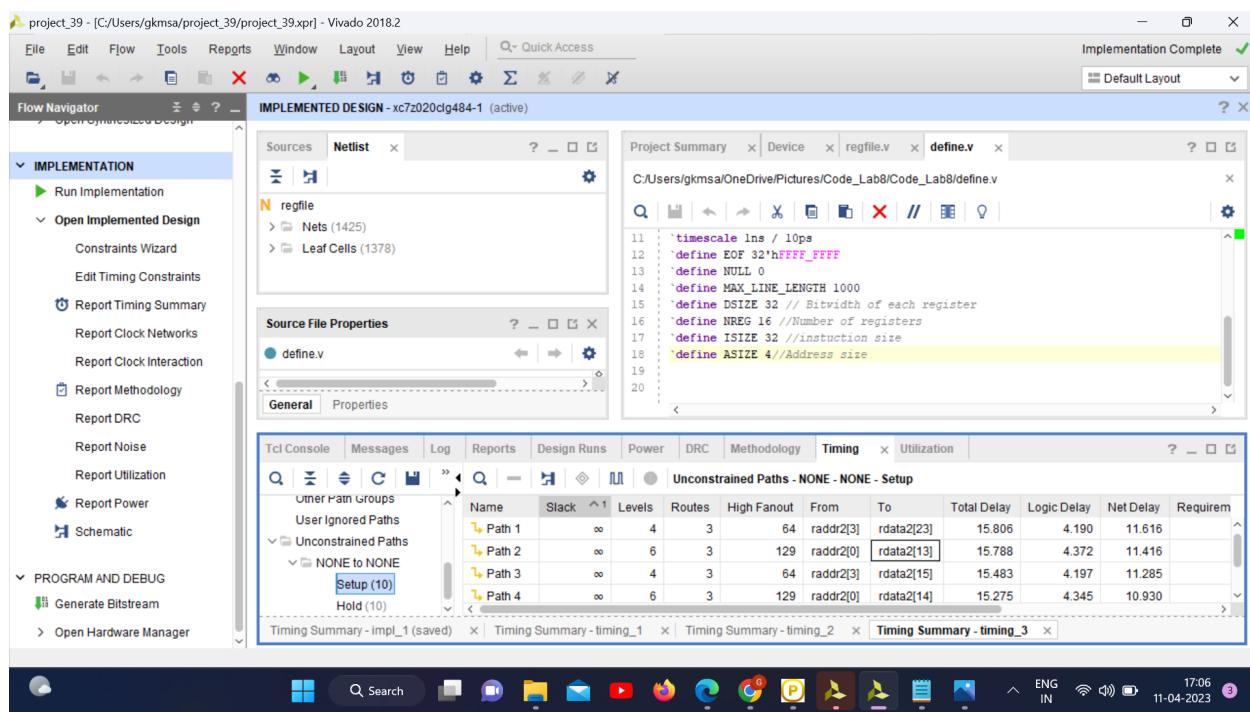
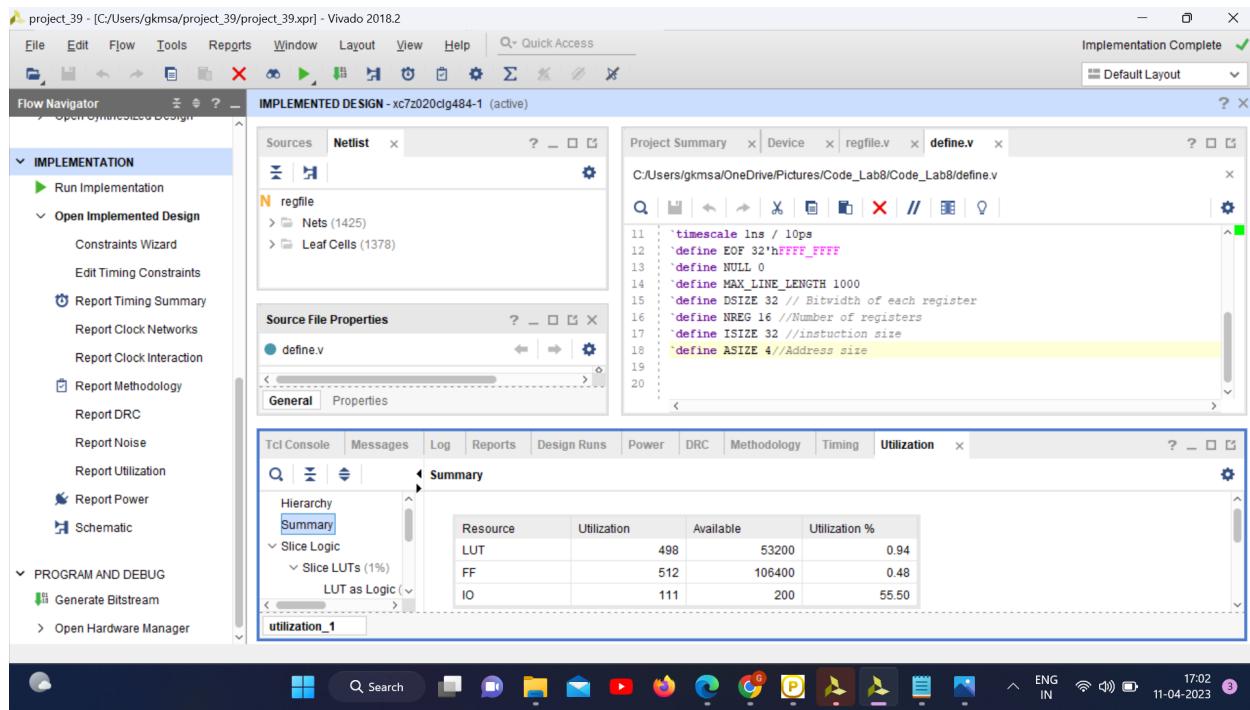




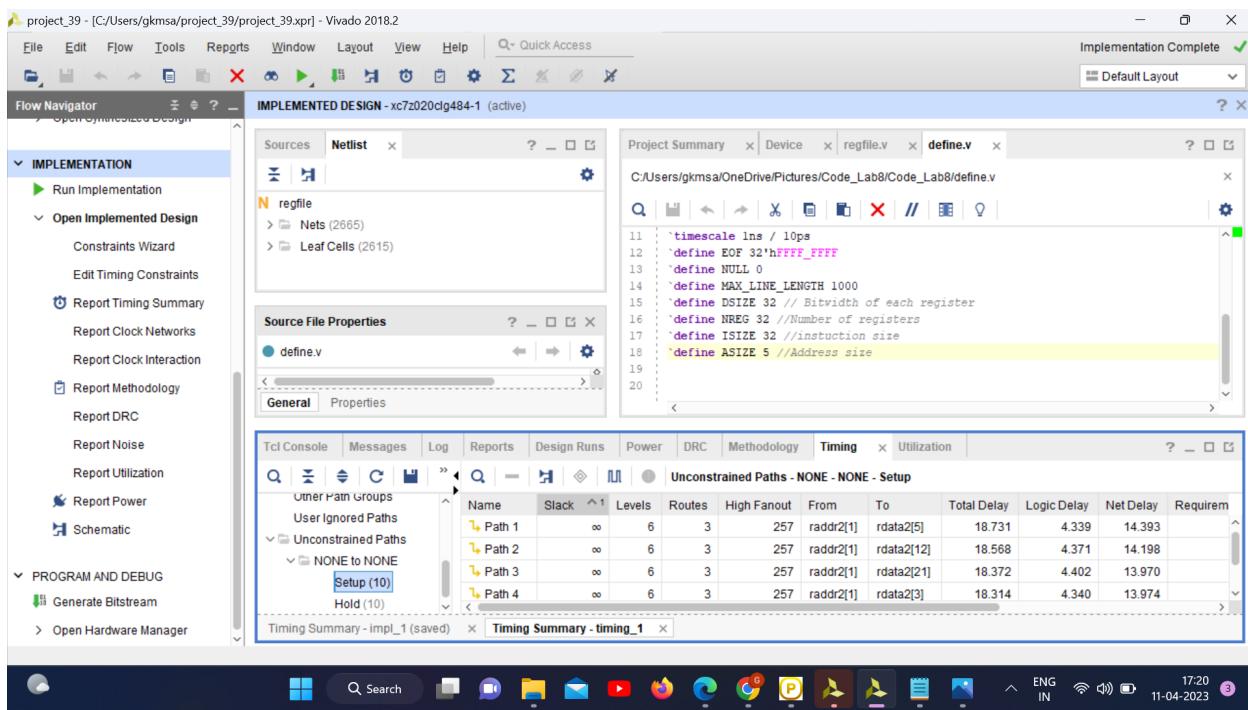
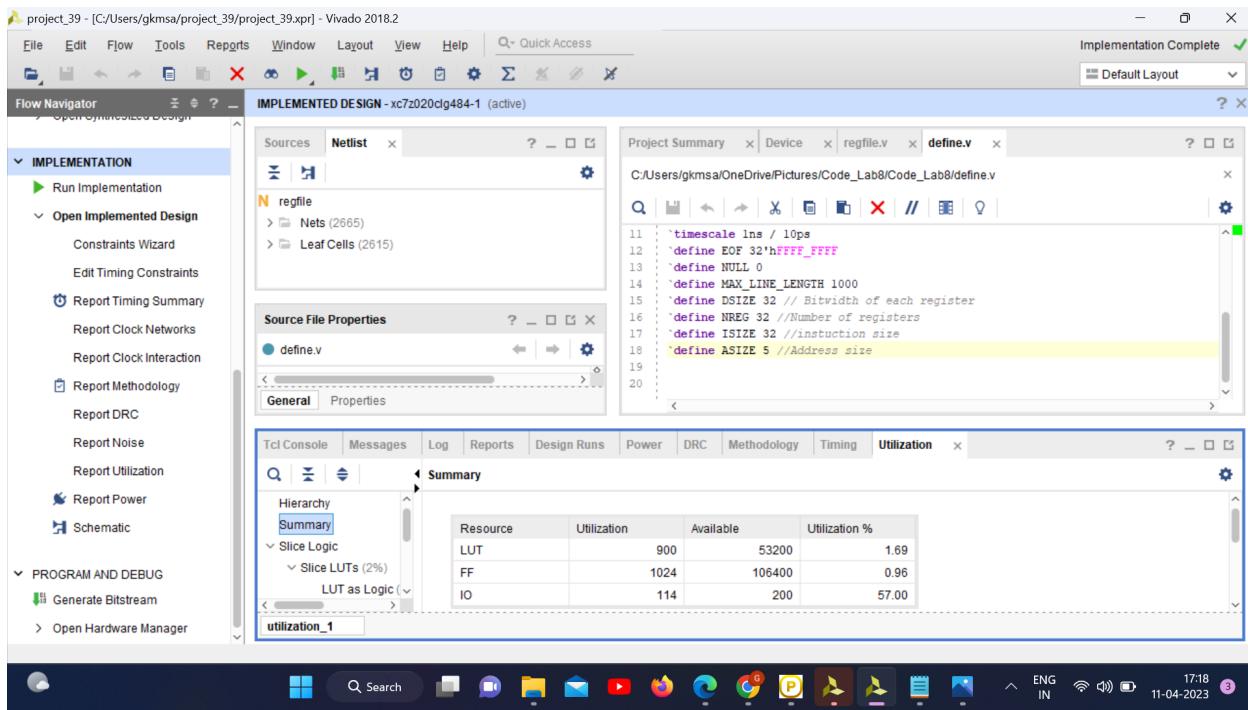
Start NREG = 8



Start NREG = 16

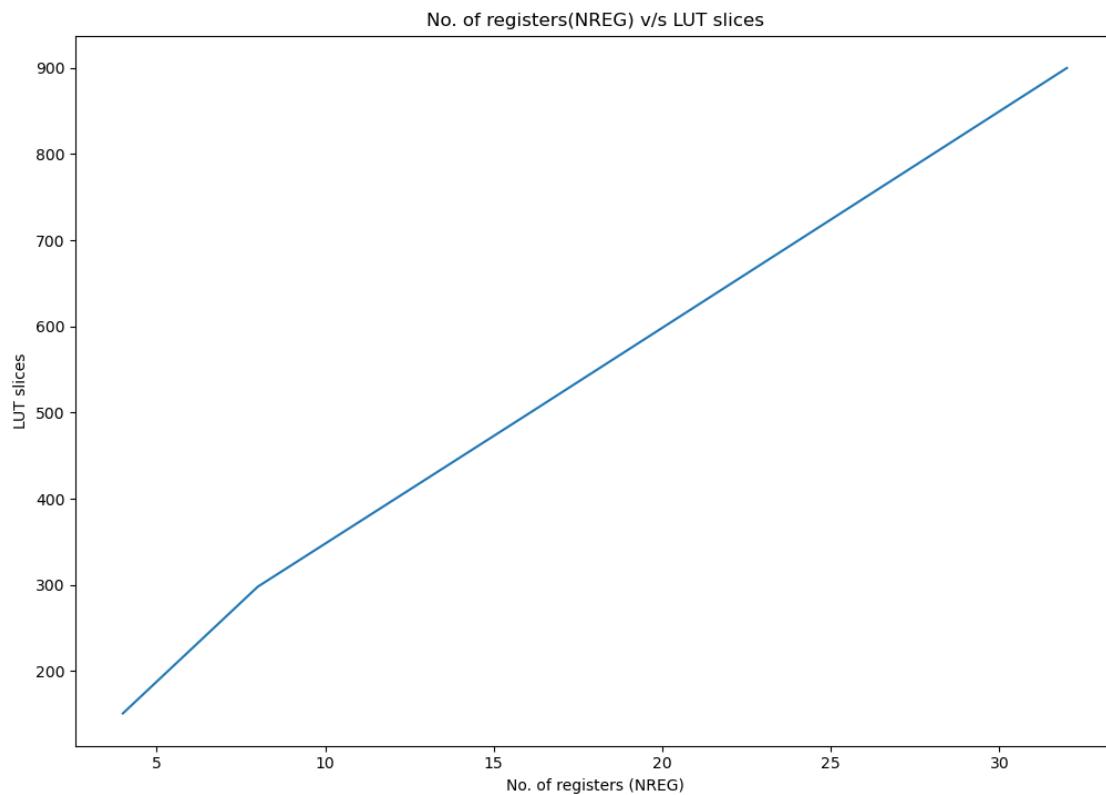


Start NREG = 32

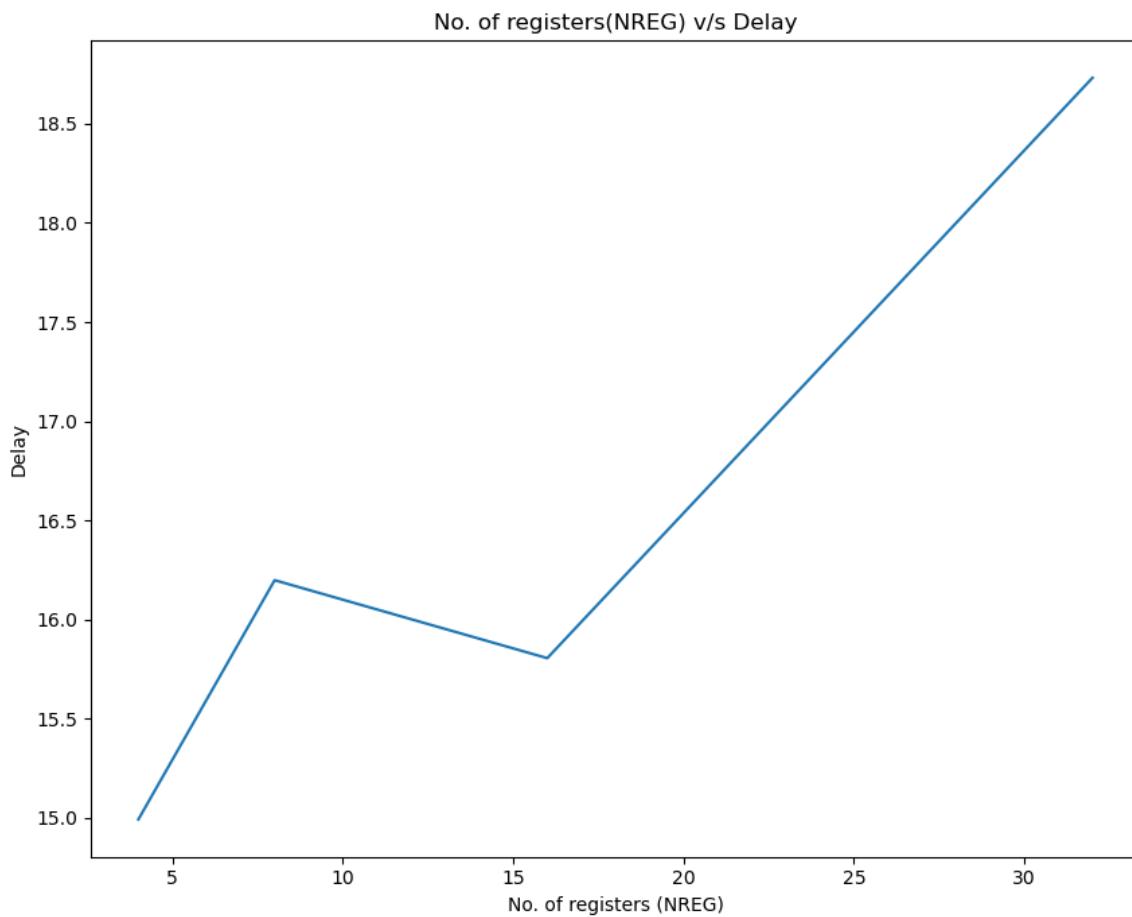


No. of Registers(NREG)	Bit-width of the register (DSIZE)	No of register slices used	No of LUT slices used	Minimum clock Period in ns
4	32	128	151	14.993
8	32	256	298	16.199
16	32	512	498	15.806
32	32	1024	900	18.731

Plot graph, No. of registers (NREG) v/s area in LUT slices



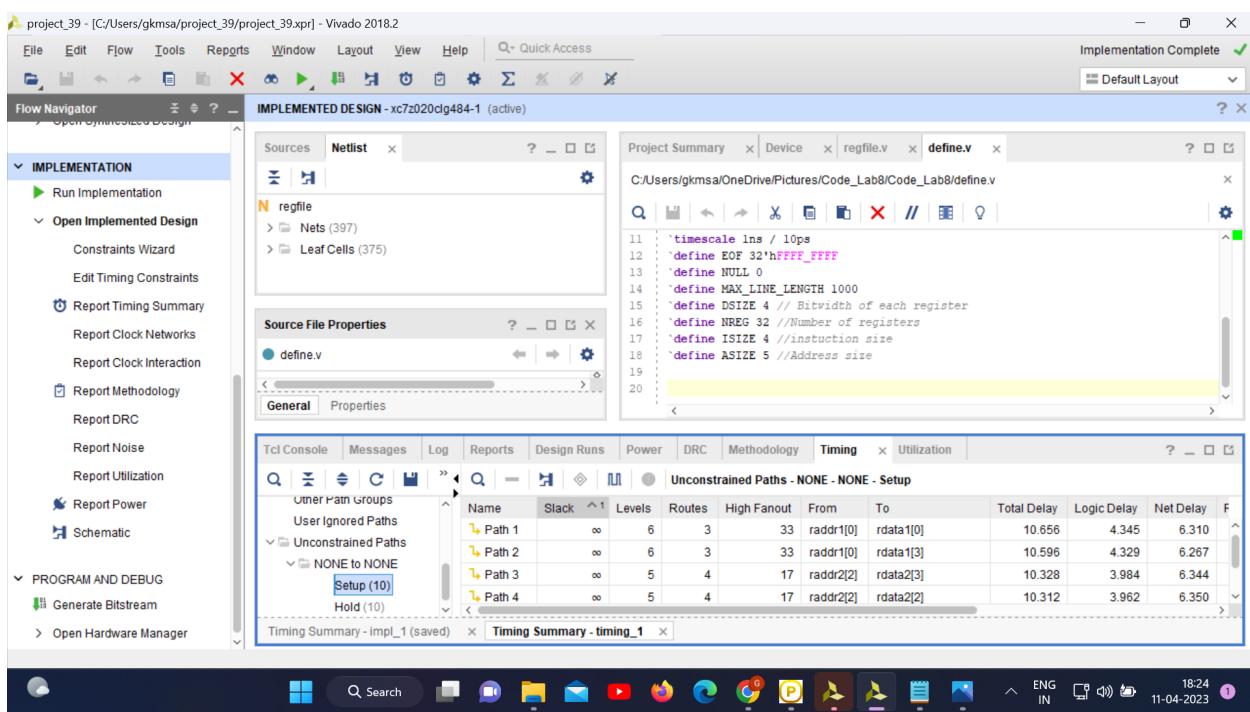
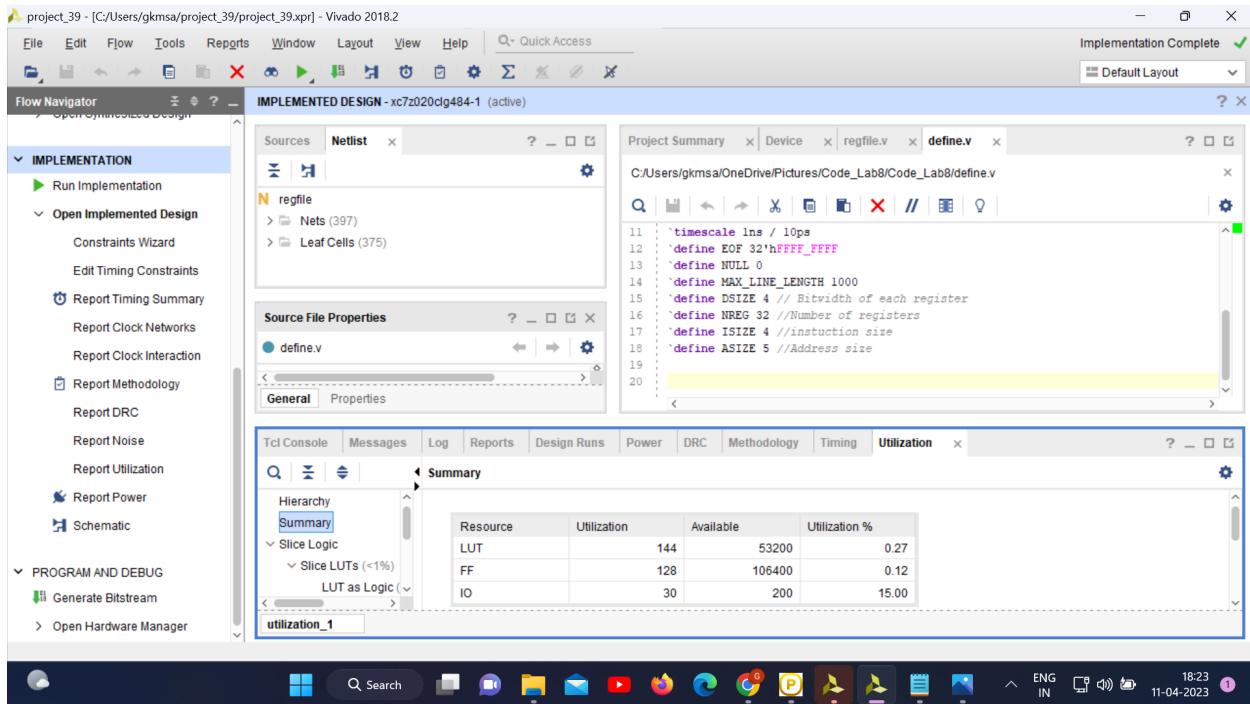
Delay (vs) No. of registers (NREG)



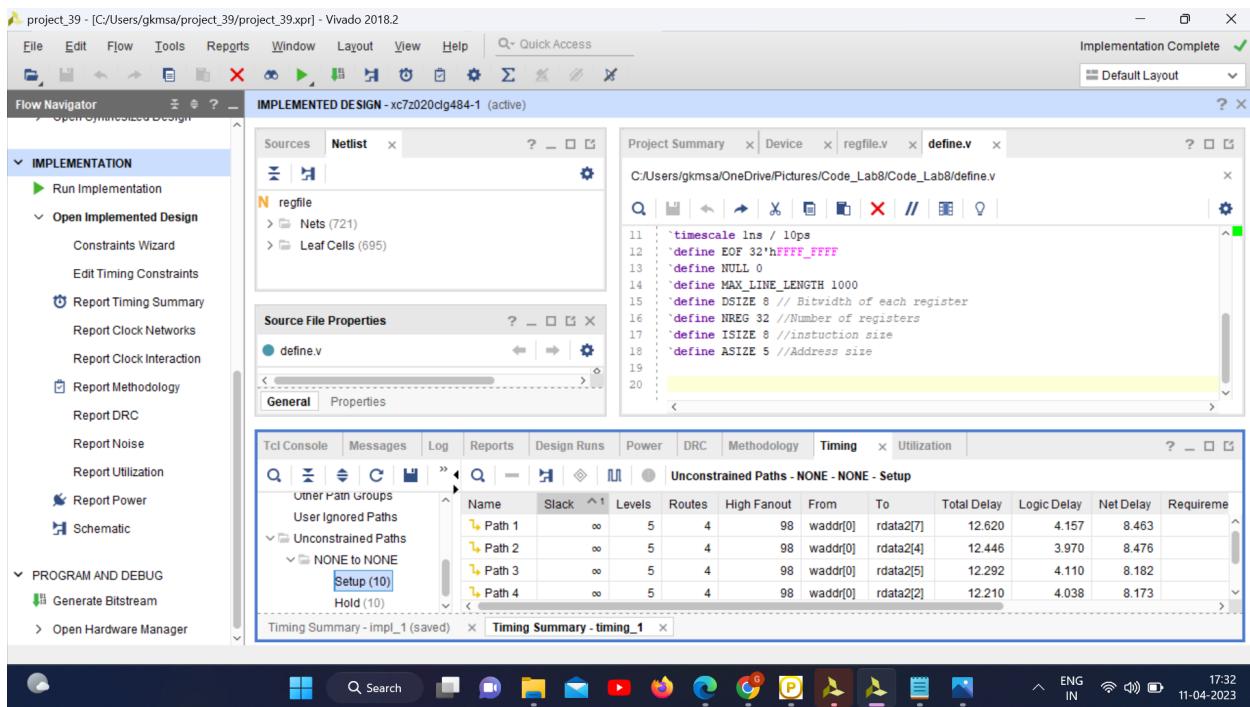
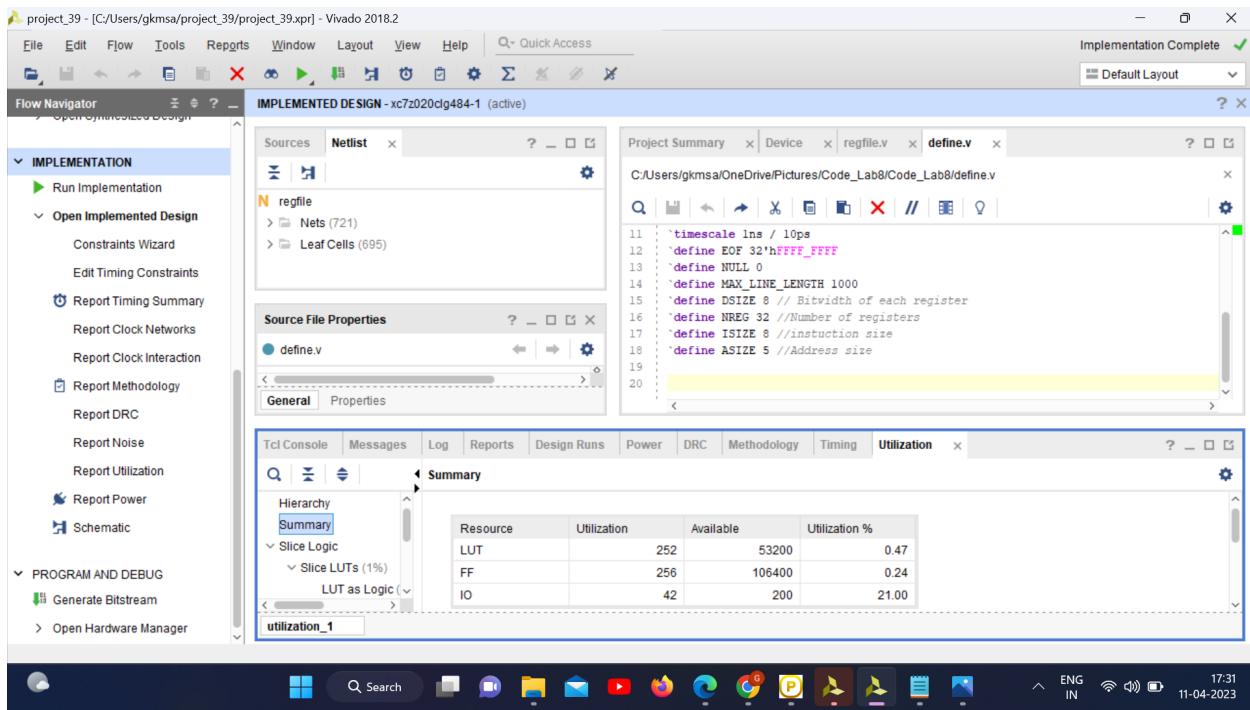
Question 2

Plot the graph, area in LUT slices (vs) bit-width of the register (DSIZE) as well as a delay (vs) bit-width of the register (DSIZE) for the register file module for DSIZE =4, 8, 16, 32, 64. Set NREG (number of registers) =32.

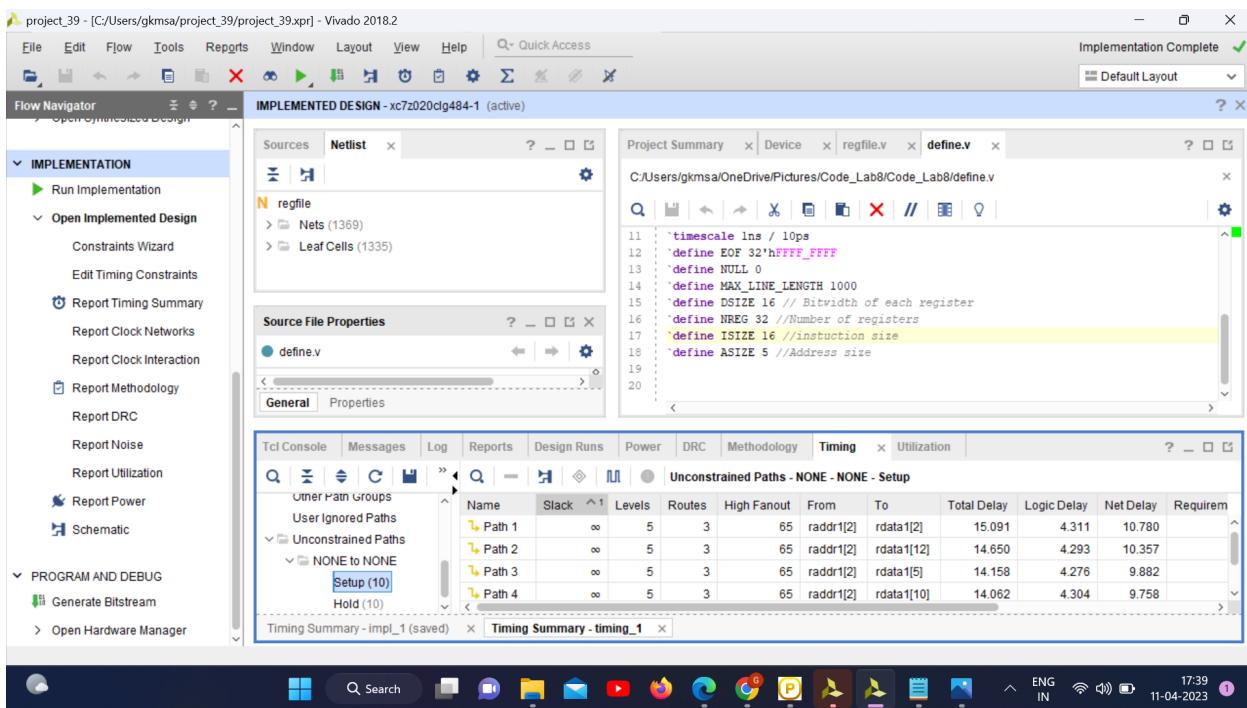
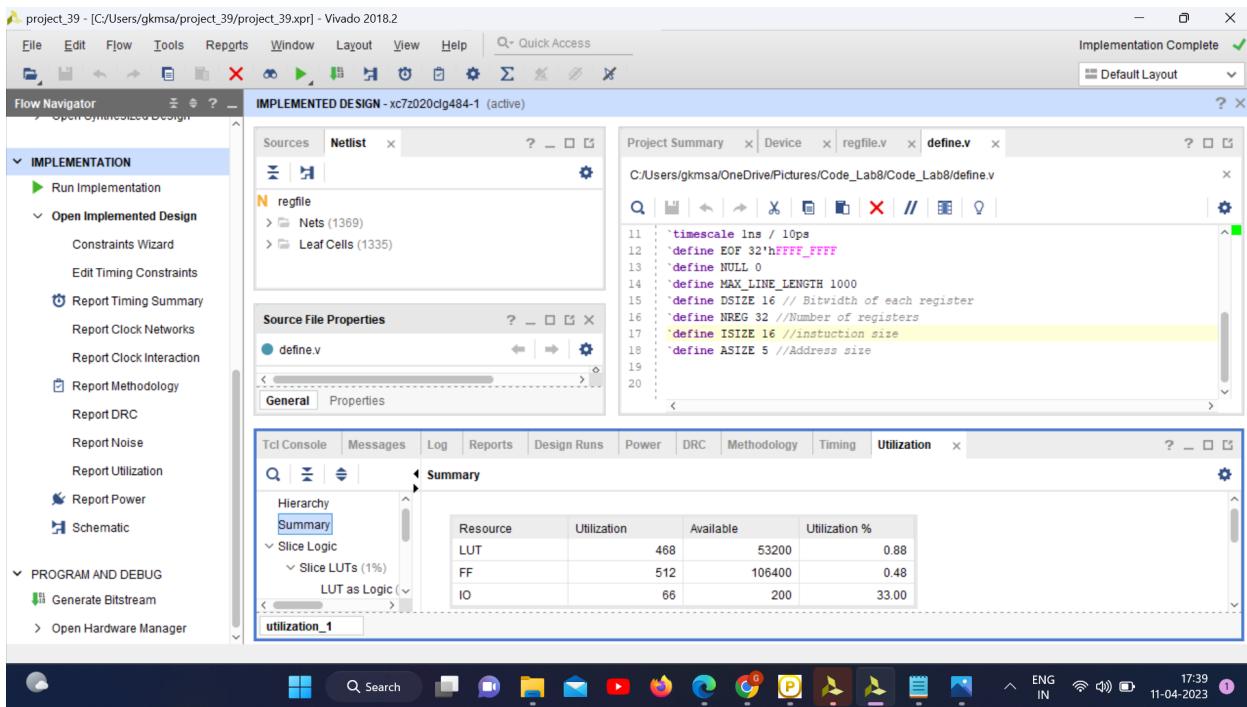
Start DSIZE = 4



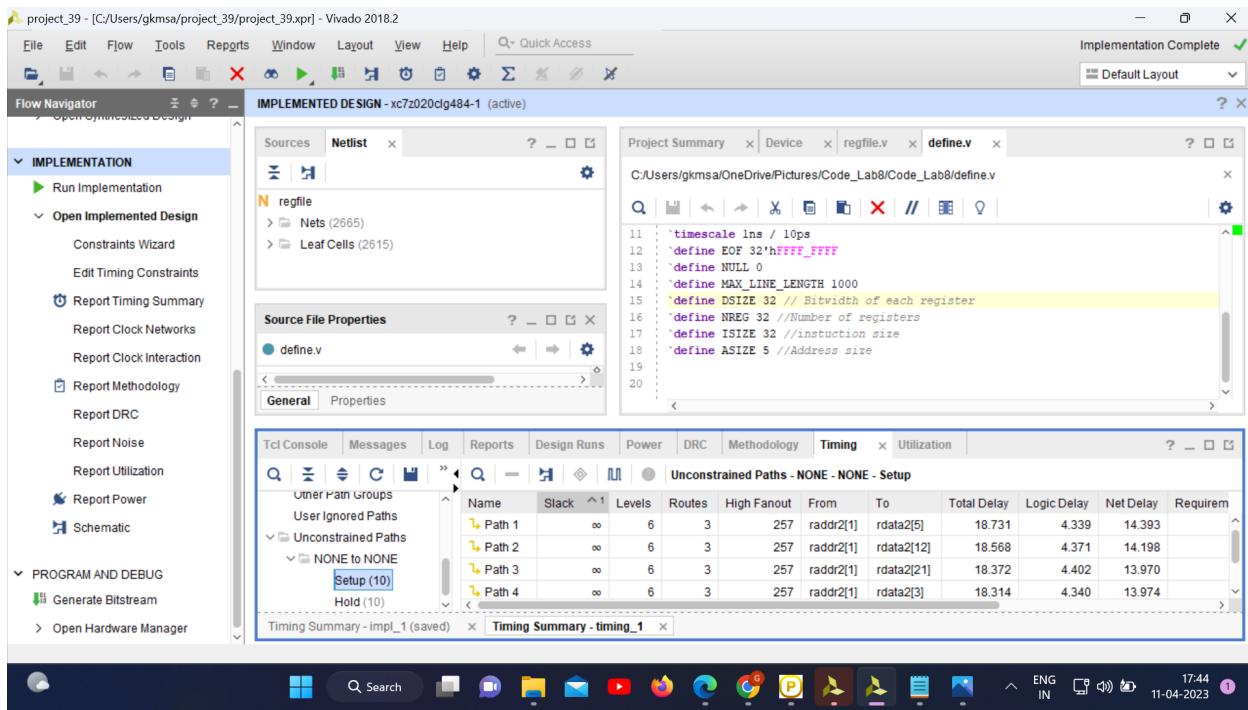
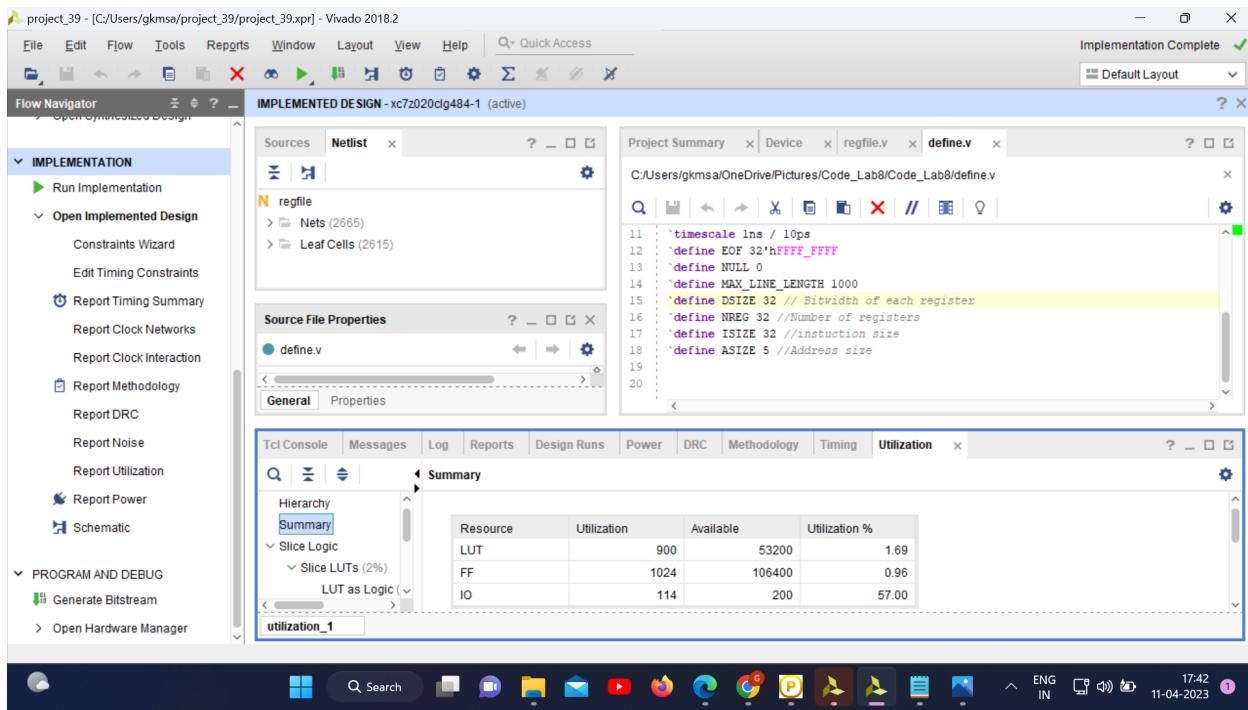
Start DSIZE = 8



Start DSIZE = 16

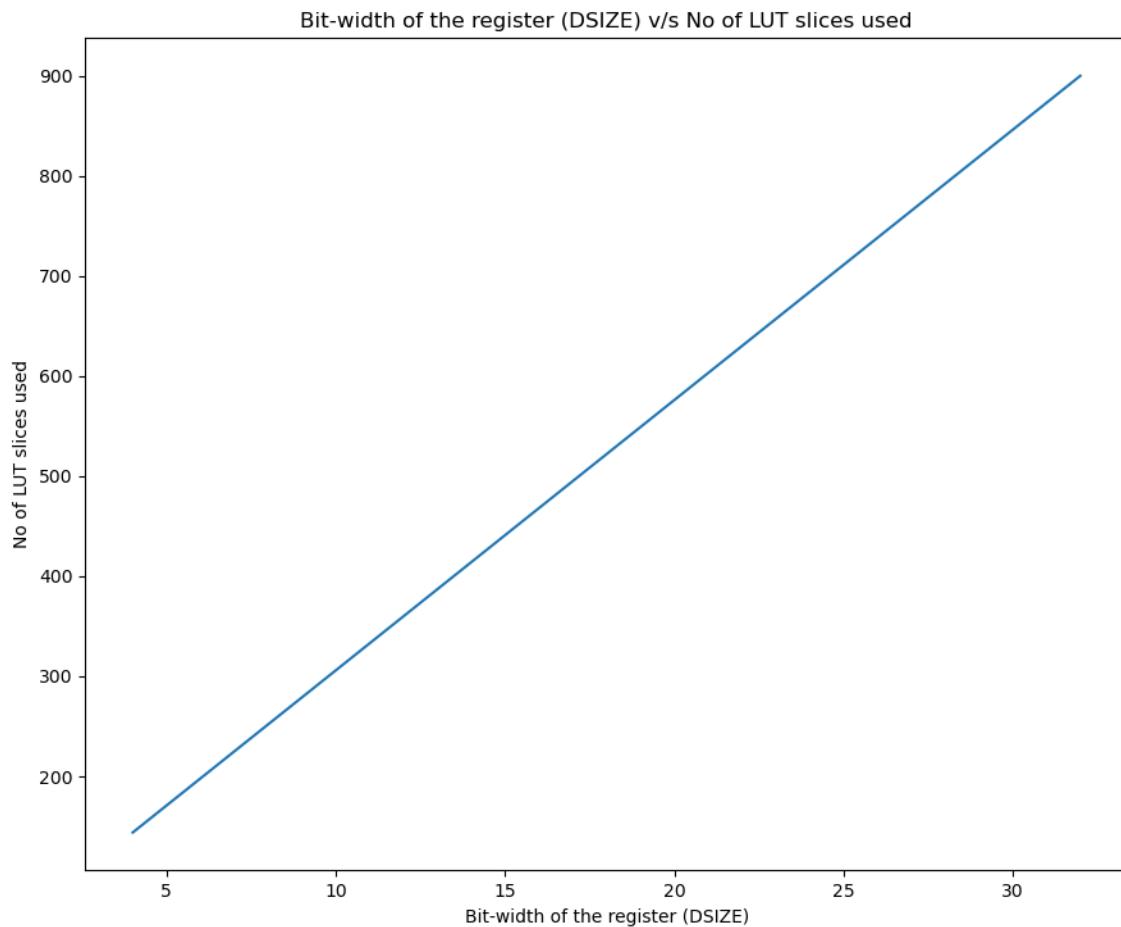


Start DSIZE = 32

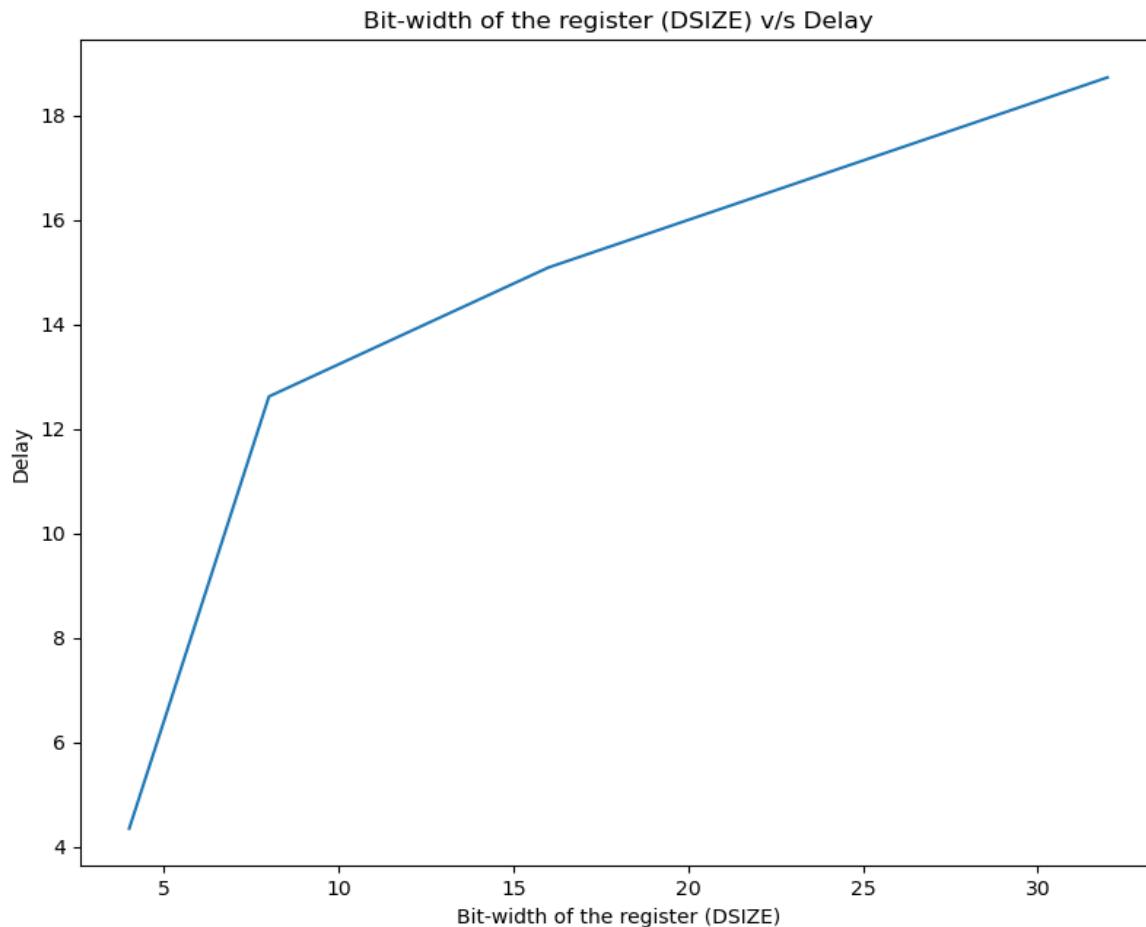


Bit-width of the register (DSIZE)	No. of registers (NREG)	No of register slices used	No of LUT slices used	Minimum clock Period in ns
4	32	128	144	4.345
8	32	256	252	12.620
16	32	512	468	15.091
32	32	1024	900	18.731

Plot the graph, an area in LUT slices (vs) bit-width of the register (DSIZE)



Delay (vs) bit-width of the register (DSIZE).



Thank You