

# CS 211

## LAB 7: Arithmetic Circuits and ALU

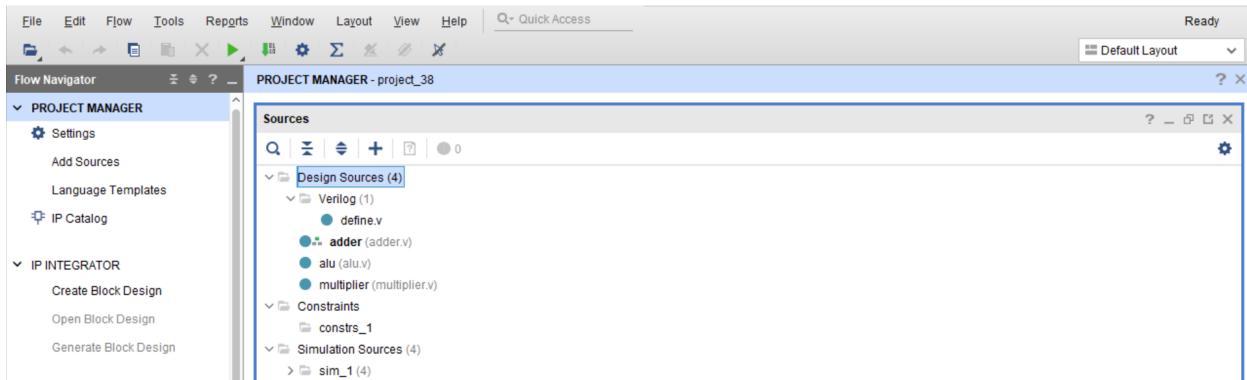
Name – Gautam Kumar Mahar

Roll No. – 2103114

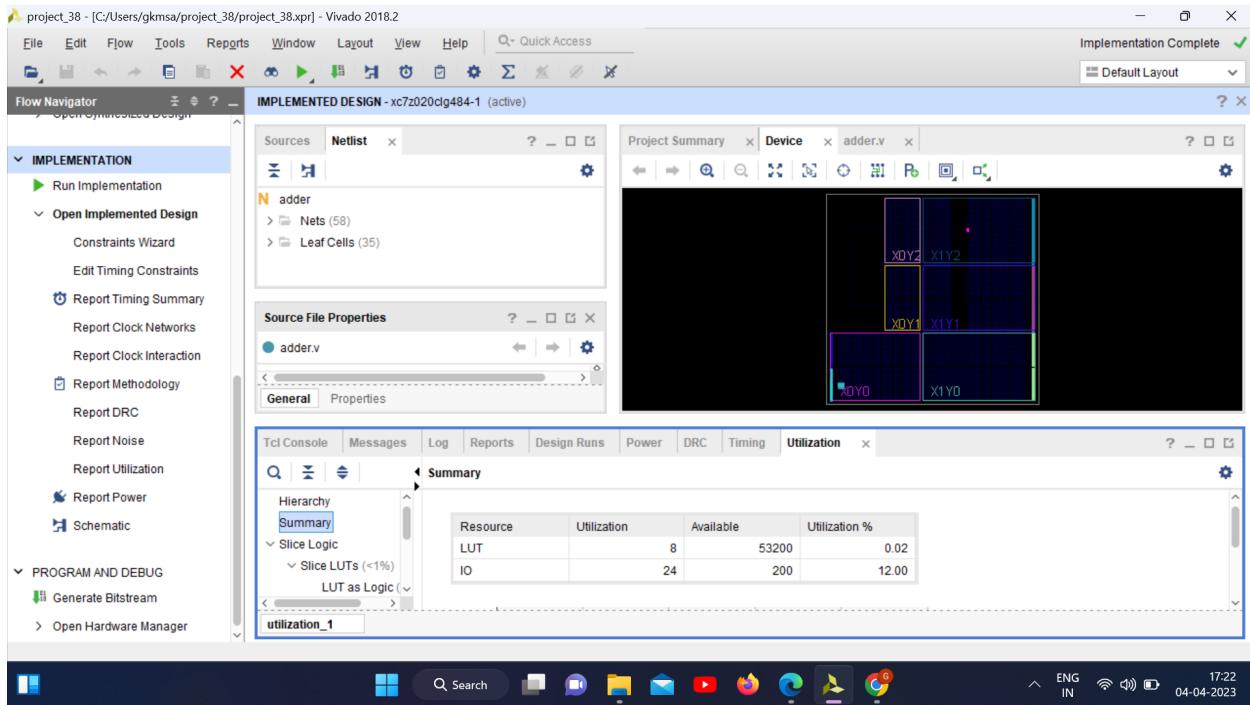
Branch – Computer Science Engineering

1. Plot the graph, area (vs) bit-width and delay (vs) bit-width for the ALU module for DSIZE = 8 and 16.

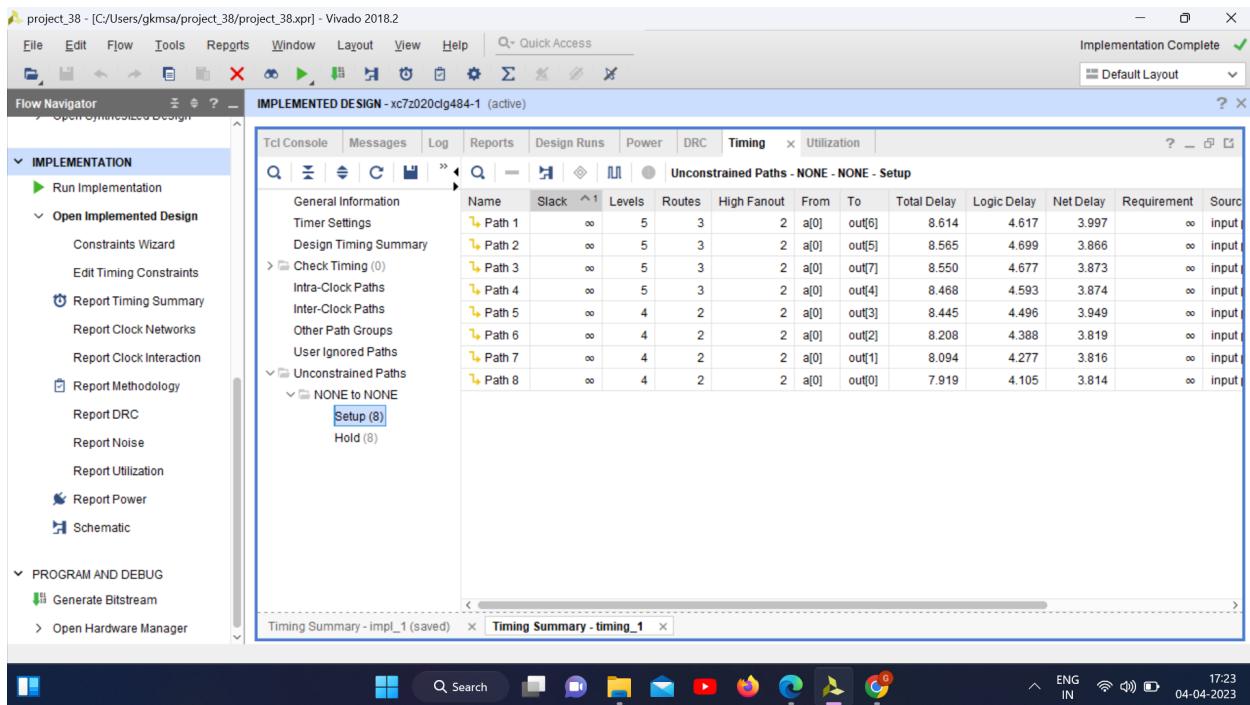
### adder ( DSIZE = 8 )



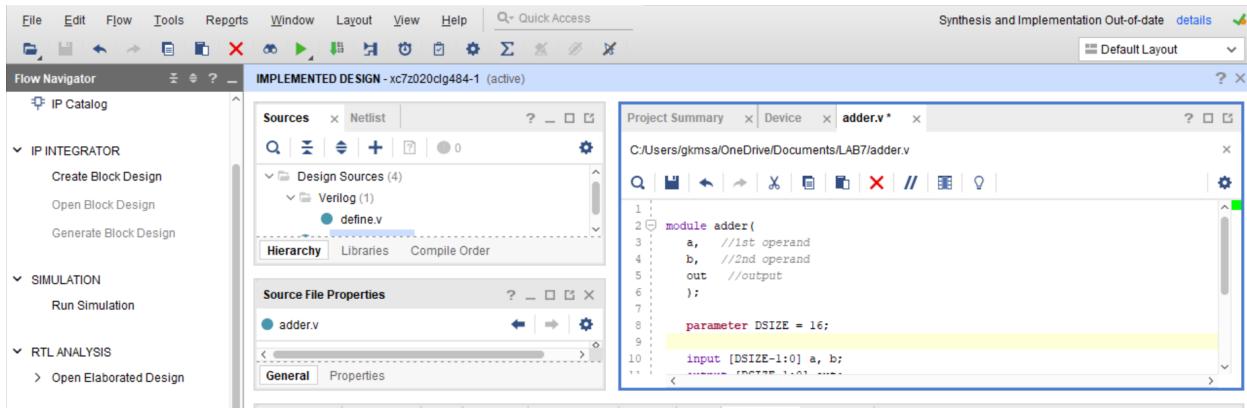
## Report Utilization



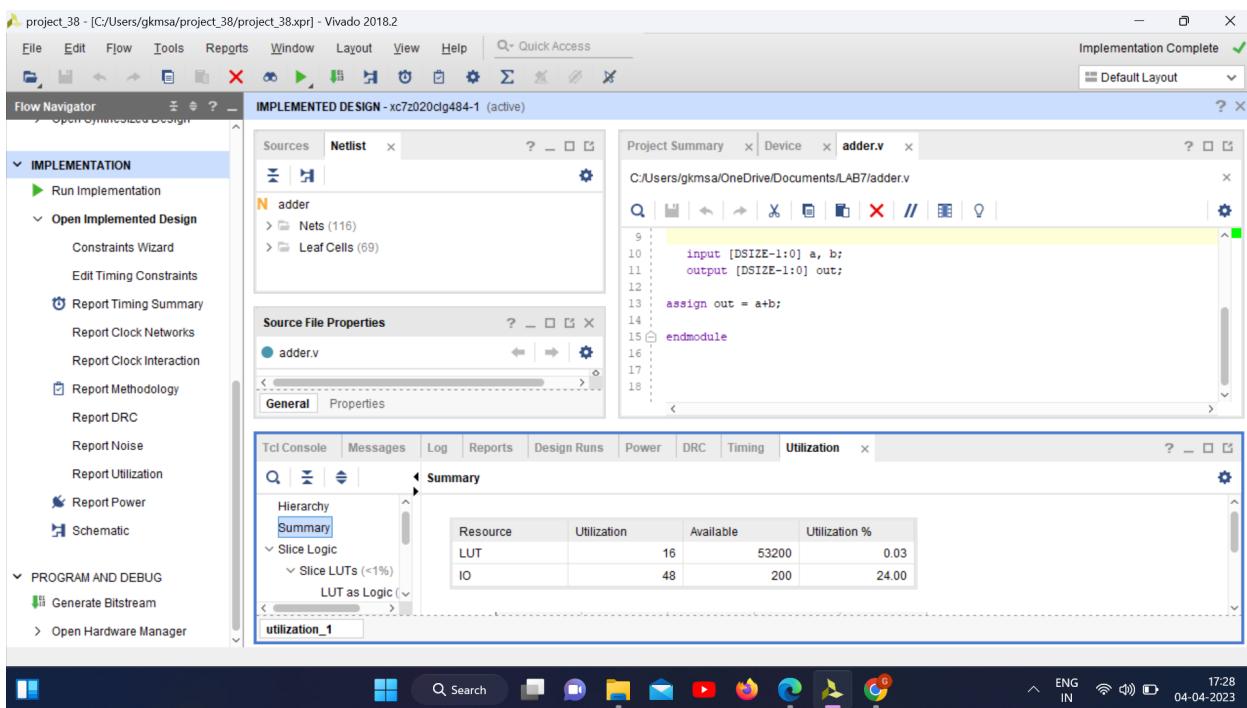
## Report Timing Summary



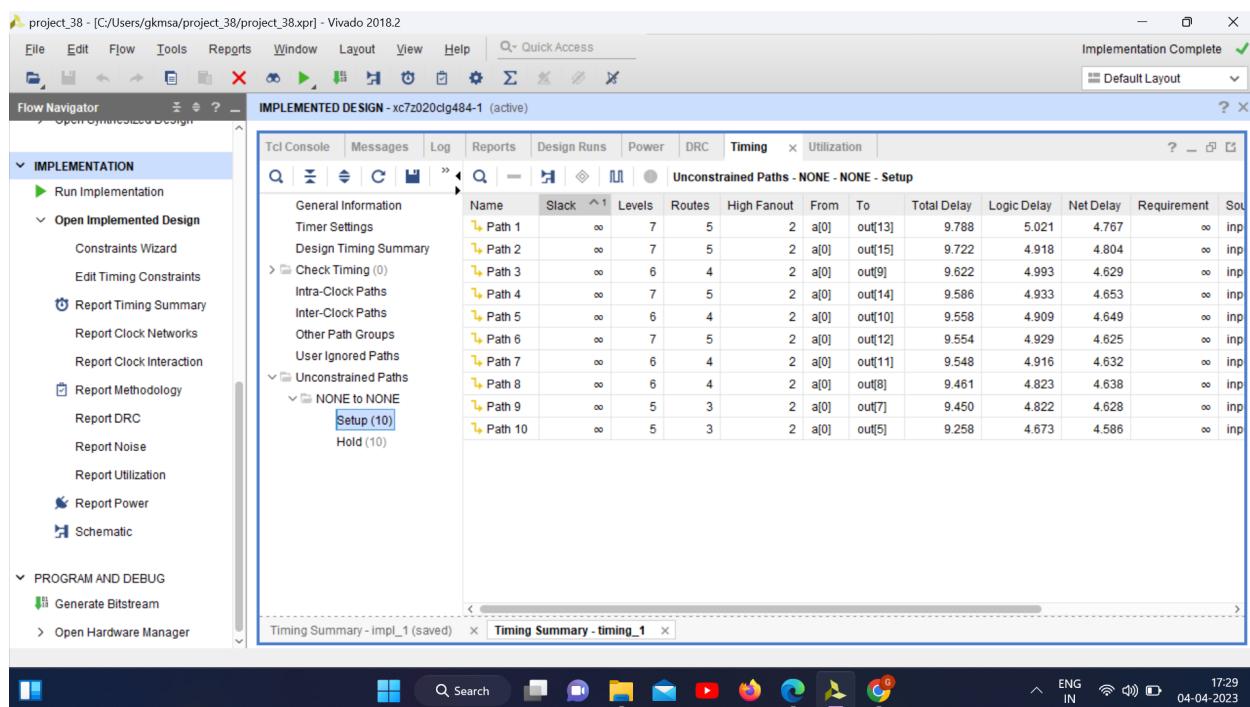
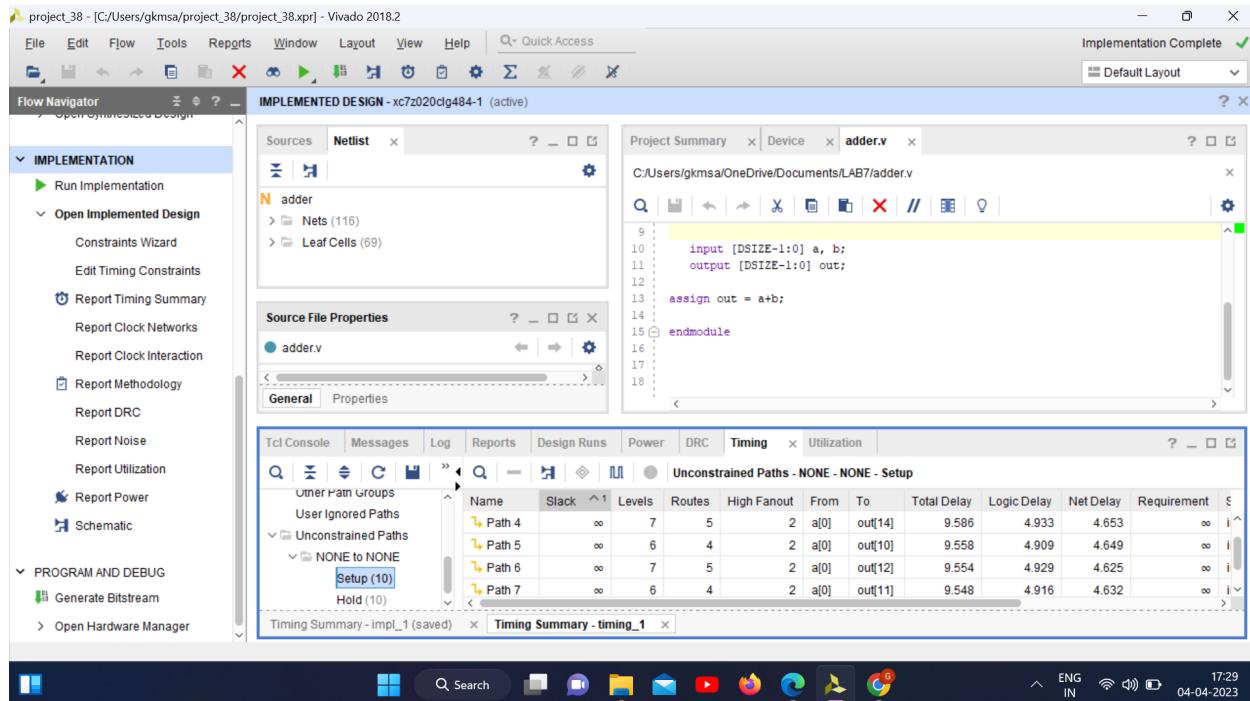
## adder ( DSIZE = 16 )



## Report Utilization

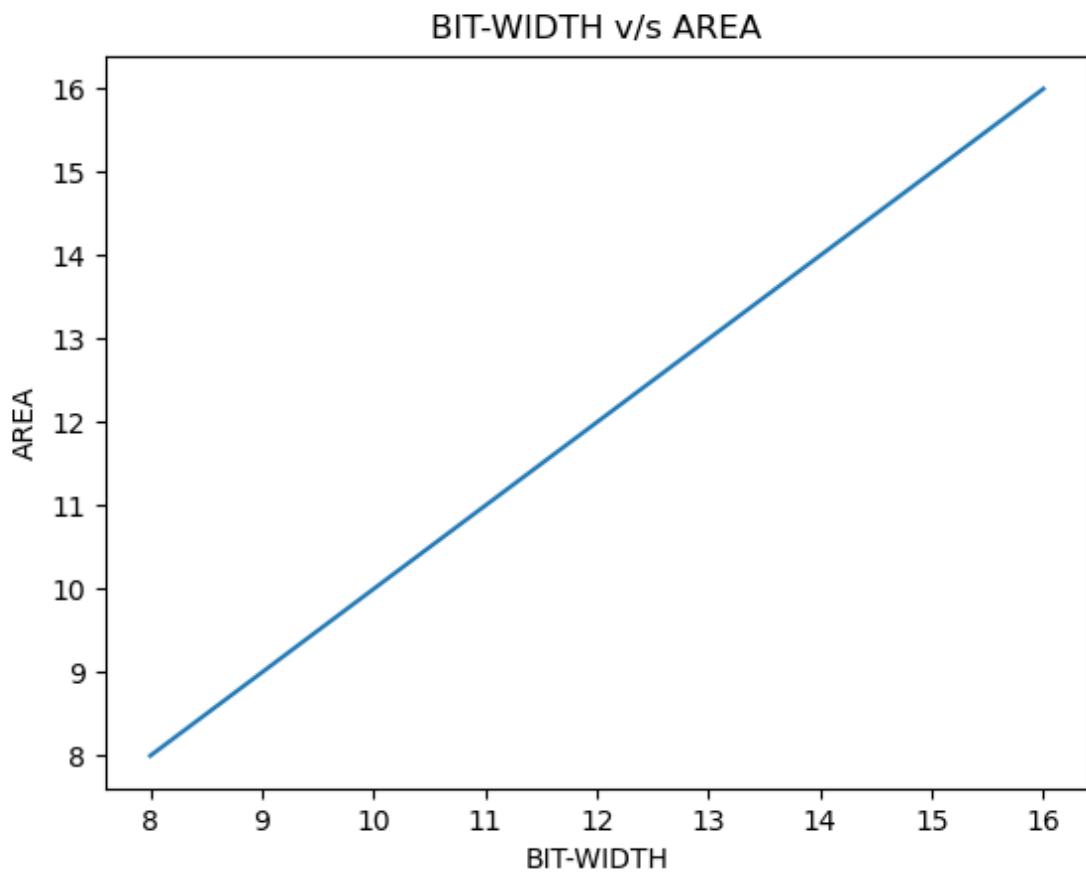


## Report Timing Summary

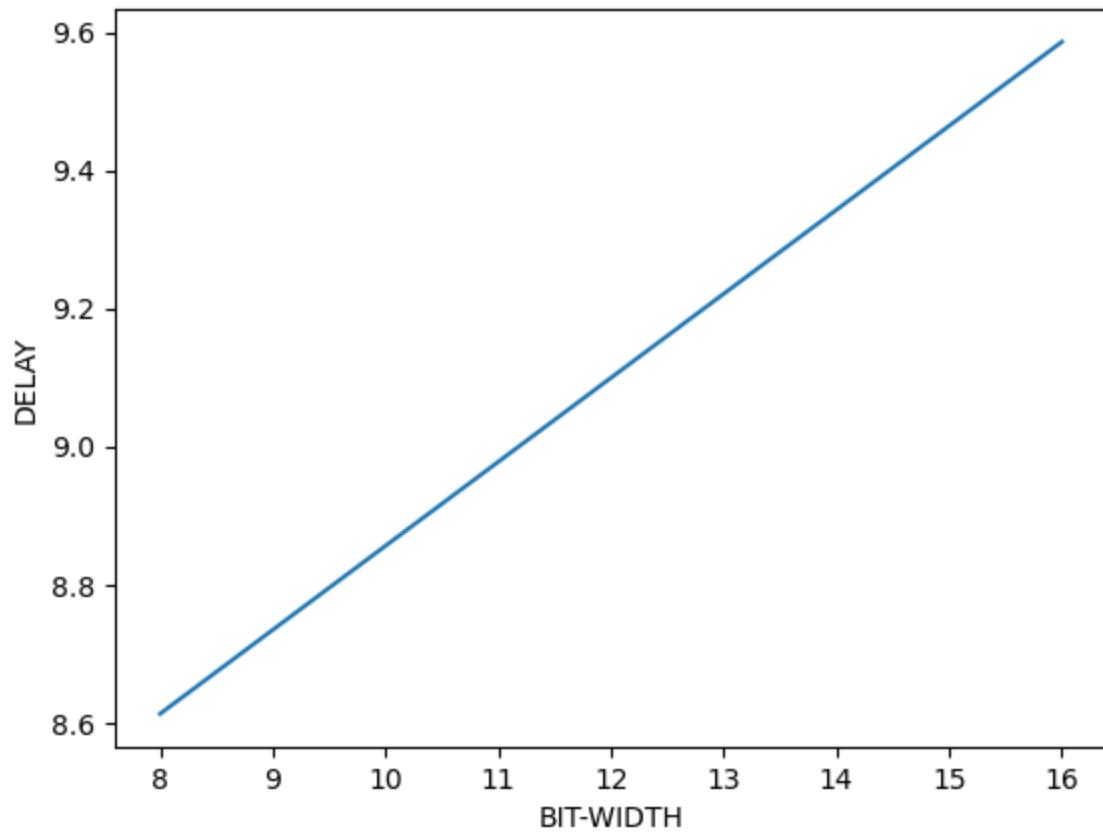


## adder- graph

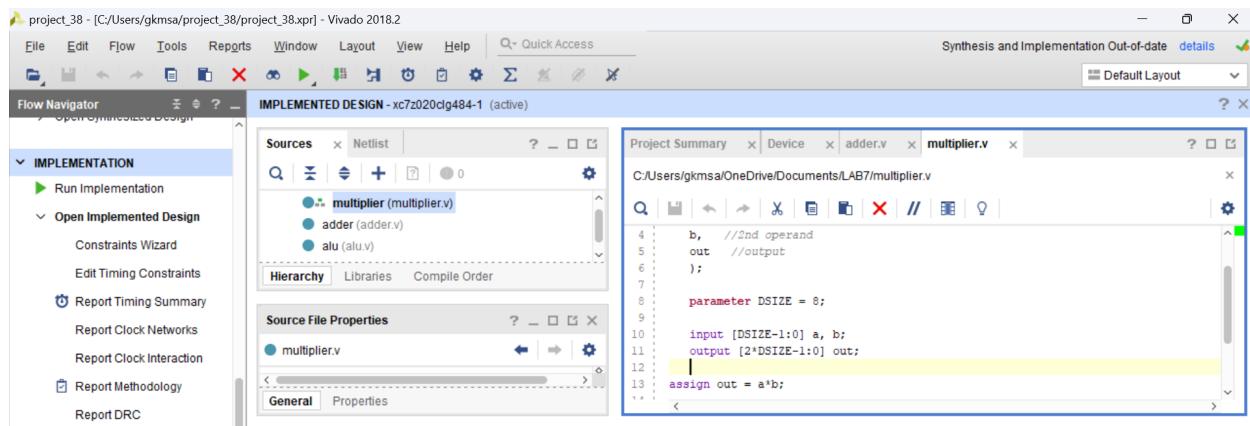
DSIZE	BIT-WIDTH	No of slices	Delay in ns
8	8	8	<u>8.614</u>
16	16	16	<b>9.586</b>



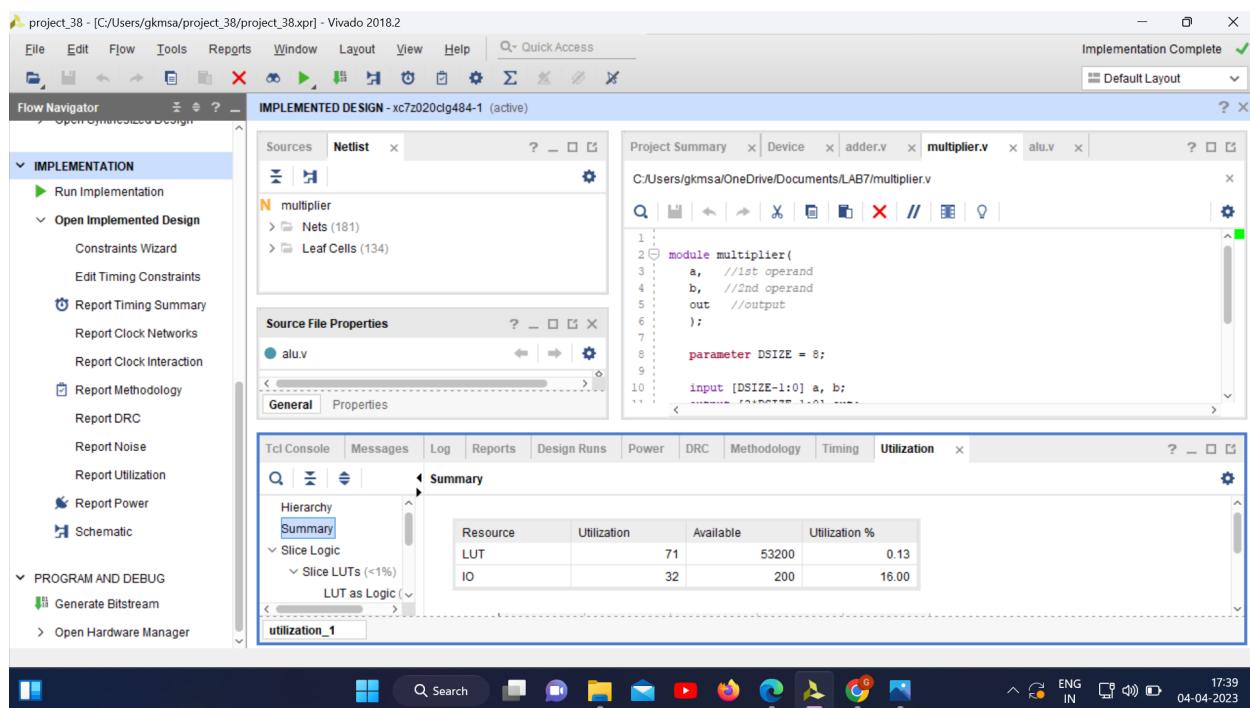
BIT-WIDTH v/s DELAY



## multiplier ( DSIZE = 8 )



## Report Utilization



## Report Timing Summary

The screenshot shows the Vivado 2018.2 interface with the project "project\_38" open. The left sidebar is expanded to show the "IMPLEMENTATION" section, which includes options like "Run Implementation", "Open Implemented Design", "Report Timing Summary", and "Report Power". The main workspace displays the "IMPLEMENTED DESIGN - xc7z020clg484-1 (active)" window. In the center, there is a code editor showing the Verilog file "multiplier.v" with the following code:

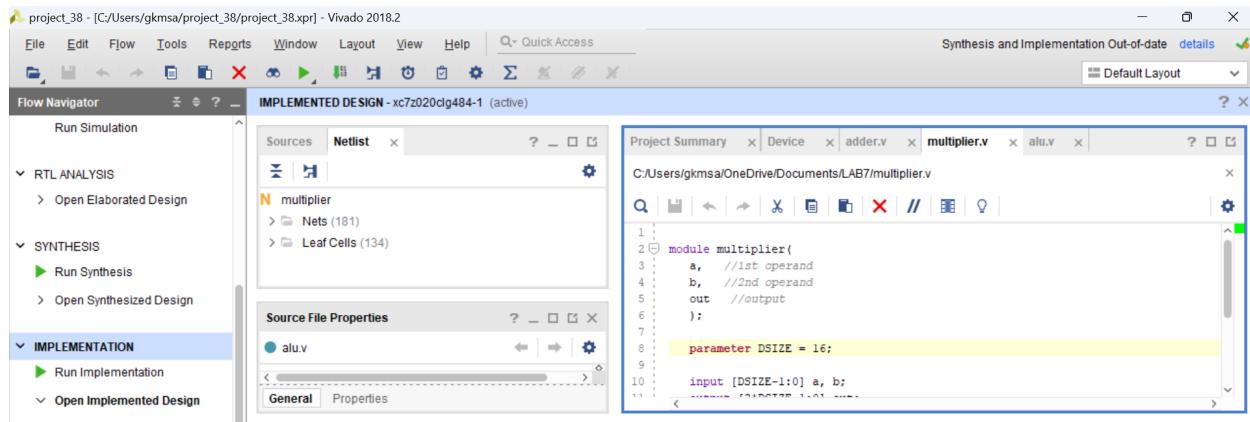
```
9
10    input [DSIZE-1:0] a, b;
11    output [2*DSIZE-1:0] out;
12
13    assign out = a*b;
14
15 endmodule
```

Below the code editor is a "Timing" report table titled "Unconstrained Paths - NONE - NONE - Setup". The table lists four paths with their respective parameters:

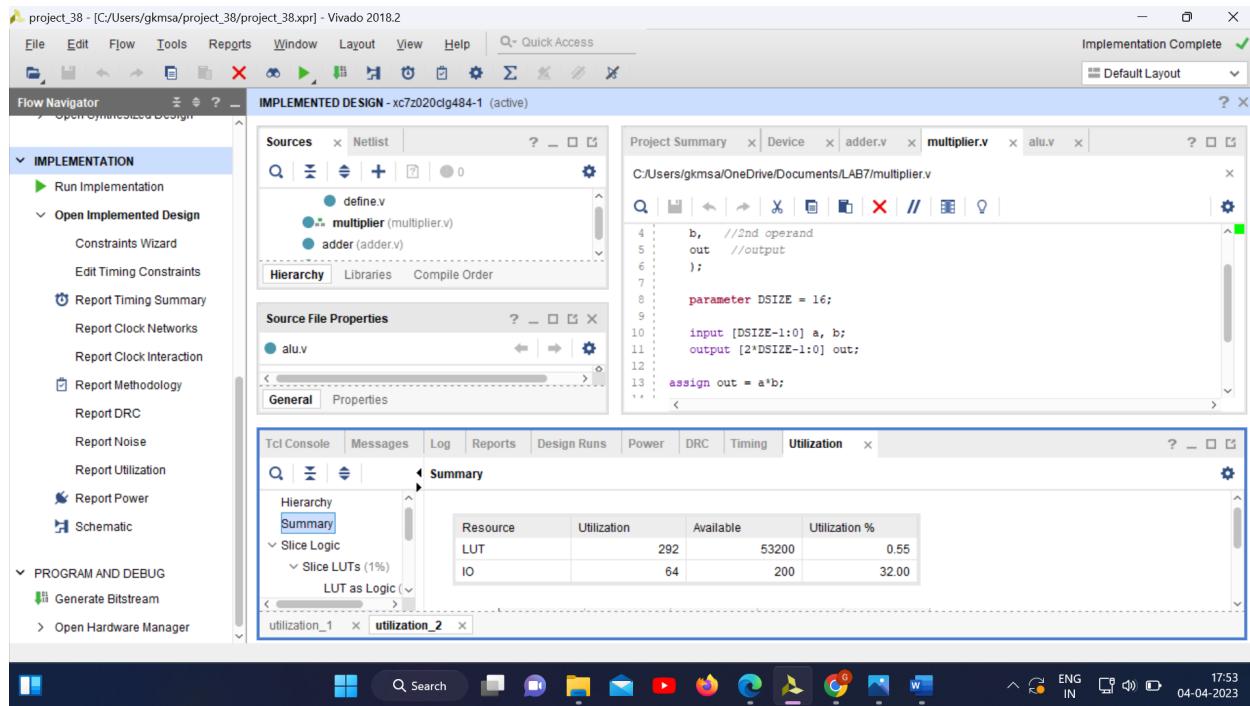
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	∞	10	8	16	b[2]	out[15]	13.676	6.072	7.603	∞
Path 2	∞	9	7	16	b[2]	out[14]	13.437	5.987	7.450	∞
Path 3	∞	9	7	16	b[2]	out[13]	13.359	5.911	7.448	∞
Path 4	∞	9	7	16	b[2]	out[12]	13.309	5.980	7.329	∞

At the bottom of the timing report, there are two sections: "Setup (10)" and "Hold (10)".

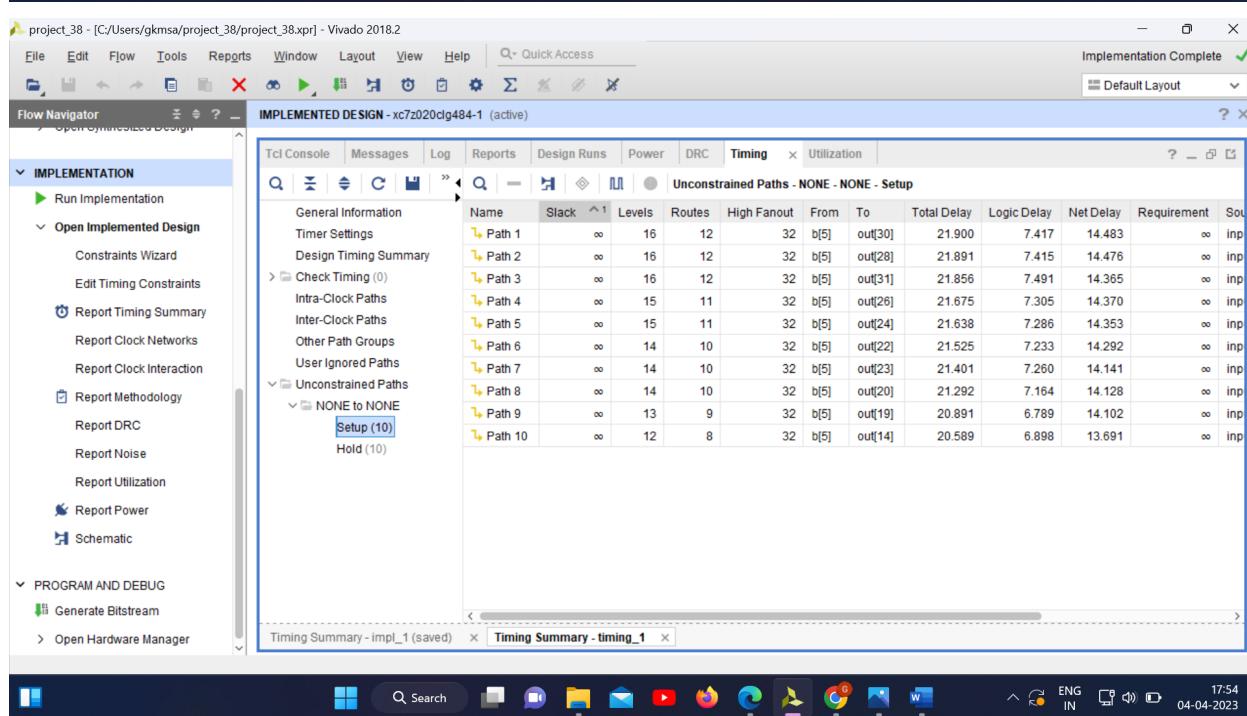
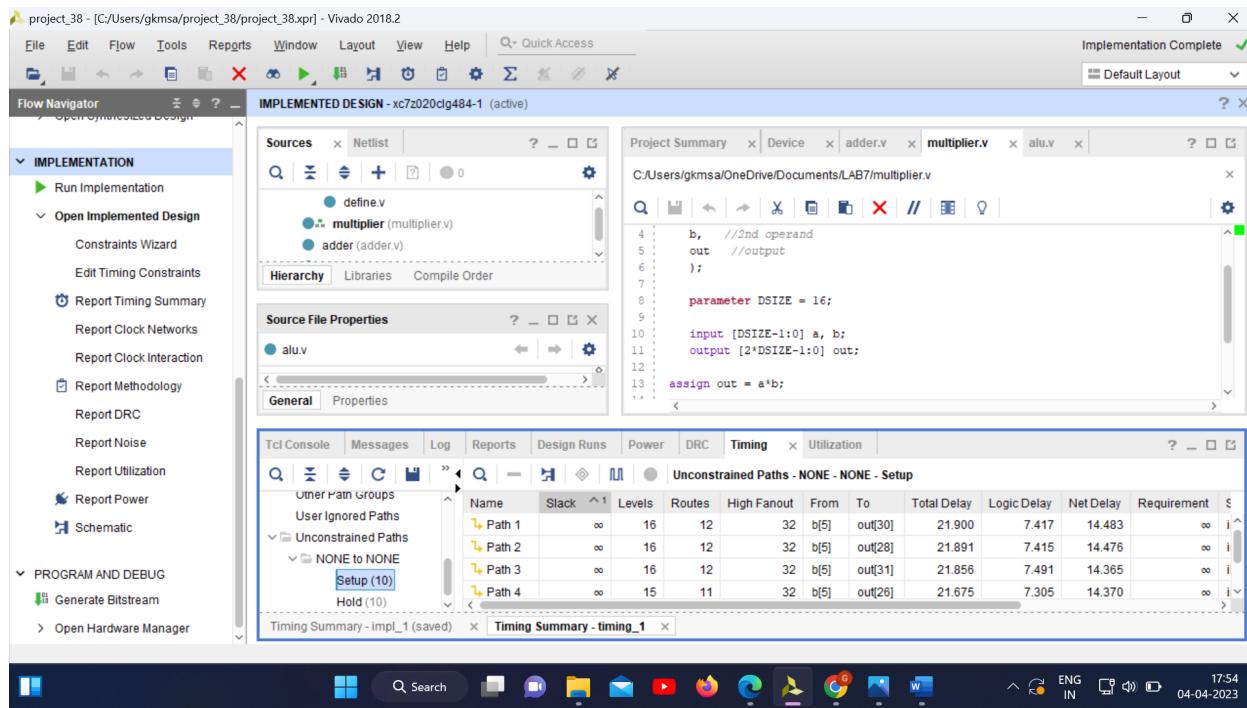
# multiplier ( DSIZE = 16 )



## Report Utilization

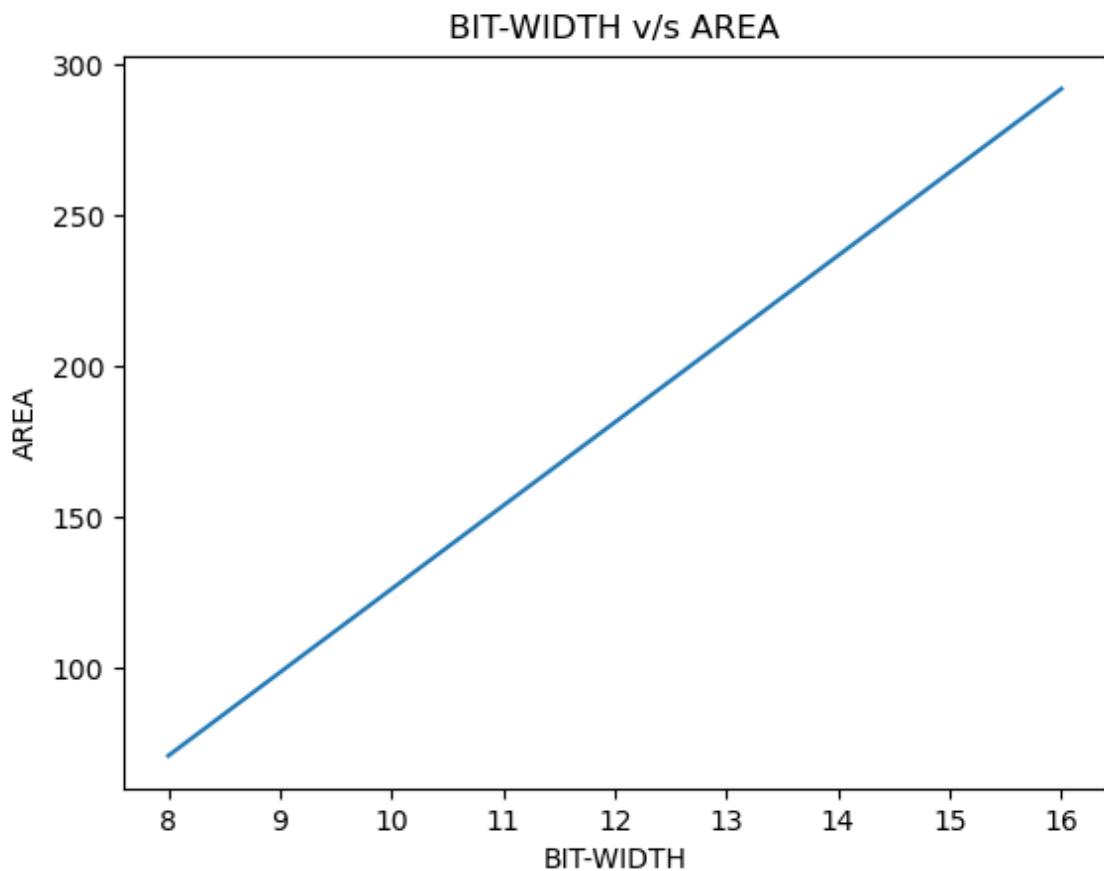


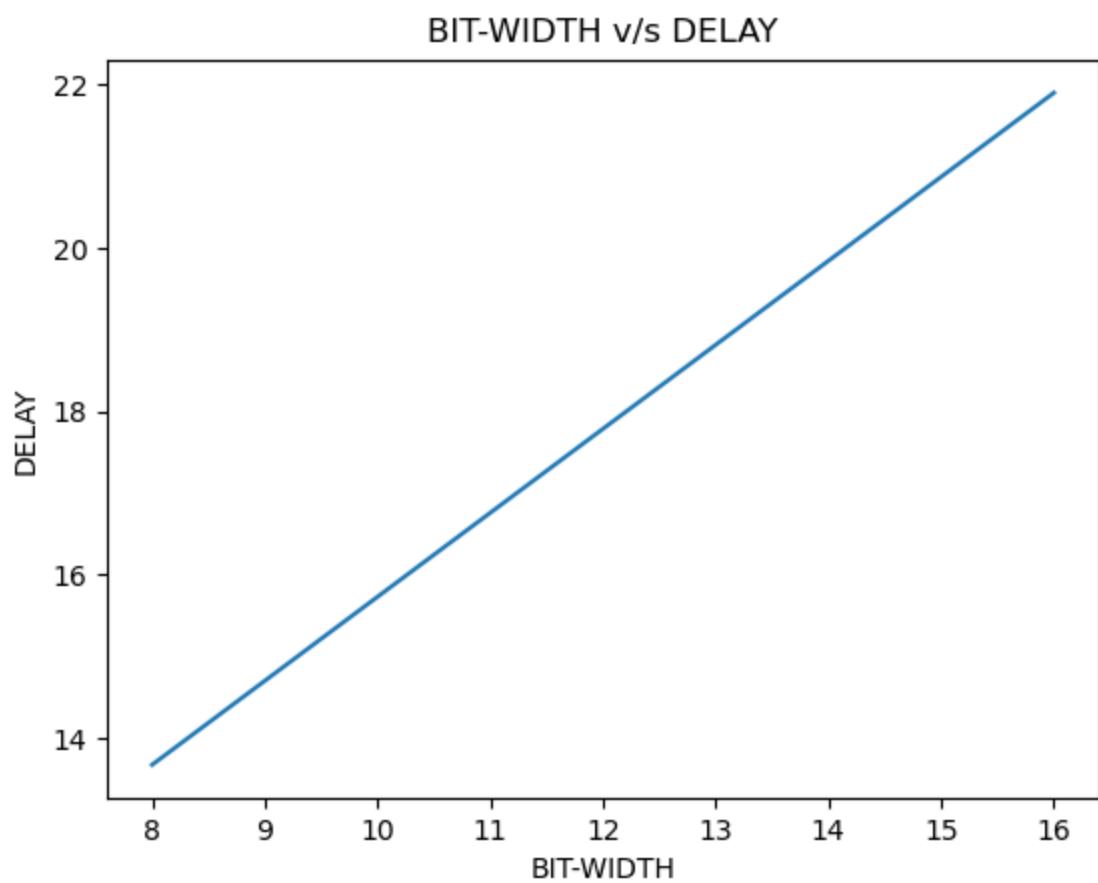
# Report Timing Summary



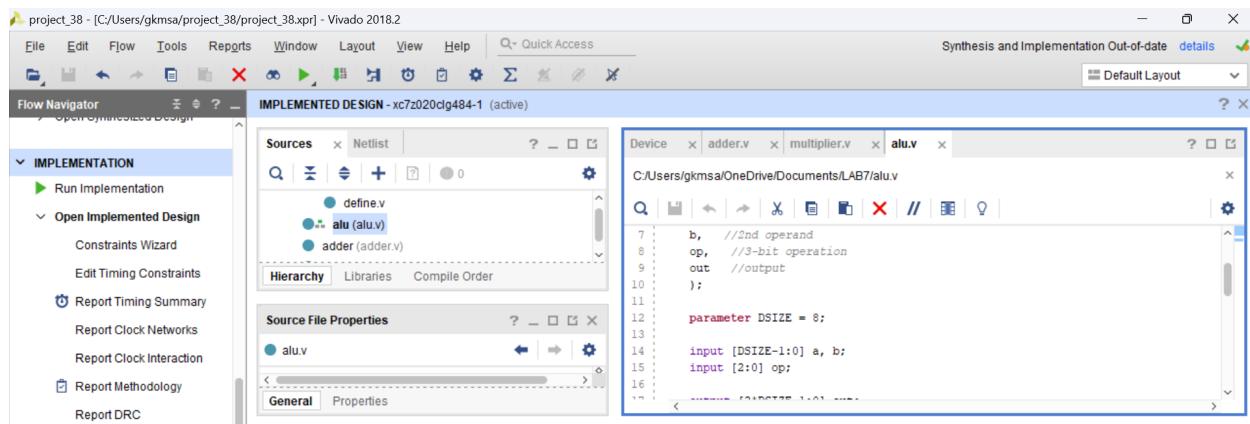
## Multiplier - Graph

DSIZE	BIT-WIDTH	No of slices	Delay in ns
8	8	<u>71</u>	<u>13.676</u>
16	16	<u>292</u>	<u>21.900</u>

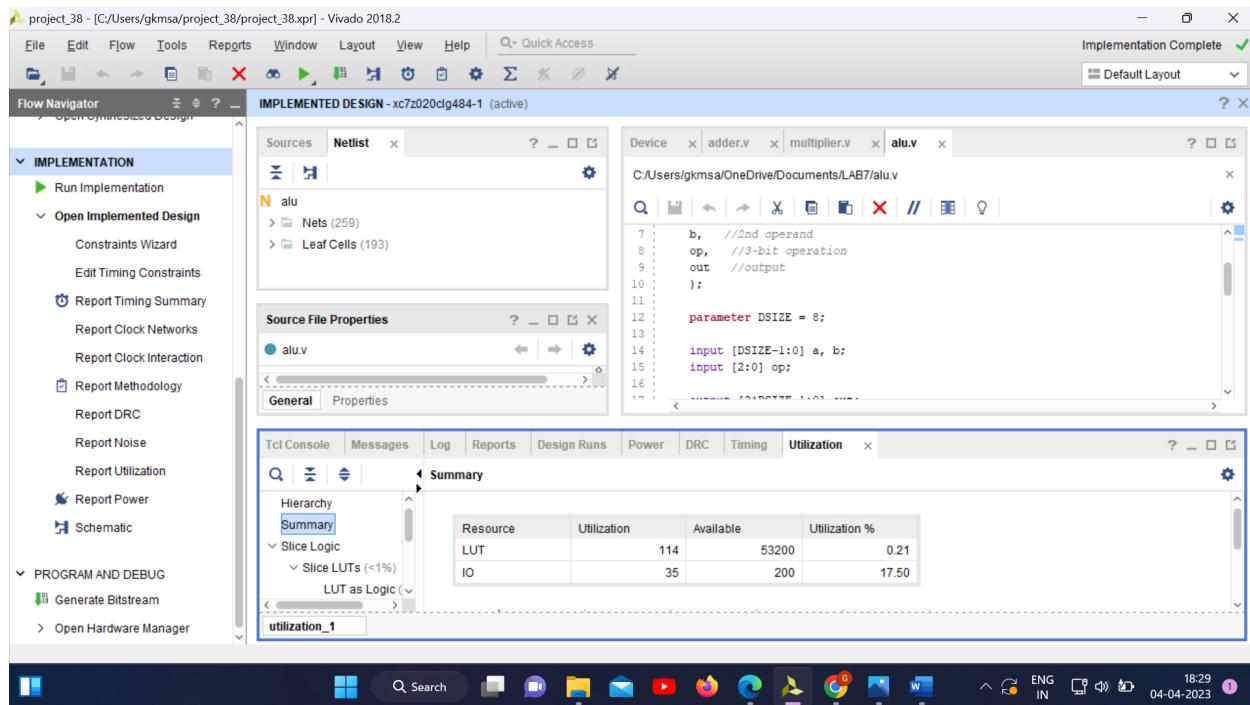




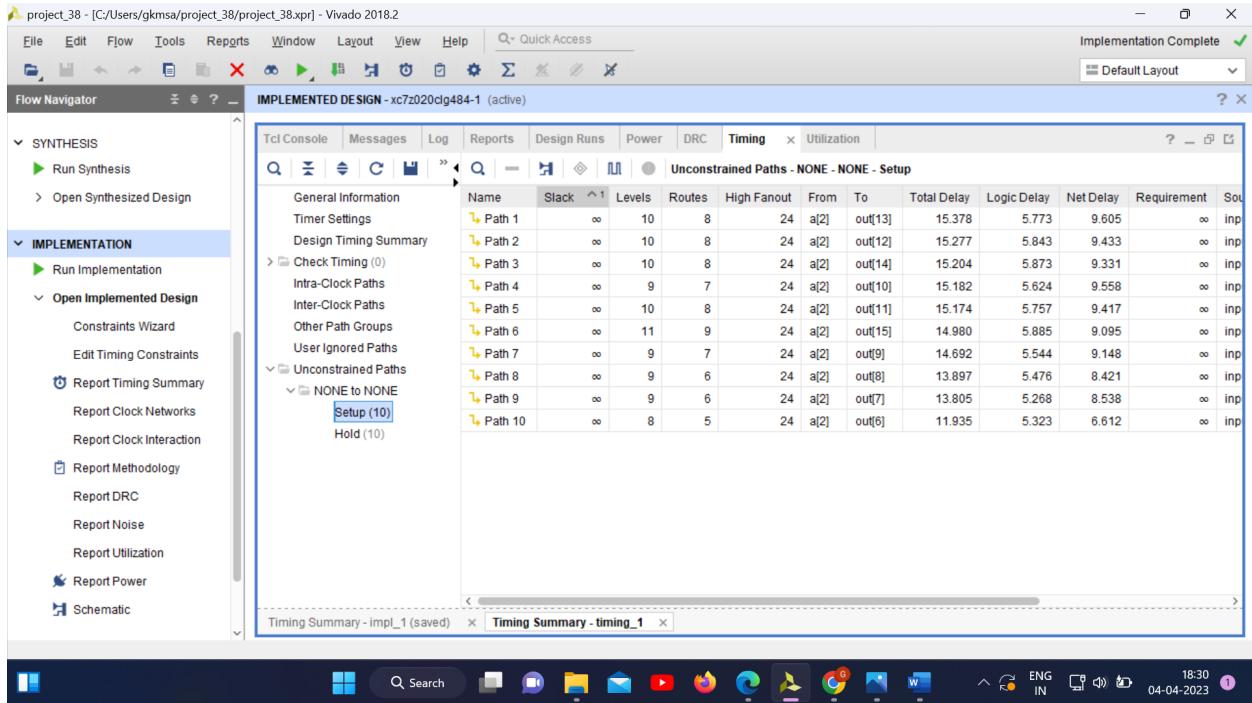
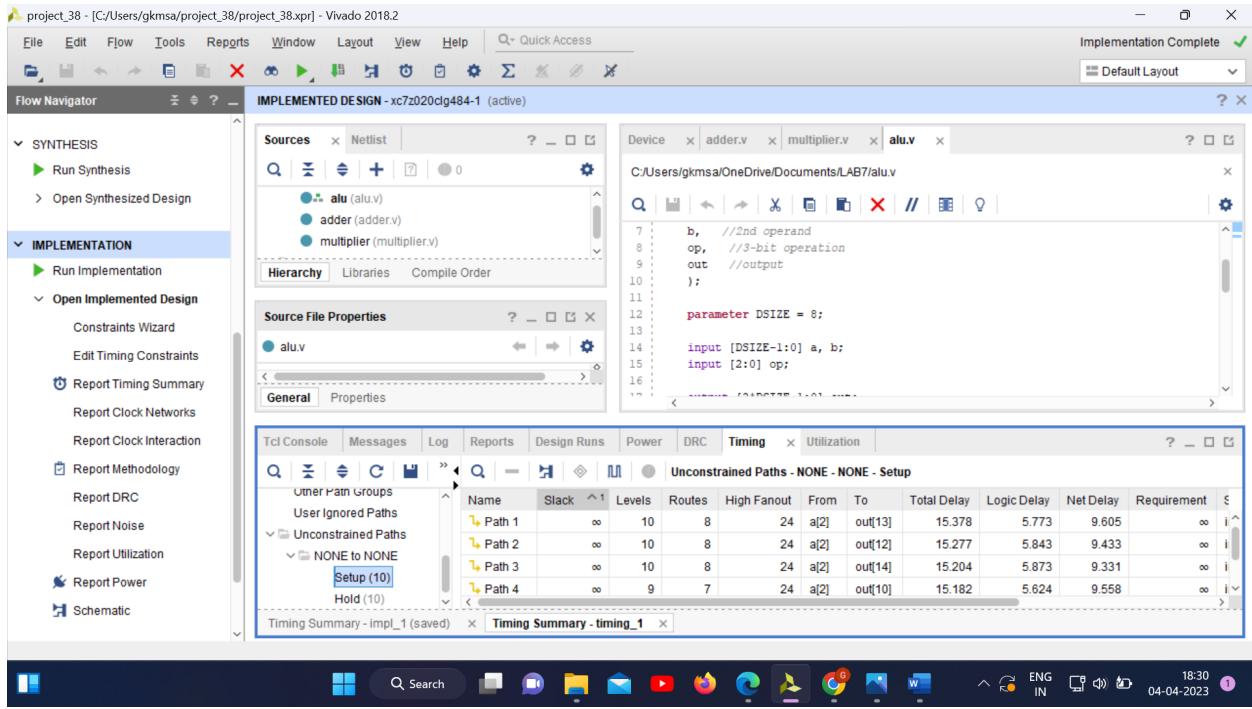
## alu ( DSIZE = 8 )



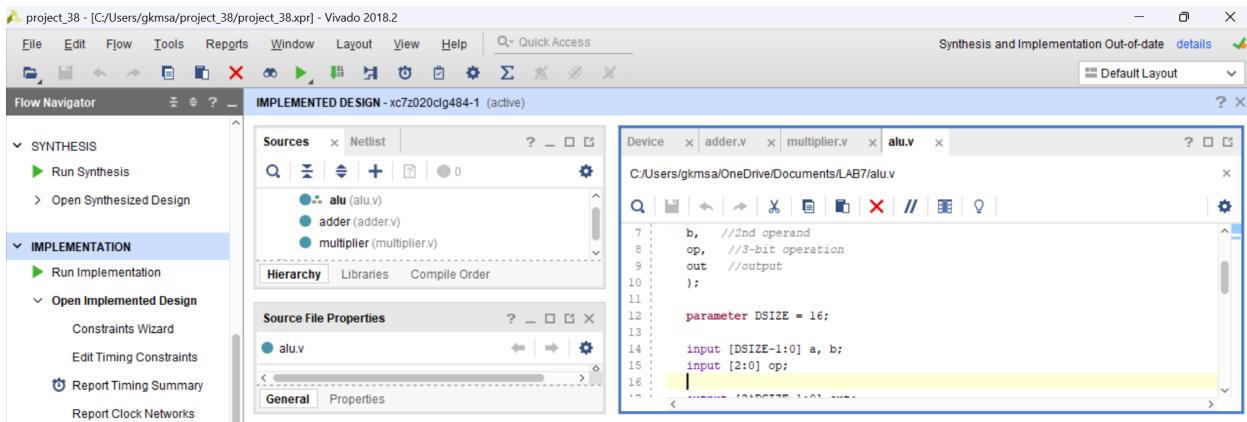
## Report Utilization



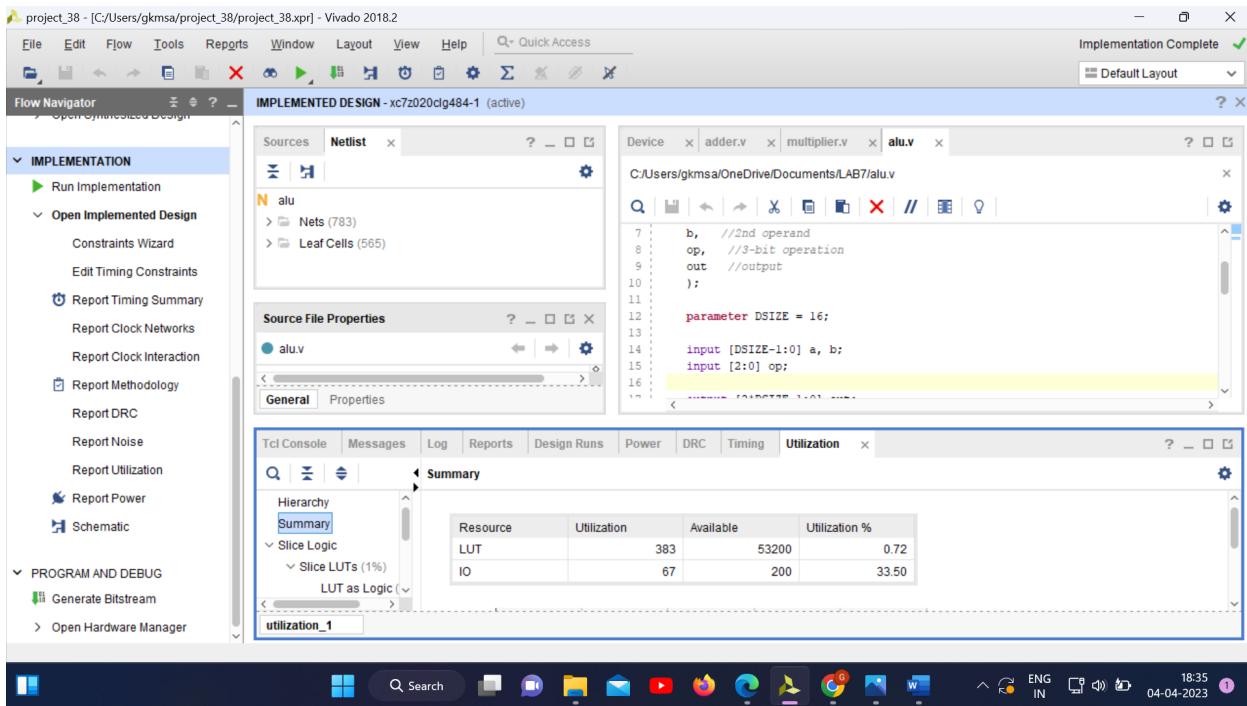
# Report Timing Summary



## alu ( DSIZE = 16 )



## Report Utilization



## Report Timing Summary

Screenshot of Vivado 2018.2 showing the Report Timing Summary feature.

The screenshot displays two windows of the Vivado interface. Both windows show an "IMPLEMENTED DESIGN - xc7z020clg484-1 (active)" project. The top window shows the "Timing" tab selected in the "Reports" tab bar, displaying the "Unconstrained Paths - NONE - NONE - Setup" report. The bottom window also shows the "Timing" tab selected, displaying the same report.

**Top Window (Vivado 2018.2):**

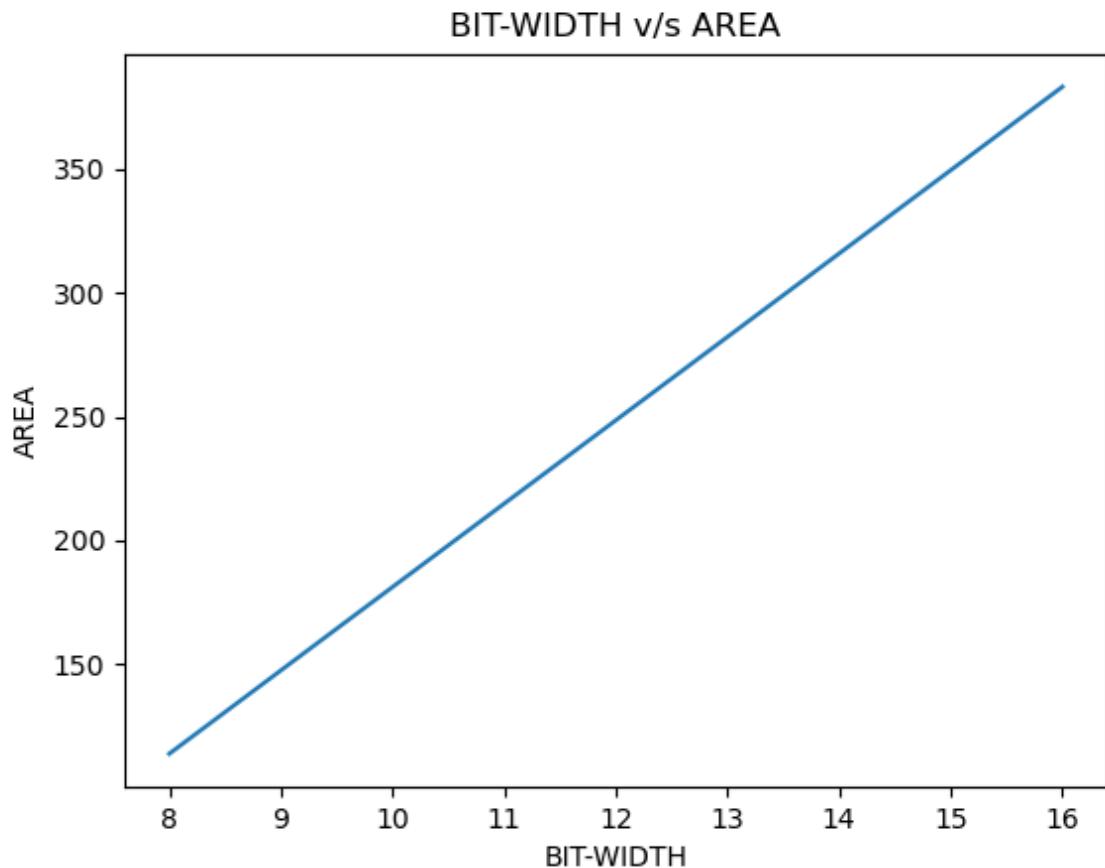
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source
Path 1	$\infty$	15	11	38	a[12]	out[31]	22.047	7.322	14.725	$\infty$	inp
Path 2	$\infty$	15	11	38	a[12]	out[28]	22.033	7.235	14.797	$\infty$	inp
Path 3	$\infty$	15	11	38	a[12]	out[27]	21.664	7.129	14.535	$\infty$	inp
Path 4	$\infty$	15	11	38	a[12]	out[24]	21.651	7.019	14.632	$\infty$	inp
Path 5	$\infty$	15	11	38	a[12]	out[30]	21.451	7.244	14.207	$\infty$	inp
Path 6	$\infty$	14	10	38	a[12]	out[23]	21.425	6.774	14.651	$\infty$	inp
Path 7	$\infty$	15	11	38	a[12]	out[29]	21.418	7.344	14.074	$\infty$	inp
Path 8	$\infty$	15	11	38	a[12]	out[25]	21.124	7.130	13.994	$\infty$	inp
Path 9	$\infty$	15	11	38	a[12]	out[26]	21.052	7.044	14.008	$\infty$	inp
Path 10	$\infty$	14	10	44	a[3]	out[17]	20.790	6.882	13.907	$\infty$	inp

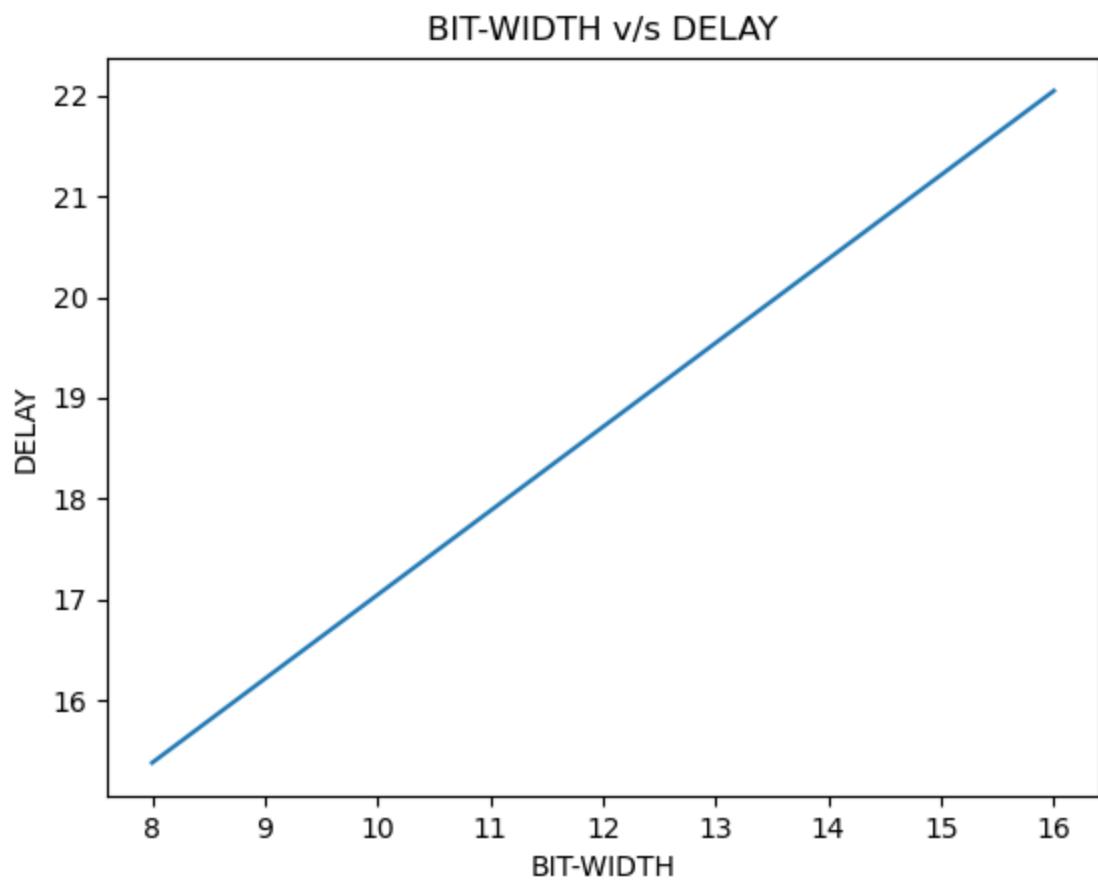
**Bottom Window (Vivado 2018.2):**

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source
Path 1	$\infty$	15	11	38	a[12]	out[31]	22.047	7.322	14.725	$\infty$	inp
Path 2	$\infty$	15	11	38	a[12]	out[28]	22.033	7.235	14.797	$\infty$	inp
Path 3	$\infty$	15	11	38	a[12]	out[27]	21.664	7.129	14.535	$\infty$	inp
Path 4	$\infty$	15	11	38	a[12]	out[24]	21.651	7.019	14.632	$\infty$	inp
Path 5	$\infty$	15	11	38	a[12]	out[30]	21.451	7.244	14.207	$\infty$	inp
Path 6	$\infty$	14	10	38	a[12]	out[23]	21.425	6.774	14.651	$\infty$	inp
Path 7	$\infty$	15	11	38	a[12]	out[29]	21.418	7.344	14.074	$\infty$	inp
Path 8	$\infty$	15	11	38	a[12]	out[25]	21.124	7.130	13.994	$\infty$	inp
Path 9	$\infty$	15	11	38	a[12]	out[26]	21.052	7.044	14.008	$\infty$	inp
Path 10	$\infty$	14	10	44	a[3]	out[17]	20.790	6.882	13.907	$\infty$	inp

## alu

DSIZE	BIT-WIDTH	No of slices	Delay in ns
8	8	<u>114</u>	<u>15.378</u>
16	16	<u>383</u>	<u>22.047</u>





**Thank You**