**MODELING AND DESIGN OF MEMRISTOR & DGFET AS LIF (LEAKY INTEGRATE AND FIRE) NEURON USiNG SENTAURUS TCAD**

**EED498**

**(Spring 2021)**

END TERM REPORT

*Project report submitted in partial fulfillment of the requirement for the degree of*

Bachelor of Technology

In

Electronics and Communication Engineering

**Submitted by**

Datla Gautam Varma (171011099)

Vidhip Vutsela (1710110)

Under supervision of

Prof Amitabh Chatterjee

Electrical Engineering

**Department of Electrical Engineering**

**School of Engineering**

SNU

**Abstract:**

Memristor is one of the four fundamental passive electrical components with

the others being resistor, capacitor, and inductor. It is a non-linear two-terminal electrical component which relates electric charge and magnetic flux linkage. It not only acts as a resistor i.e., regulates the flow of electrical current in a circuit but also acts as a non-volatile electronic device meaning that these devices would retain the memory even without power. Since the first fabrication in 2008, it has been extensively studied for wide electronic applications, so in this project what we would primarily like to do is to design a memristor. Using a device simulator “Sentaurus” and UNIX commands, we will be first building a Memristor model and then perform a detailed analysis on this first devised model. Then we will be trying to optimize the hysteresis loop and design a better memristor model.

Now the question we tend to face is if we have a better device than memristor having, not only better reliability but also has a better calibrated and controlled CMOS process. The answer is Yes, we can implement the LIF (Leaky Integrate and fire) neuron model using DGFET. Double Gate Junction less field effect transistor (DGFET) is one of the most promising technologies for sub-40 nm design of transistors, not only the absence of metallurgical junctions in DG-JLFET eases the fabrication complexity, it also cuts down the thermal budget requirement. Various attempts have been made to exploit this newly emerging technology in electronic circuits. So, in this project we will be primarily dealing with DGFET and its implementation as a LIF neuron.

Candidate Declaration

I hereby declare that the thesis entitled “Vidhip Vustela” and “Datla Gautam Varma” submitted for the B Tech Degree program. This thesis has written in my own words. I have adequately cited and referenced the original sources.

Datla Gautam Varma (1710110099)

Date:21-2-2021

Vidhip Vustela (1710110)

Date: 21-02-2021

**TABLE OF CONTENTS**

**List of figures**.........................................................................................................................5

**List of tables**...........................................................................................................................6

1. **Introduction..........................................................................................................................7**

a) Motivation.................................................................................................................7

b) Problem Statement.....................................................................................................7

**2.**  **Literature Review............................................................................................................8**

a) Introduction to Memristor..........................................................................................8

i) Types of memristor...............................................................................................9

ii) Ti02 memristor....................................................................................................10

iii) Linear Drift mathematical model........................................................................11

b) Sentaurus Device Editor...........................................................................................12

i) Introduction the Sentaurus Device Editor...........................................................12

ii) Graphic User Interface of SDE..........................................................................13

iii) Working with structures in SDE........................................................................14

iv) Working with structures in SDE.........................................................................15

c) Electrical switching of chalcogenide-based variable resistance devices.................16

d) Spiking Neural Network (SNN) and Leaky Integrate-and-fire (LIF) model...........17

i) Spiking neural network........................................................................................17

ii) LIF model............................................................................................................18

iii) DGFET................................................................................................................18

iv) DGFET LIF neuron.............................................................................................19

e) Sentaurus TCAD Tools............................................................................................20

i) Sdevice..................................................................................................................23

ii) Sentaurus Workbench...........................................................................................23

iii) Sentaurus Visual...................................................................................................24

**3. Work Done...................................................................................................................25**

i) Introduction to the device (Silver chalcogenide memristor) ..................................25

ii) Building the required 2D/3D memristor models in SDE........................................26

iii) Contacts and mesh generation …............................................................................28

iv) Shift from memristor to DGFET..............................................................................30

**4**.  **Results.........................................................................................................................30**

**5. Conclusions.................................................................................................................39**

**6. References...................................................................................................................40**

**LIST OF FIGURES**

2.1 Conceptual symmetries of resistor, capacitor, inductor, and memristor

2.2 Classification and different types of memristor

2.3 Titanium dioxide memristor

2.4 Working of the titanium dioxide memristor

2.5 Modelling memristor as On and Off Resistance

2.6 Graphic user interface of Sentaurus structure editor

2.7 Working of chalcogenide-based ion-conducting variable resistance devices

2.8 Working of SNN

2.9 LIF neuron circuit model

2.10 DGFET structure

2.11 Electrostatic potential variation and output characteristics of DGFET

2.12 (i)Equilibrium band diagram (ii) Electron hole pair production as a result of ionization (iii) Barrier lowering as a result of hole accumulation iv) When the threshold is crossed (“fire event”), the VDG is removed, allowing the holes to escape through both junctions and restoring the barrier to its original location (“reset”).

2.13 DG-JFET LIF neuron circuit

2.14 Sentaurus workbench window

2.15 Sentaurus visual window

3.16 Structure of EMB memristor

3.17 Biasing of EMB memristor

3.18 2D structure of memristor in SDE

3.19 3D structure of memristor in SDE

3.21 Memristor with Anode contact

3.22 Memristor with cathode contact

3.23 Meshing done on the 3D memristor structure

4.24 DGFET structure in sentaurus device editor with contacts

4.25 Meshing of DGFET

4.26 Meshed structure of DGFET from .tdr file in Svisual

4.27 Simulation command file code snippet

4.28 I-V characteristics of DGFET (not scaled using parameters)

4.29 Meshed structure of properly scaled DGFET structure

4.30 Output characteristics of DGFET

4.31 Current vs time and Voltage vs time for DGFET with Vg=1volt

4.32 Drain current (Id) vs Gate Voltage (Vg) graph (Vd=1.5V)

4.33 Drain current (Id) vs Gate Voltage (Vg) graph (Vd=1V)

4.34 Leakage current (Source) vs time

4.35 Hole current vs time

4.36 Drain Current Vs Time

4.37 Input voltage vs time

4.38 Drain current vs Time for Triangular waveform as input

**LIST OF TABLES**

3.1 Materials and the corresponding color scheme of different layers of memristor in SDE

**1) Introduction**

Since the invention of transistors in 1948 by bell laboratories, the fabrication industries have started churning out billions of transistors, with this growth drastically improving from one year to another. Now in such a situation the question that we tend to face is whether in such a thriving semiconductor unit monoculture, will a brand-new circuit component notice an area to require root and grow? This is where memristor comes into limelight, a device which was first theoretically discussed in 1971 by Leon Chua but finally implemented in hardware in 2008 by the HP laboratories. Though such a device would not totally replace transistors it would supplement them in the logical and memory circuits in addition to which it might also bring out some form of analog information processing back into our digital world of computing technologies. But the modelling of memristor is a very difficult process using sentaurus TCAD mainly because of the fact the mobility models we plug-in our TCAD simulations have not been well defined yet which directly states the fact that we cannot optimize the memristor device properly. So, as an alternative to memristor we look for a device with similar behavior having better reliability, more controlled and CMOS process, having well defined ionic conduction simulation models for devices and can be used in modelling a neuron using existing models. DGFET is one such device. So, in this project we will be mainly dealing with a highly scalable and CMOS compatible double-gate junction less field-effect transistor (DG-JLFET)-based leaky integrate-and-fire (LIF) neuron

**A) Motivation**

Modern devices such as our computers and smartphones have improved in their cost speed and power by scaling down device size. But the manufacturing costs and physical limits of fabrication impede the sustainable growth and the traditional von Neumann computer architecture cannot satisfy people's unlimited demand on high performance computation. Consequently, neuromorphic systems which mimic our nervous system have recently drawn people’s attention to overcome these technical and economic limitations. Realizing such a network results in high design complexity and cost as it requires humongous memory and also should be adaptive to the environment. The first step toward realizing such a neuromorphic system is to develop an artificial synapse capable of emulating synapse functionality, such as analog modulation, with very low power consumption in addition to robust controllability. Among the plethora of available devices, the recently rediscovered memristor device has been proved to be the ideal candidate mainly attributed to its ability of analog switching, low power consumption, high speed and artificial synapses i.e. its unique property to record the historical profile of the excitations on the device. But due to certain limitations in modelling and simulation of memristor was not feasible. . To achieve a large-scale network akin to biology, a power and area efficient electronic neuron is essential. Now looking at a few other alternatives we find that DGFET (Double Gate JunctionLess Field Effect Transistor) should be the device of our choice mainly because of better reliability, well controlled and calibrated CMOS process and availability of well-defined models which we can plug-in to our simulations.

**B) Problem Statement**

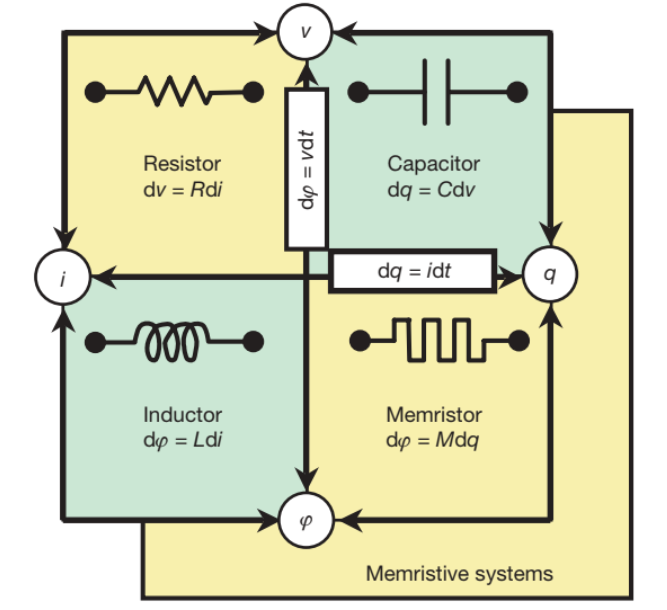
Now, as already said, spiking neural networks (SNNs) have gotten a lot of recognition in the last few years for next-generation computing because of their potential to achieve low power and concurrent computing in addition to von Neumann-based processors. The SNN is a third-generation artificial neural network (ANN) that resembles biological neurons very closely. The leaky-integrate-and-fire neuron model is one such example (LIF). For the hardware realization of the LIF neuron model, CMOS-based analog circuits, digital circuits and non-Si-based systems have all been extensively studied. But most of the circuits have higher power consumption, more area and circuit complexity. So, in order to overcome such shortcomings and still implement the LIF neuron model we use DGFET.

Furthermore, while researchers have looked into FETs without metallurgical junctions for digital, analog, and memory applications, there have been no studies that have looked into FETs without metallurgical junctions for LIF neuron applications. So, in this article, an analog implementation of a LIF neuron using highly scalable and CMOS compatible double-gate JLFET (DG-JLFET) is investigated via well-calibrated TCAD simulations.

**2.Literature Review**

**A) Introduction to memristor:**

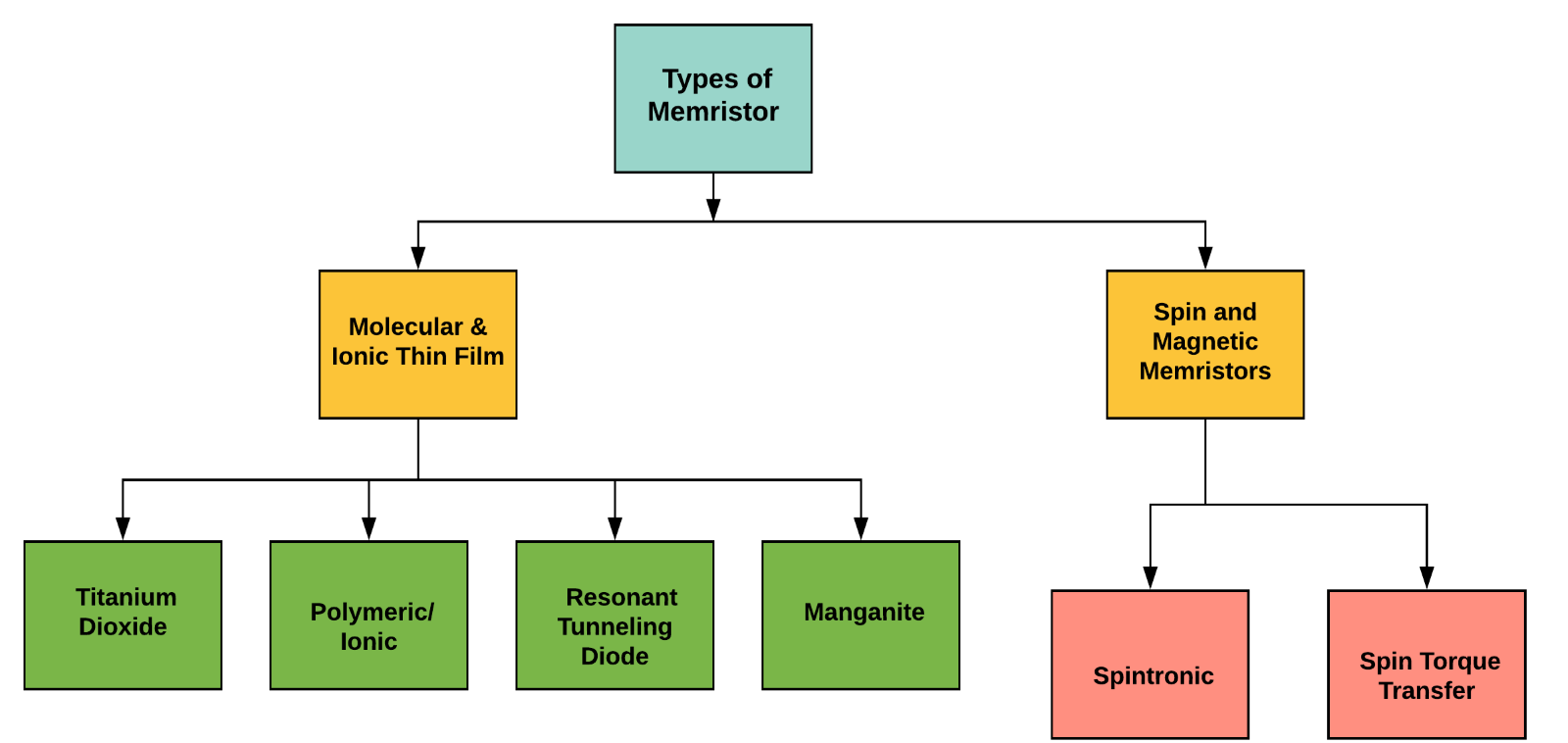
Anyone in the field of electronics would be familiar with the three passive and fundamental circuit elements namely capacitor, inductor and resistor. However, in 1971 Leon Chua noted that there are six different mathematical relations connecting pairs of the four-fundamental circuit variables: electric current i, voltage v, charge q and magnetic flux Q. One of these relations (the charge is the time integral of the current) is determined from the definitions of two of the variables, and another (the flux is the time integral of the electromotive force, or voltage) is determined from Faraday’s law of induction. Thus, he concluded that there should be four basic circuit elements described by the remaining relations between the variables. From this symmetry he put forth a fourth fundamental circuit element, memristor (memory resistor) by linking magnetic flux and charge. However, since then, the definition of memristor has been broadened to include any form of non-volatile memory that is based on resistance switching, which increases the flow of current in one direction and decreases the flow of current in the opposite direction.



**Fig1. Conceptual symmetries of resistor, capacitor, inductor, and memristor**

Now looking at the relationship d(phi) =(M)dQ , if we treat M as a constant, memresistance is identical to resistance. However, if M is itself a function of q, yielding a nonlinear circuit element, then the situation is more interesting as the i–v characteristic of such a nonlinear relation between q and Q for a sinusoidal input is a frequency-dependent Lissajous figure.

**i) Types of memristor:**

**Fig2. Classification and different types of memristor**

**1. Molecular and Ionic Thin Film Memristive Systems**

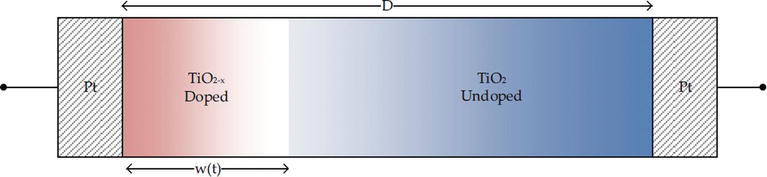
These types of memristors primarily rely on different material properties of thin film atomic lattices that exhibit hysteresis under the application of charge.

**2. Spin Based and Magnetic memristive systems**

Spin-based memristive systems, as opposed to molecular and ionic nanostructure-based systems, rely on the property of degree of freedom in electron spin. In these types of system, electron spin polarization is altered, usually through the movement of a magnetic “domain” wall separating polarities.

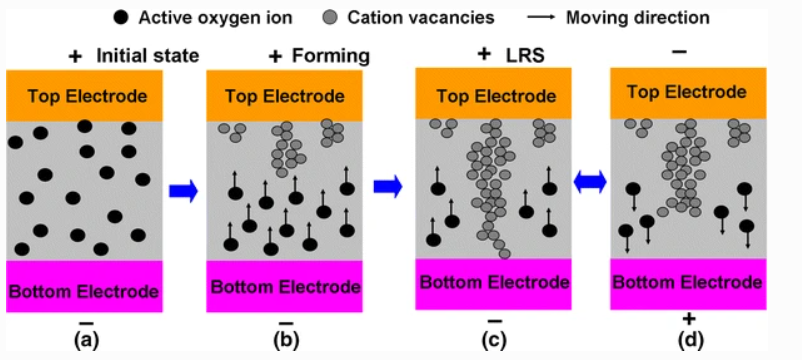
**ii) TIo2 Memristor model**

Memristor-based applications require a suitable model for analysis and simulation of the system. The HP memristor model where the memristor mechanism based on the drift of oxygen vacancies is widely used. The memristor model developed by HP Lab has Pt/TiO2/Pt structure.



**Fig3. Titanium Dioxide Memristor**

Here the TiO2 layer which is doped with positive charged-rich oxygen vacancies (TiO2−x) exhibits a low resistance behavior, while the undoped part exhibits a high resistance behavior. As a result of the appropriate excitation on this structure, the ionic drift between the doped part and the undoped part results in a dynamic change in the width of the doped region. That is, the width of the doped region is taken as a state variable. As the width of the doped region approaches zero (w→0), the memristor goes to a high resistance state (HRS), and as the width of the doped region approaches D (w→D), the memristor goes to a low resistance state (LRS).

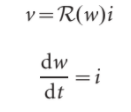


**Fig4. Looking into the working of TiO2 memristor**

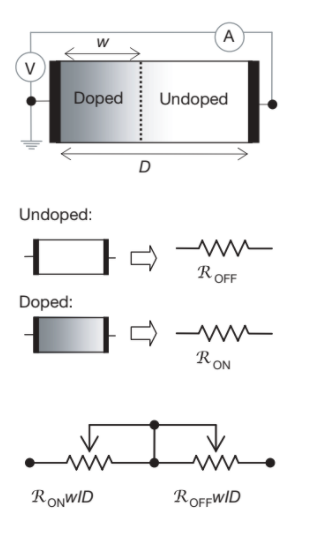
Taking a look into what happens inside the memristor we can say that in the initial state we have randomly distributed mobile oxygen ions. When a voltage bias is applied the nucleation and subsequent growth from anode to cathode of CFs (Conductive films) composed of cation vacancies happens. When the positive bias is applied to positive charged oxygen vacancies, The LRS with a full CF whose thinnest region is near the cathode is formed. If the exact opposite voltage bias is applied, The HRS is formed with a partially ruptured conducive filament at its thinnest region.

**iii) Mathematical model (Linear Drift Model)**

Looking at the mathematical model we can start analyzing the working of memristor. The most basic mathematical definition of a memristor device for circuit analysis can be put forth in the differential form as follows,



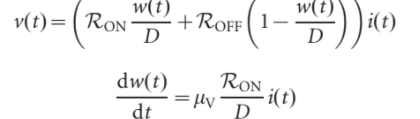
Here, w is the state variable of the device and R is a generalized resistance that depends upon the internal state of the device.



**Fig5. Modelling memristor as Ron and Roff**

To explain in the simplest possible way let us consider a thin semiconductor film of thickness D sandwiched between two metal contacts. The total resistance of the device is determined by two variable resistors connected in series, where the resistances are given for the full-length D of the device. Specifically, the semiconductor film has a region with a high concentration of dopants having low resistance RON, and the remainder has a low dopant concentration and much higher resistance ROFF.

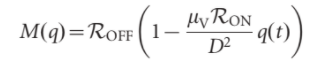
Now with the application of an external bias v(t) across the device will move the boundary between the two regions by causing the charged dopants to drift. For the simplest case of ohmic electronic conduction and linear ionic drift in a uniform field with average ion mobility, we get

.

Solving which we get w(t) as,



Substitution this w(t) in v(t) and assuming Ron <<<< Roff,



So, in a way we can say that the relationship between current, voltage, charge, and flux for the memristor is given by:

v(t) = M(q(t))i(t)

M(q) = dφ(q) / dq

i(t) = W(φ(t)) v(t)

W(φ) = dq(φ)/dφ

show us that the memristance value is related to the history of the current passing through the memristor. That is, when the current passing through the memristor is cut off, it remains at the value of the memristance value. The memristance value starts to change from the last value when it provides the current again to memristor. In other words, the memristor has a **nonvolatile memory effect**. On the other hand, memristor is not an element that stores energy

**b) Sentaurus Device Editor:**

SDE uses a 2D/3D structure editor and 3D process emulator to create TCAD devices. Structures are generated or edited interactively using GUI (Graphic user interface). Alternatively, devices can be generated in batch mode using scripts (this is useful for creating parameterized structure devices).

The 2D and 3D device editor modules provide GUI and scripting to support:

i) Generate model geometry

ii)Define contact regions

iii)Add constant, analytic and externally generated doping profiles to model

Also, SDE uses a default geometric coordinate system. T has no default units or assumptions for automatic geometric scaling. Users must select modelling units and enter all the necessary geometric dimensions expressed in selected units.

**ii) GUI (Graphic User Interface) of SDE**

The graphical user interface is a form of user interface that allows users to interact with electronic devices through graphical icons and audio indicators such as primary notation, instead of text-based user interfaces. Talking of the various options available with us in the GUI of SDE we have various options such as,

**a) Rendering mode toolbar buttons (for 3D)**

Here we have various options such as facets, wireframe, Hidden lines, etc.

**b) Standard views toolbar buttons**

Here we can change the perspective from which we see in the view window. We have options such as Isometric view, XY view, YZ view, XZ view.

**c) GUI actions toolbar buttons (zoom and move)**

Used to move and zoom the created structure, we have options such as select, zoom to window, etc.

**d) GUI actions toolbar buttons (2D edit tools)**

Here we can edit the 2d structure we have created in the view window such as adding a vertex moving a vertex, moving the edge, etc.

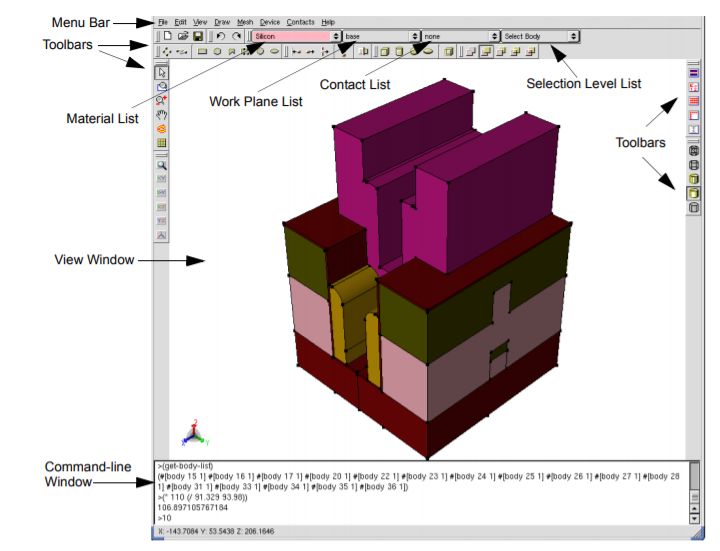
**e) GUI actions toolbar buttons (2D create tools)**

Here we can find various objects used to create 2d structures. For example, we can choose to create an Elliptical region, Circular region, Rectangle, etc.

**f) GUI actions toolbar buttons (3D create tools)**

Various tools used to create 3D objects can be found here. Example:

Create cuboid, sphere, etc.



**Fig6. GUI of Sentaurus Device Editor**

Also, as we can see in the picture above, the main window of Sentaurus Structure Editor contains four lists (combo boxes):

**Material list –** Select the material which we would like to be assigned to new objects.

**Work Plane list –** Used to set the work plane for 3D editing.

**Contact list –** Used to select the contact's name to be that we want to use in the next set contact region, or face, or edge operations.

**Selection Level list –** Selects which types of objects can be selected.

**iv) Working with structure in Sentaurus TCAD:**

Whenever one is working with the 2D/3D generation of structure in sentaurus SDE, one must follow these steps:

1) Create “top level” entities first (Ex: Rectangle, sphere, polygon, etc.)

2) Next one should modify using operations such as chambering and filleting.

3) Now if we are dealing with two-dimensional models I.e., 2D is “top level “model operations such as “Extrusion “and “Sweep” must be used to generate 3D models.

4) Next, we must apply local operations and Boolean expressions if necessary.

5) Finally, we should assign material properties, region names and contacts.

Also, whenever we are working with structures, it is always beneficial if we are familiar with various other options such as adding removing vertices, moving edges, moving vertices, automatic region naming, overlap behavior and few others.

C) **Electrical switching of chalcogenide-based ion-conducting variable resistance devices:**

Ion-conducting devices are made up of an amorphous medium and which serves as an insulator and also has a storage medium for metal ions along with a source for metal ions. The source of metal ions is an electrochemically active material that is enclosed next to the amorphous medium between two electrode pads, forming a simple metal-insulator metal (MIM) structure. While silver or copper are the most common electrochemically used active elements, common amorphous materials used include oxides and chalcogenides.

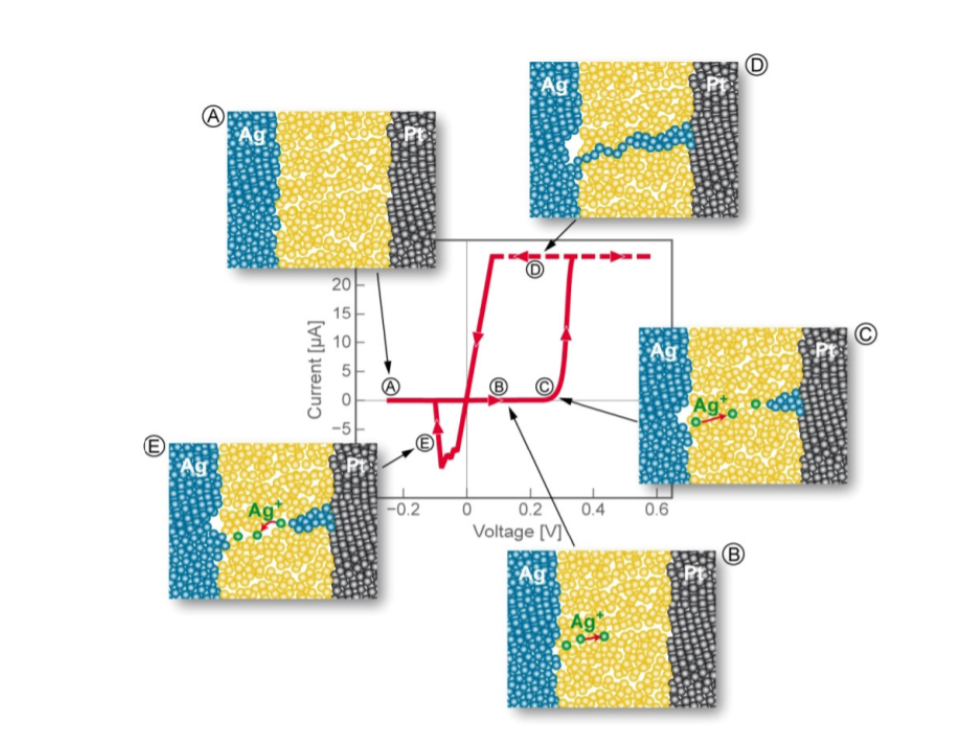
(LOW RESISTANCE STATE)

When a voltage bias is applied to the positive electrode, the active metal will oxidize and become a positive ion (Example, Ag → Ag+ + e −).

Now this positively charged metal ion will drift because of electric field through the amorphous layer. Finally, when the positively charged metal ion reaches the cathode, reduction would take place and the positive charge would then become neutral; this process is referred to as electrochemical deposition. Additional positively charged metal ions will then reach the now neutral metal and be reduced. Now this process would continue till active metal creates a conductive channel between the two electrodes. The conductive channel will be thicker in shape at the cathode because the bulk of electro-deposition occurs there.

(HIGH RESISTANCE STATE)

Now if the opposite polarity is applied, the role of the electrodes is reversed Now, the neutral metal in the conductive channel would be oxidized again and drift with the electric field, which is opposite to the original direction. Because of the lack of an active metal source on the cathode side of the device, the conductive channel will break down and the device will reach a high resistance state.To have a better understanding of such “ELECTROCHEMICAL METALLIZATION BRIDGE MEMRISTORS”, let us look at the picture below.

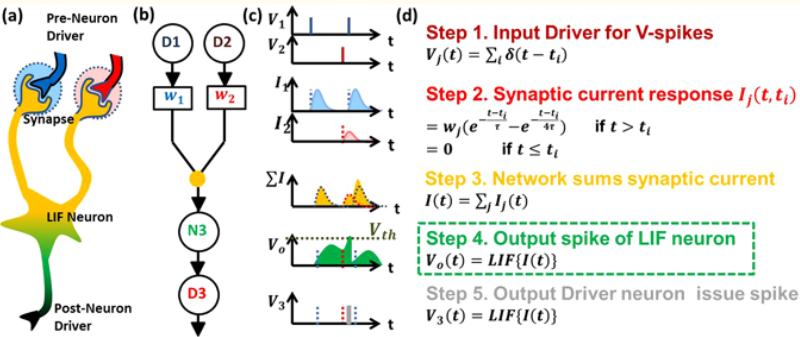


**Fig7. Working of chalcogenide-based ion-conducting variable resistance devices**

In Step “A” the device is usually in its high resistance state after its fabrication. When an electric field is applied atoms from the active metal layer oxidize and travel through the electrolyte layer as shown in “B”. Now as shown in “C” the active metal ions deposit on the surface of the inactive metal electrode layer. Now if we look at the I-v plot for the device we can see that from a->b due to lack of physical connection in the device we observer minimal current with increasing voltage. With repeated and concentrated deposition, a conductive metal dendrite forms across the electrolyte layer, thus from c->d we can see a drastic increase in the current flow in the device. Now, if an electric field is applied in the opposite direction, it returns active metal atoms to their original layer and causes disconnection. As, shown in the I-v plot, this metal dendrite disconnection returns the current to back zero which becomes our high resistance state.

**E) SPIKING NEURAL NETWORK AND LIF NEURON MODEL**

The figure below shows a simplified step-by-step representation of the SNN algorithm. The input voltage spikes are first given by presynaptic neuronal drivers D1 and D2 (where the ith spike occurs at time t = ti. Second, these feedback spikes are transformed into a slowly varying current signal proportional to synaptic weight (wj). Next, the network adds the current from synapses (w1 and w2) to the input of LIF neuron N3. Once the current from synapses are added, the LIF neuron (detailed description follows) integrates the input current through a capacitor, raising its potential. Once the potential reaches/exceeds a threshold, N3 resets (i.e., loses stored charge). Finally, every time N3 reaches threshold, a driver neuron D3 produces a spike. Unlike other neuronal models, the leaky integrate and fire (LIF) model can imitate the action of a biological neuron with the fewest possible circuit elements.



**Fig8. Working of SNN**

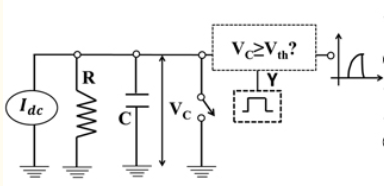
In general, each neuron in a spiking neural network has a membrane potential. When voltage crosses a threshold, an action potential or spike is emitted – the membrane potential then resets. Spikes are the main way in which neurons in SNN communicate. Spikes are very quick; voltage shoots up and then gets pulled down quickly. SNNs can be very efficient because they only perform computation when receiving spikes and such spiking activity is sparse.

There many different models, capturing different aspects of how neurons behave. Some of these are very complex and some require precise numerical simulations. One of such simple models to deal with is the LIF neuron model I.e., Leaky integrate and Fire neuron model.

**LIF MODEL:**

The LIF model describes a neuron as a parallel combination of a "leaky" resistor (gL) and a capacitor (C). Current source I(t) acts as a synaptic current supply, and is used to charge the capacitor and deliver a potential V(t). As the capacitor's potential reaches the level (V(t) Vth), the voltage-controlled transition discharges the capacitor to a resting potential, much like a biological neuron. When the voltage of the LIF neuron crosses the threshold, a separate driver circuit fires a spike. As a result, the LIF model is governed by the differential equation:

**C\*dv/dt = gL \*(V(t) -EL) + I(t)**

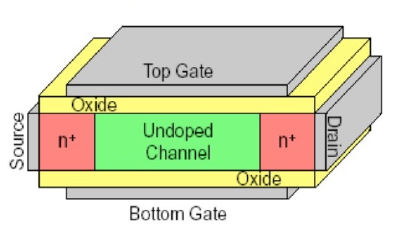


**Fig9. LIF neuron circuit model**

**D) DGFET (DOUBLE GATE JUNCTIONLESS FET)**

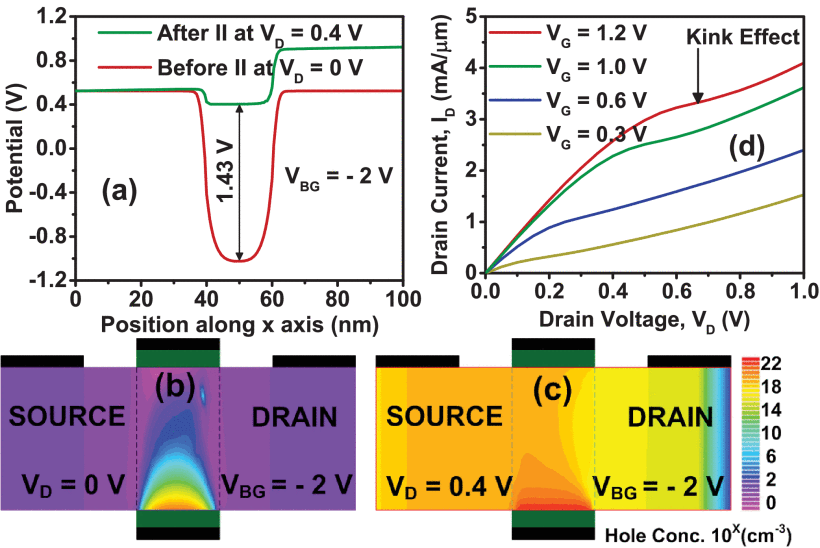
The Spiking Neural Network (SNN), which is inspired by neurobiology, allows for effective learning and recognition tasks. The spiking neural network (SNN) is an effort to comprehend and replicate human brain functions, which is a crucial obstacle for next-generation computing. To achieve a large-scale network akin to biology, a power and area efficient electronic neuron is essential. Si CMOS technology is mostly used for analogue application of electronic neurons, with which the dynamic nature of the cell has been successfully recorded. But we have a couple of constraints to deal with namely area and power, the individual components (e.g., neurons and synapses) must be highly area and power efficient. So, this is where DGFET comes into picture, the Impact ionization (II) induced floating body effect in SOI-MOSFET is used to capture LIF neuron behavior to demonstrate spiking frequency dependence on input. MHz operation enables attractive hardware acceleration compared to biology.

When comparing the DGFET configuration to that of a traditional MOSFET, we can see that the DGFET has only one kind of dopant from source to drain, resulting in a simpler fabrication process flow and lower thermal budget demand. Lower channel doping also allows for a higher ON state current and a lower subthreshold slope (SS). The DG-JLFET has two gates: a front-gate/top-gate (FG/TG) and a back-gate/bottom gate (BG). The top gate is used to ground the LIF, while the bottom gate is used to confine the holes near the channel-oxide interface and the bottom gate. As seen in the diagram below, a negative gate bias on BG induces channel depletion and hence the creation of a potential well.



**Fig10. DGFET structure**

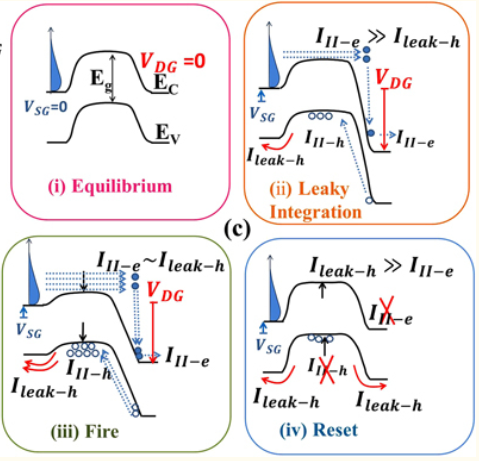
Now when a drain bias is applied, the electron-hole pairs are generated due to the ionization at the channel drain interface. The electrons are swept toward the drain and excess holes are confined in the potential well. The accumulation of excess holes results in a reduction of potential well depth after impact ionization. Also, we can clearly notice that it is due to the excess whole generation we have a kink in the output characteristics or I-v curve of DGFET.



**Fig11.Electrostatic potential variation and output characteristics of DGFET**

**DG-JFET LIF neuron**

To initiate impact ionization, a low VS and a high V DG are used; the induced electron current escapes through the drain, while the hole (h) current flows into the channel potential well. Some fraction of hole current leaks through the source barrier (equivalent to leaky integrate function in LIF).Over time, the net hole current which is the difference between hole current due to ionization minus the leakage hole current accumulates positive charges i.e., holes in the channel potential (equivalent to integrate function in LIF). Increasing holes charge lowers the source e-injection barrier electrostatically, allowing further electron injection for a stronger ionization and establishing a positive feedback loop. The e-injection barrier is reduced in tandem with the hole-well width, increasing the leakage hole current.

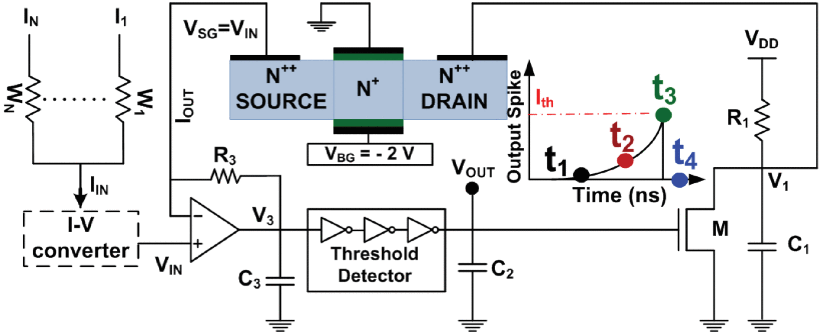


**Fig12. (i)Equilibrium band diagram (ii) Electron hole pair production as a result of ionization (iii) Barrier lowering as a result of hole accumulation iv) When the threshold is crossed (“fire event”), the VDG is removed, allowing the holes to escape through both junctions and restoring the barrier to its original location (“reset”).**

When the leakage hole current equals the ionization hole current, a steady state is reached, which prevents the formation of new holes. The new, however, crosses a pre-set threshold before reaching steady state (equivalent to fire function in LIF). The I(t) I th state activates a small "reset circuit" that disables impact ionization by removing drain bias (i.e., drain voltage is rendered zero). As a result, all of the deposited hole's leak into both the source and drain junctions, resetting the neuron to its original state. After the reset is complete, the drain is reset to high drain voltage and the LIF process is restarted after a normal timescale (called the "refractory period"). Thus, the dc input V in(t) produces cycles of leakage, integration, firing and resetting (LIF process) to produce firing frequency in the output drain current.

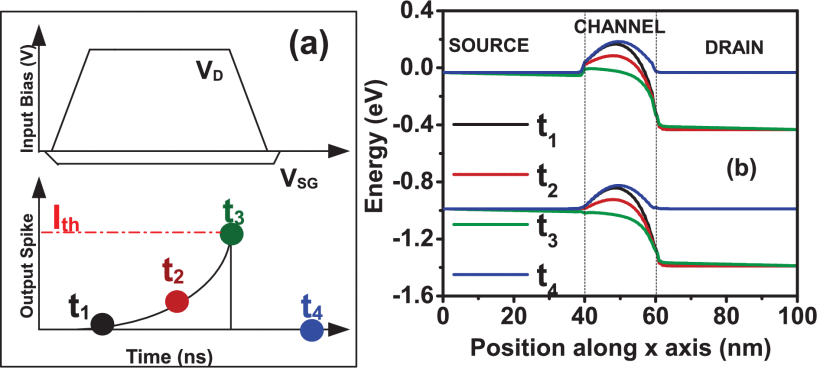
**Complete circuit of the proposed DG-JFET LIF neuron:**

A current to voltage (I –V) converter converts the current pulse (I1, I2, …., IN) obtained from presynaptic neurons through synapses to the corresponding voltage (VIN). The VIN is then transmitted to the DG-JLFET LIF neuron's source terminal via the Op- Amp's short terminals. When VIN=VSG (|VSG|>=Vth) and VD=VDD at time instant t1, the potential barrier in the channel is considerably higher, and there is minimal injection of electrons from the source region to the drain region, resulting in ionization being low and showing zero output current also, in addition, the channel area has a very low excess hole concentration.



**Fig13. DG-JLFET LIF neuron circuit**

In comparison to time instant t1, the potential barrier in the channel area is lower at time instant t2. As a result, further electrons are injected from the source region to the drain region, and when these electrons reach the drain region, the reverse bias around the drain junction is high enough to trigger the ionization, which causes holes to accumulate in the potential well, causing output current to rise. Furthermore, as holes accumulate in the potential well, the source to channel barrier decreases, allowing some holes to pass through the channel to the source area, resulting in a leaky DG-JFET LIF neuron that also initiates positive feedback.



**Fig14. Input voltage, Output current and energy along x-axis**

Furthermore, as time passes and t3 approaches, positive feedback reduces the potential barrier, resulting in a higher excess hole concentration in the channel area. As a result, IOUT rises dramatically, increasing the potential between the C2 and the C2 charges at the same time. when the potential across the capacitor C2 reaches the threshold voltage, the neuron fires and then resets abruptly because the transistor M switches on, causing the capacitor to discharge, V1 to decrease, and the DG-JLFET LIF neuron to lose the stored holes throughout the channel area. As a consequence, at time instant t4, output current reduces due recombination of holes present in the DGJLFET channel area, causing the DGJLFET LIF neuron to reset. As the potential across capacitor C2 falls below the threshold voltage, transistor M turns off, and C1 begins charging again, repeating the same integrate and reset cycle to ensure that each LIF cycle is equal.

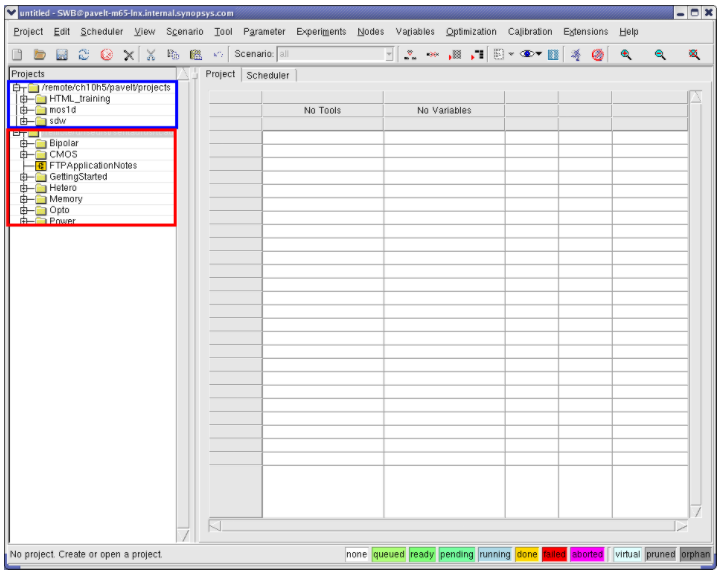
**SENTAURUS TCAD TOOLS**

**i) SDEVICE:**

The electrical behavior of a single semiconductor device in isolation or multiple physical devices integrated in a circuit is numerically simulated by Sentaurus Device. The physical system equations that characterize the carrier transport and conduction processes are used to calculate terminal currents, voltages, and charges.

**ii) SENTAURUS WORKBENCH:**

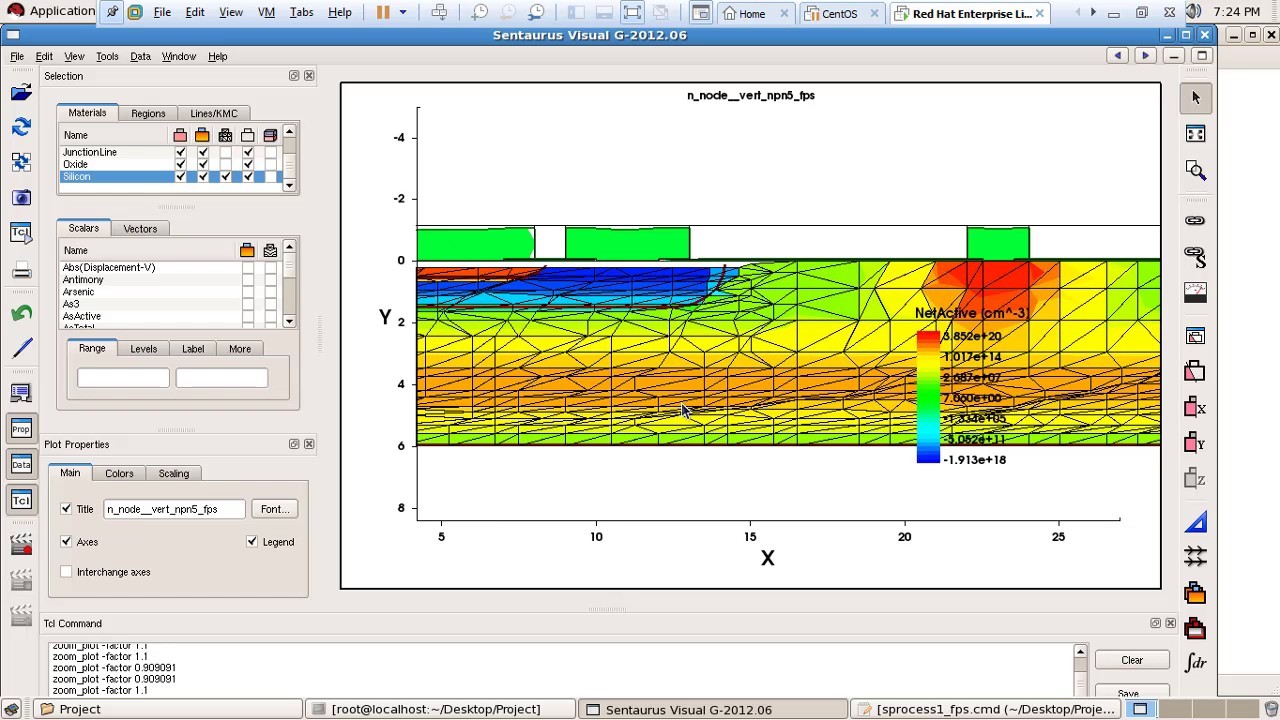
TCAD Sentaurus simulation tools are integrated into one environment by Sentaurus Workbench, which is the main graphical front end. It's used to plan, coordinate, and run simulations in the semiconductor industry. The information flow is managed dynamically by Sentaurus Workbench, which involves preprocessing user input files, parameterizing tasks, setting up and running tool instances, and visualizing output.



**Fig15. Sentaurus workbench window**

**iii) SVISUAL:**

Sentaurus Visual is an advanced visualization tool for TCAD data. It includes extensive capabilities for plotting and interactive manipulation of X-Y data and 2D/3D TCAD structures.

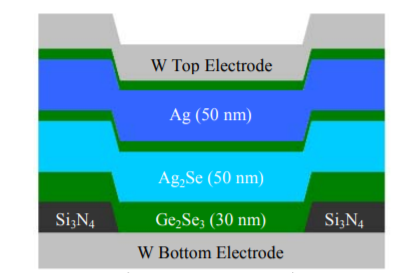
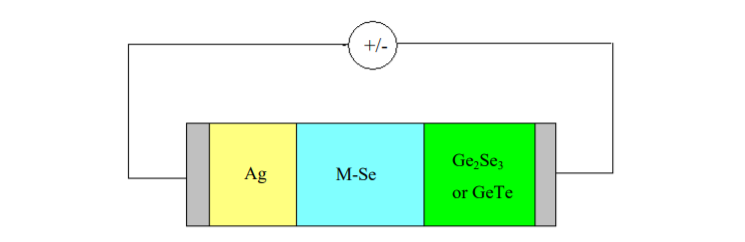


**Fig16. Sentaurus visual window**

**3) WORK DONE**

**I) Introduction to memristor design we will be working with:**

For our project we will be working with silver chalcogenide based memristor. Talking of the physical construction of the device, initially, Memristor devices were fabricated on 200 mm p-type Si wafers. Isolated bottom electrodes made of tungsten were patterned on the wafers and a planarized nitride layer was used for device isolation (similar to LOCOS in CMOS technology). Vias were etched through the nitride layer to provide contact to the bottom electrode. The memristor device structure consists of the layers (from bottom electrode contact side to top electrode contact): **300 Å Ge2Se3** / **500 Å Ag2Se**/ **100 Å Ge2Se3**/ **500 Å Ag**/**100 Å Ge2Se3.**

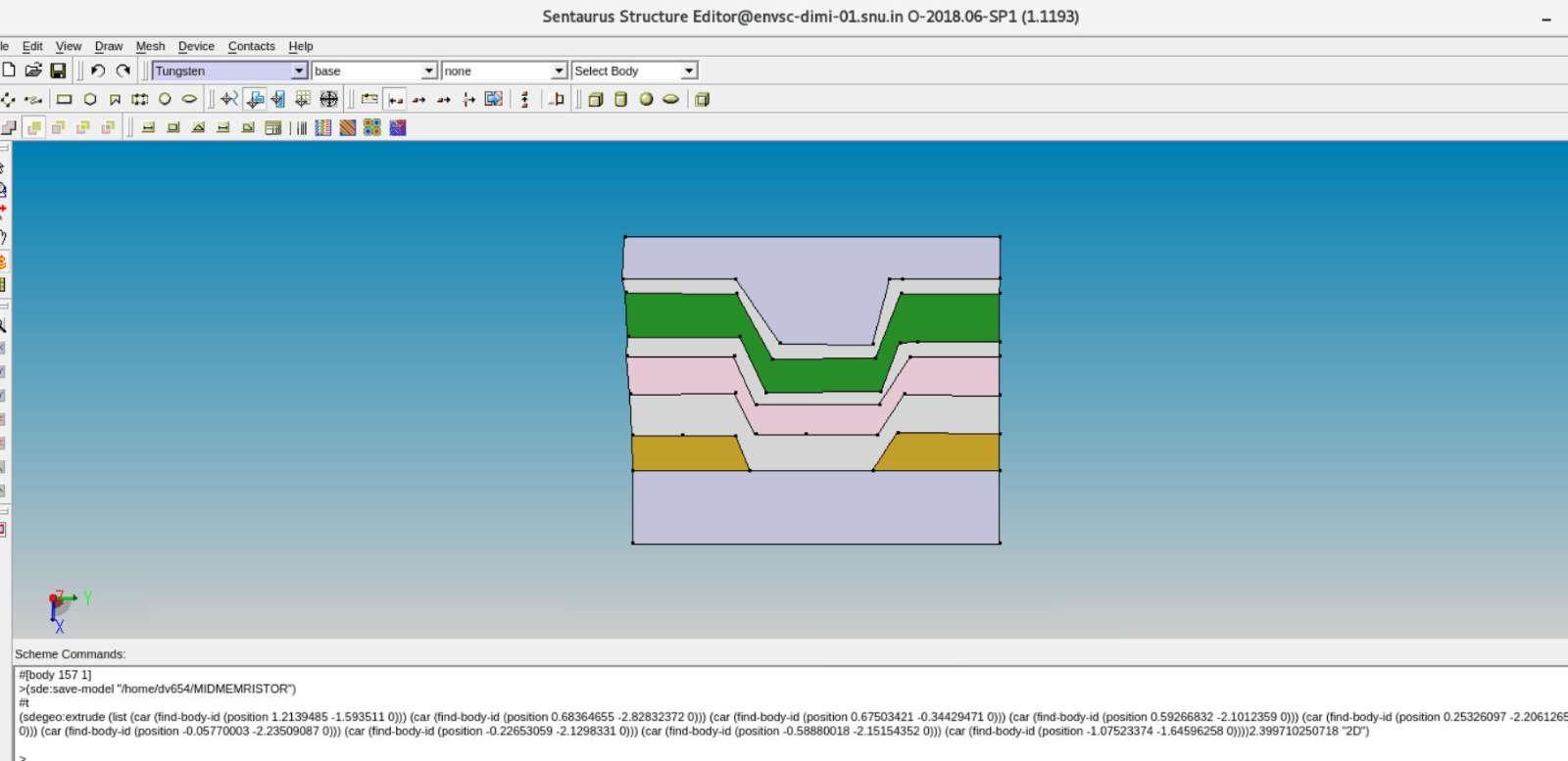
**Fig17. Structure of electrochemical metallization Fig18. Biasing of EMB memristor**

**Bridge memristor**

As discussed above, we can notice that here we have two additional germanium selenide layers of 100 Armstrong, this is because the 100 Å Ge2Se3 layers are needed for device processing only since Ag cannot be deposited directly on Ag2Se and since W (for the top electrode) does not adhere well to Ag in this material stack.

The exact mechanism by which the Ag (or Cu) forms and dissolves as a conductive channel has not been fully understood. However, one theory that can put forth to explain the working of this device is that the amorphous chalcogenide films I.e., the germanium selenide in this case provides the pathway for fast transport of cations like silver in a reduction-oxidation (redox) reaction when a potential is applied to the electrodes. The ease with which this happens not only depends on the 4 applied potentials but also on the structure of the amorphous chalcogenide. And here, the blue middle layer having Ag2-Se is the amorphous insulation layer, where silver can be replaced with various other metals. Using different materials for the M-Se layer, different device characteristics can be achieved.

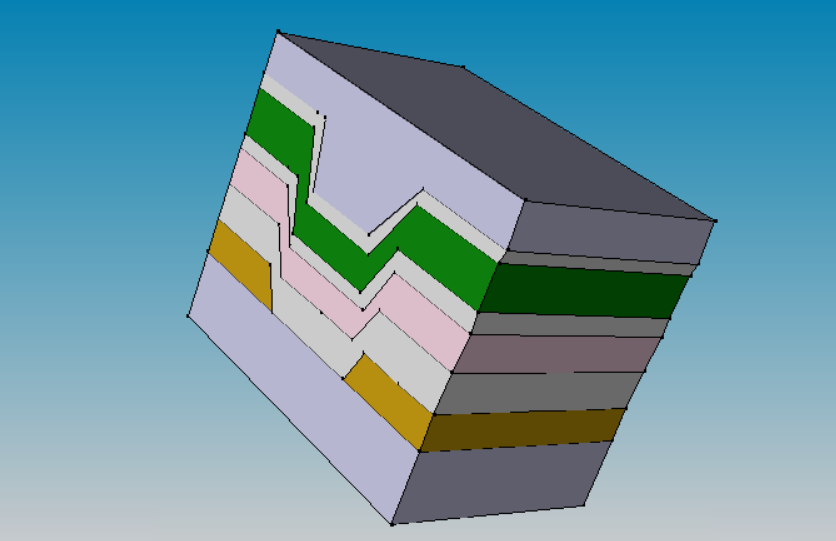
**II) Building 2D/3D models of required memristor in SDE:**



**Fig19. 2D model of memristor in SDE**

First, we shall open SDE and define our structure regions using 2D create tools (mainly polygon) and a few other options such as Snap to vertex. Once the 2D structure has been created successfully we use the extrusion option available to us in SDE to convert the initially created 2-dimensional device structure into 3-dimensional structure.

As we can see in the picture above the bottom and top layers are essentially the tungsten electrodes. The orange layer above is the si3n4(Silver nitride layer). However, while working using SDE one can notice that we are provided with access to a limited number of materials. Since Germanium selenide (chalcogenides) are not available, I have used GaAs (Gallium arsenide) as a replacement since Gallium arsenide also acts as an amorphous semiconductor. Then finally the green layer we can see in the picture is the silver layer (The main active region where oxidation-reduction process takes place).



**Fig20. 3D model of memristor structure in SDE**

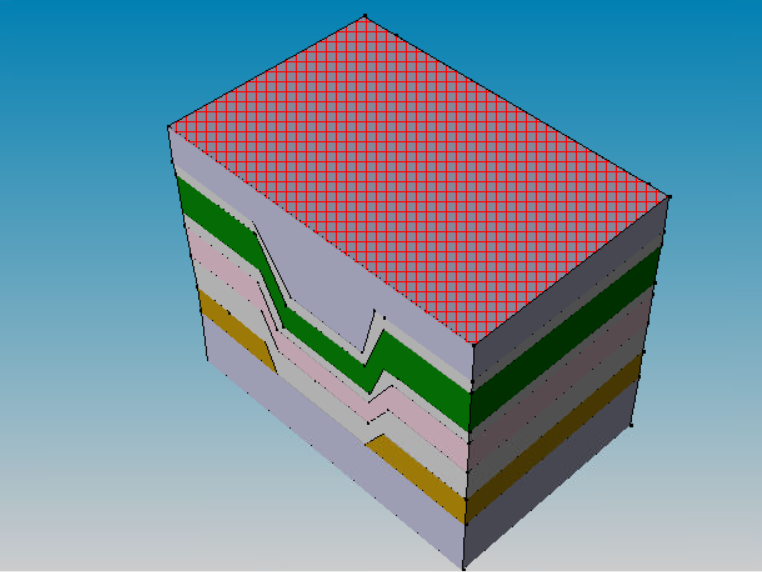
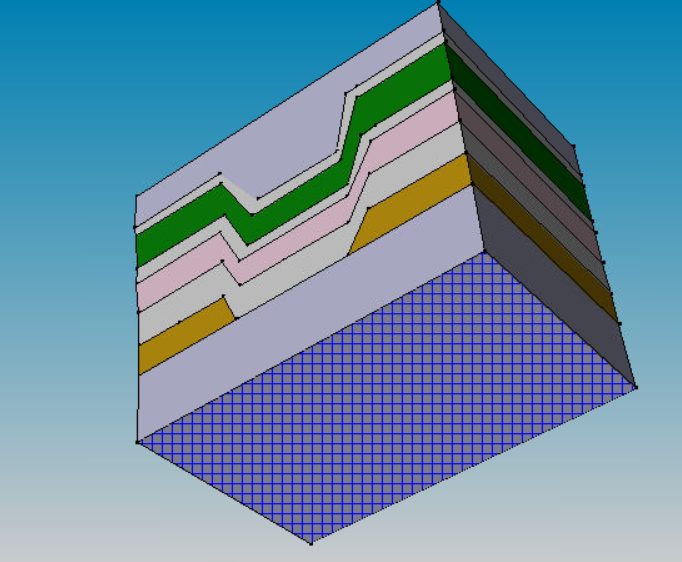
|  |  |  |
| --- | --- | --- |
| Serial No | Material Used | Color in model |
| 1 | Tungsten | Grey |
| 2 | Silver | Green |
| 3 | Gallium Arsenide | White |
| 4 | Silver Selenide | Pink |
| 5 | Silicon nitride | Orange |

**Fig21. Table having details about materials used and their respective colors in SDE structure**

Once we have extruded the structure to its three-dimensional model using SDE, we now have to define contacts for the memristor through which we will be biasing the memristor. To define contacts, go to,

**Contacts -> contact set -> Write down contact name-> Choose the required color (RGB combinations)-> Set**

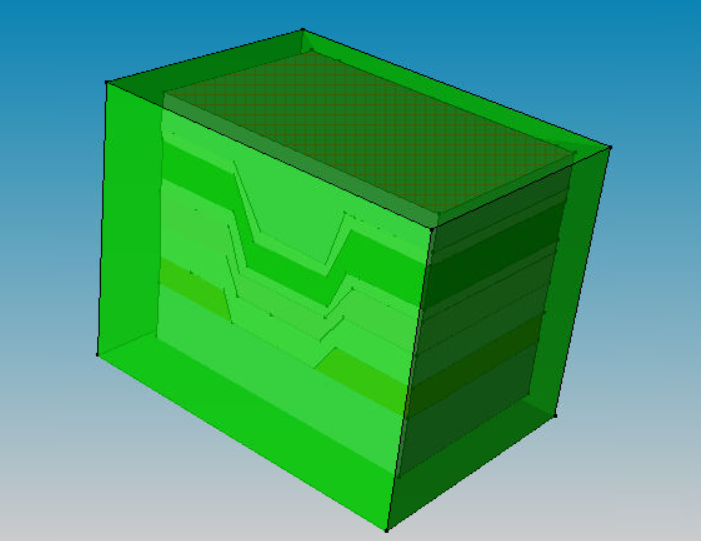
Using the above steps, we have to define the cathode and anode contacts for memristor. Once the contacts have been defined select the bottom and topmost face of the 3D model (tungsten) and correspondingly apply the defined cathode and anode contacts to memristor structure respectively.



**Fig 22. Cathode contact of the memristor Fig23. Anode contact of the memristor**

**iii) Mesh Generation:**

Once we have designed structure of the device, we will now have to pass this structure to the simulator for device simulations. Using the drift-diffusion approach for simulation we usually tend to deal with 5 types of equations, Poisson equations, Continuity equations (2), and Current density equations (2) which are continuous in nature, but since computer would only understand discretized values, we would like to discretize continuous values. We do this with the help of meshing.



**Fig25. Defined mesh on 3D memristor structure**

Now to create a mesh we need to first create a reference / evaluation window. In order to create a Ref/Eval window, the steps are as follows:

1. Mesh > Define Ref/Eval Window

2. Select the shape of the Ref/Eval window (Since our figure was 3d, we chose a cuboid shape)

3. Draw the Ref/Eval window (2D) / Input the coordinates of vertices of the cuboid window (3D)

Here we need to ensure that the entire structure would be enclosed by the mesh, so it is only through a trial-and-error process that we can exactly fit the structure into the cuboidal mesh window.

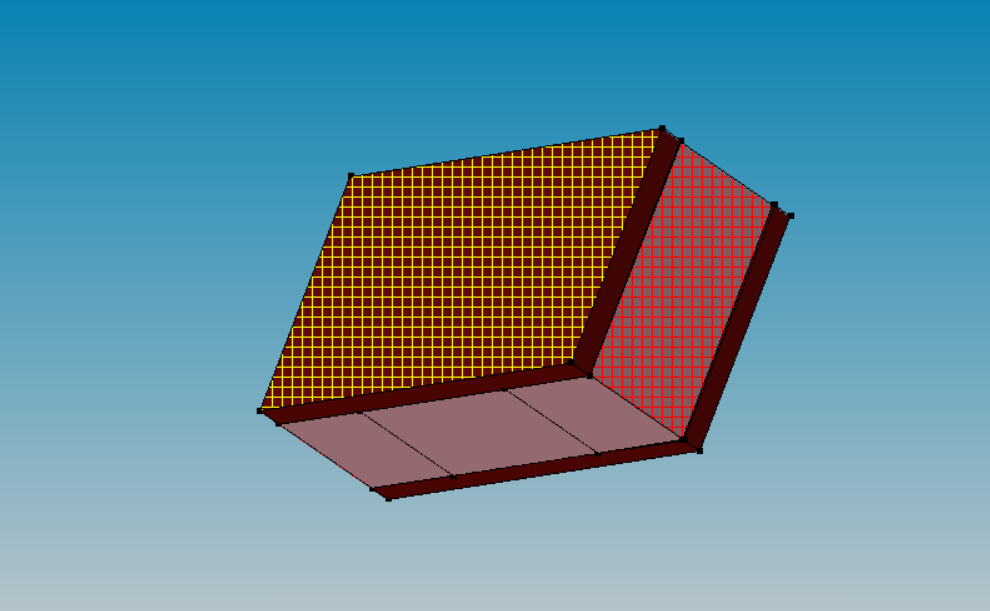
**SHIFT FROM MEMRISTOR TO DGFET:**

The main goal of this research project was to design and model a device to be used in neuromorphic computing using Sentaurus TCAD tool. So, initially we started working on memristor and structure was well defined with all materials and doping profiles.

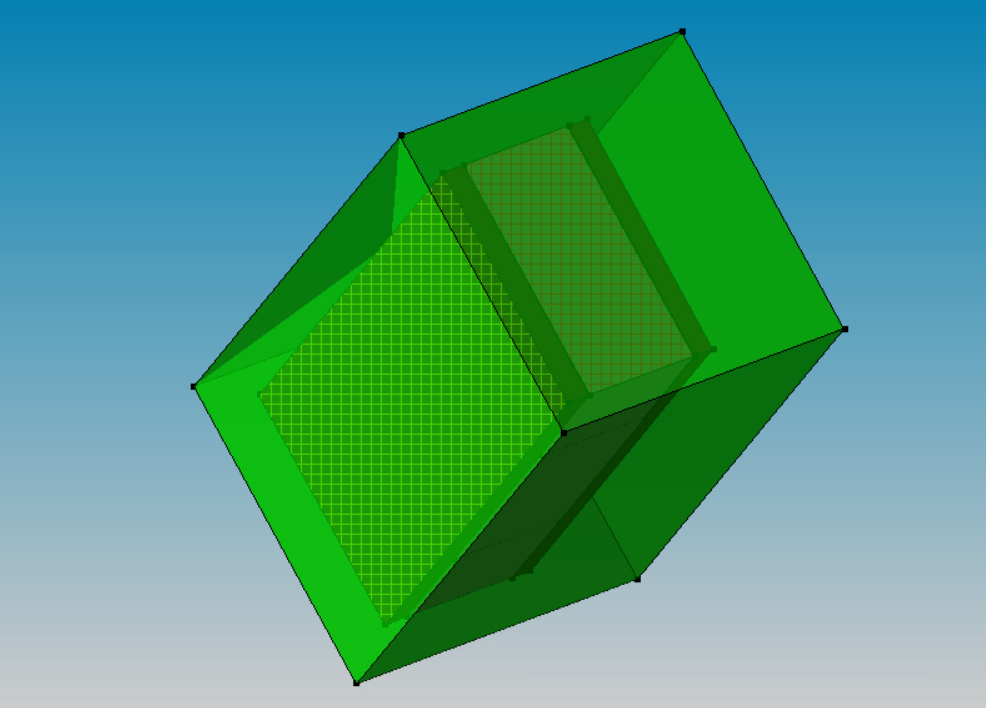
Then, once the meshing was done a .tdr file was generated. Once the tdr file has been generated and meshing has been successfully done, we now need to run the command file to simulate the structure. For memristor’s simulation we need to plug in well-defined ionic mobility models for simulation and then run it. But since models haven’t been well defined for memristor in TCAD tools, we will not be able to simulate the device properly and optimize the device. Now we look for an alternative device which not only has well defined models for simulations to be run but also should have better reliability, better calibrated and controlled CMOS process. We find out the DGFET is the ideal choice. To achieve a large-scale network akin to biology, a power and area efficient electronic neuron is essential. So, after midterm our primary focus has been to design and model DGFET as LIF (Leaky Integrate and Fire) neuron model.

**4) RESULTS**

To begin with we started off by designing the structure of DGFET in Sentaurus structure editor.

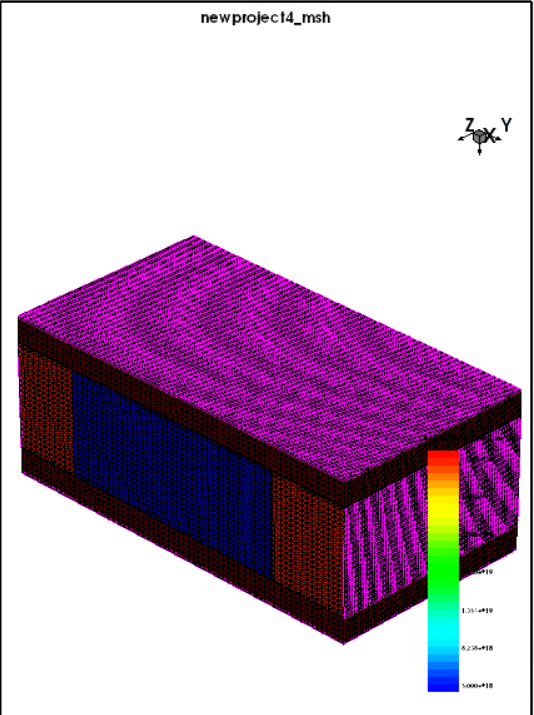


**Fig26.DGFET structure in sentaurus device editor with contacts**



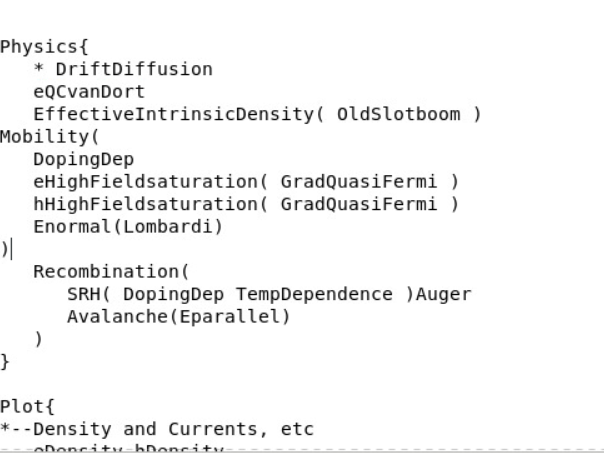
**Fig 27.Meshing of DGFET**

In comparison to the conventional MOSFET, the DG-JLFET has a similar kind of dopant (n-type) from source to drain. But the channel has a doping of (5E-18) and Source and Drain have been doped with phosphorus to have a Concentration of (1E-20). And above and below our silicon body we have a front and back gate both made from Silicon dioxide. Once the meshing was the following .tdr was shown in Sentaurus visual.



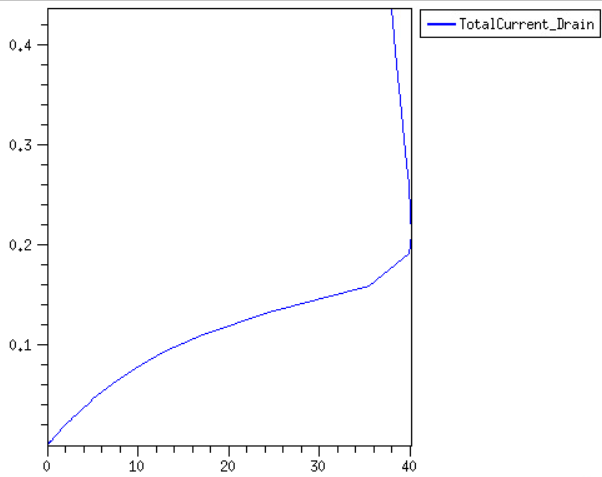
**Fig 28.Meshed structure of DGFET from .tdr file in Visual**

The TCAD tool Sentaurus is used to verify the behavior of the proposed DG-JFET LIF neuron. The following models were incorporated to characterize the DG-JET's DC and LIF characteristics.



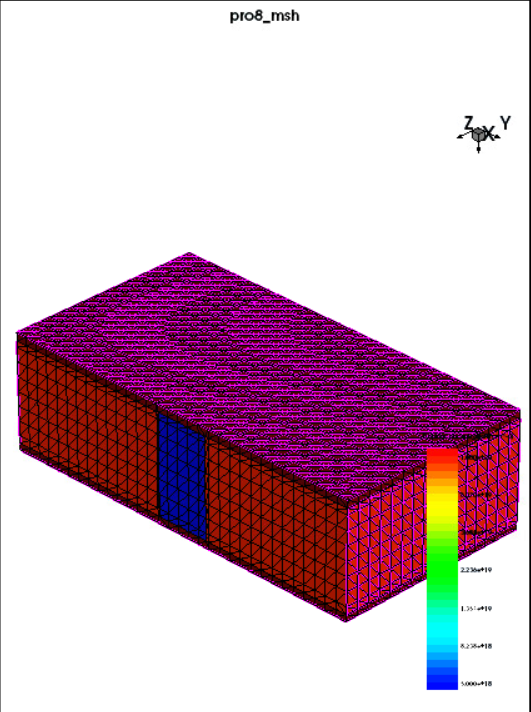
**Fig29. Simulation command file code snippet**

On simulating the above structure, we got the following output curve I.e. I-V characteristics of DGFET with y-axis representing the total drain current and x-axis representing drain voltage. We can clearly notice a kink in the graph which confirms impact ionization happening in the device. Impact ionization causes a build-up of h-charge, resulting in a slower increase in current (i.e., integration). As a result, the e-injection threshold is reduced, allowing more current to be injected.

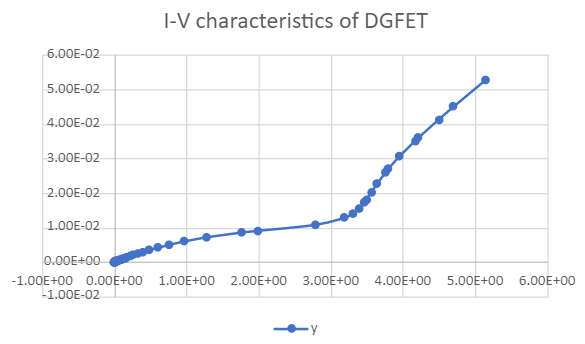


**Fig30. I-V characteristics of DGFET (not scaled using parameters)**

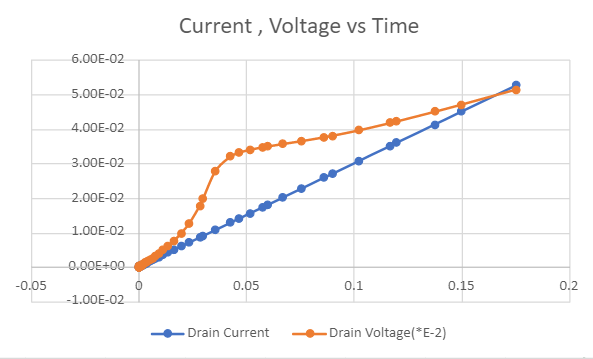
On noticing the obtained I-V curve we clearly see that our device is operating at very high voltages, this is because this initial design of our DGFET had a very thick oxide layer (close to 100 nanometers) and the device was not scaled properly. Each simulation was taking around 2 hours approximately. Now, once the device was properly scaled using schematic commands and oxide was made thinner. We get the following mesh file and output curves were obtained,



**Fig31. Meshed structure of properly scaled DGFET structure**

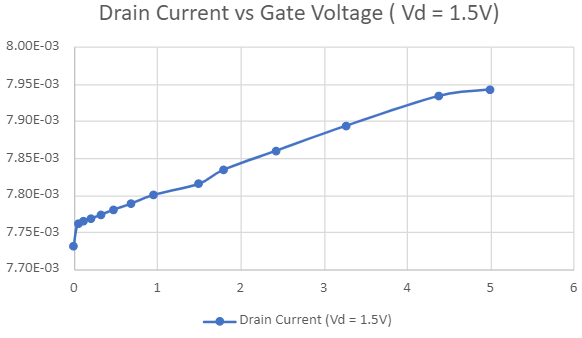


**Fig32. Output characteristics of DGFET**

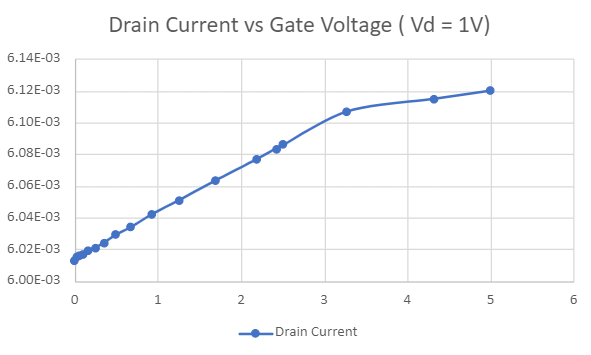


**Fig33. Current vs time and Voltage vs time for DGFET with Vg=1volt**

Here from the above I-V curve we can clearly see that the device after proper scaling is operating at a much lower voltage when compared to earlier case. Now if we try varying the gate voltage at a constant drain voltage and observe the drain current (Id), we notice that drain current increases either if we increase gate voltage or drain voltage.

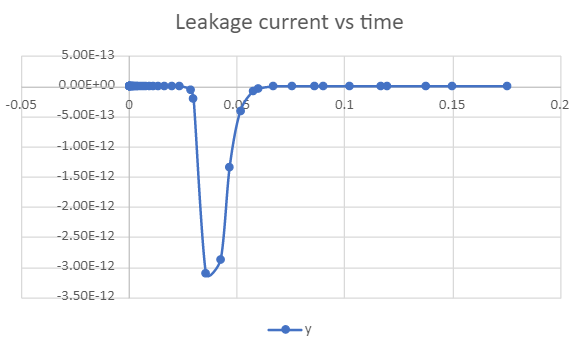


**Fig34. Drain current (Id) vs Gate Voltage (Vg) graph (Vd=1.5V)**

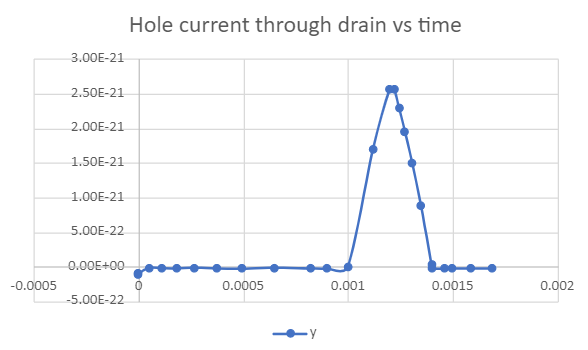


**Fig35. Drain current (Id) vs Gate Voltage (Vg) graph (Vd=1V)**

The electrons travel from the source to the drain area under the biassing conditions of |VSG|>Vth and gain energy due to the strong electric field at the channel-drain interface, resulting in ionization. Electrons and holes are formed and travel toward the drain and near the bottom gate respectively. The hole aggregation near the bottom gate lowers the source-channel barrier, allowing hole leakage from the channel to the source side, demonstrating the proposed DG-JFET LIF neuron's leaky neuron. In the figure below we can the current through the source which is the leakage current.

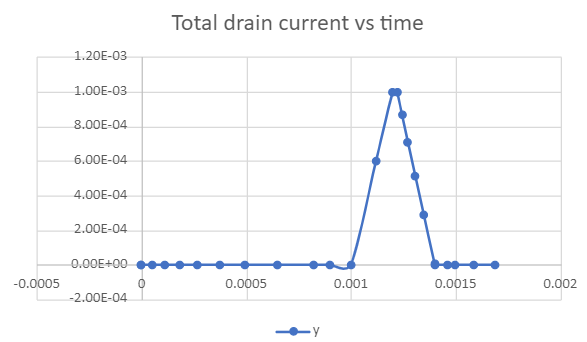


**Fig36. Leakage current (Source) vs time**



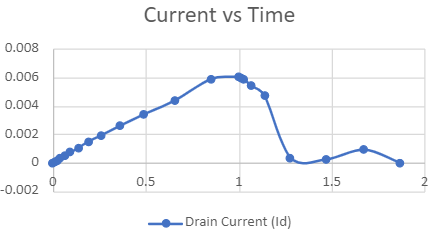
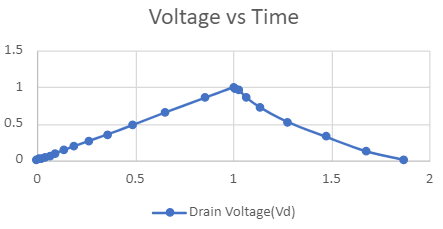
**Fig37. Hole current vs time**

For the source-gate voltage less than the threshold voltage, no spikes are generated because ID saturates before reaching Ith. But for source-gate voltage greater than the threshold voltage, the ID reaches Ith (leaky-integration), and as it surpasses the Ith a spike is generated (fire), as shown in above which is followed by forced reset by making drain voltage zero I.e., Vd=0

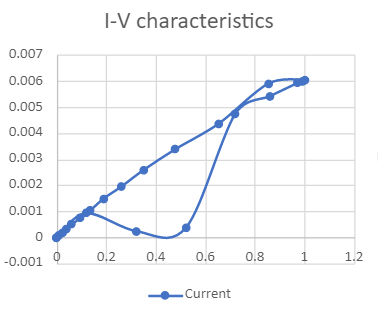


**Fig38. Drain Current Vs Time**

If a triangular waveform is given as input following are the current and I-V characteristics of our simulated DGFET devices.



**Fig39. Input voltage vs time Fig40. Drain current vs Time for triangular wave**



**Fig40. Output characteristics of DGFET for Vd=0->1->0**

**5) CONCLUSION**

The main aim of this research project was to explore and work with different devices which are used to implement neuromorphic computing. To achieve such a massively parallelly connected large-scale network similar to biological networks, a power and area efficient electronic neuron is essential. We first started the project with memristor where we familiarize ourselves with working on memristor devices, Sentaurus TCAD and also introduced ourselves to artificial neural networks, spiking neural networks. Halfway through the project when we were simulating the memristor model we faced difficulties mainly because of the fact the mobility models we plug-in our TCAD simulations have not been well defined yet which directly states the fact that we cannot optimize the memristor device properly. So, as an alternative to memristor we look for a device with similar behavior having better reliability, more controlled and CMOS process, having well defined ionic conduction simulation models for devices and can be used in modelling a neuron using existing models. DGFET is one such device.

Then we started working on the DGFET’s (Double Gate Junctionless Field Effect Transistor) structure using Sentaurus TCAD. Once the device’s most optimized structure was properly defined using a structure editor, we simulated various command files using Sdevice. Now, on observing the graphs obtained from various simulations such as the I-V characteristics or Current-Time plots we can clearly conclude that our DG-JLFET based LIF neuron can be used for the realization of SNN in the nanometer regime. To initiate impact ionization, a low VS and a high V DG were used; the induced electron current escapes through the drain, while the hole (h) current flows into the channel potential well. Some fraction of hole current leaks through the source barrier (equivalent to leaky integrate function in LIF). Over time, the net hole current which is the difference between hole current due to ionization minus the leakage hole current accumulates positive charges i.e., holes in the channel potential (equivalent to integrate function in LIF). Increasing holes charge lowers the source e-injection barrier electrostatically, allowing further electron injection for a stronger ionization and establishing a positive feedback loop. The e-injection barrier is reduced in tandem with the hole-well width, increasing the leakage hole current. When the leakage hole current equals the ionization hole current, a steady state is reached, which prevents the formation of new holes. Now, the I(t)>Ith state activates a small "reset circuit" that disables impact ionization by removing drain bias (I.e., drain voltage is rendered zero). As a result, all of the deposited hole's leak into both the source and drain junctions, resetting the neuron to its original state.

**5) References**

[1] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, “The missing memristor found,” Nature, vol. 453, no. 7191, pp. 80–83, 2008.

[2] V. Saxena, "A Compact CMOS Memristor Emulator Circuit and its Applications," *2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, Windsor, ON, Canada, 2018, pp. 190-193, doi: 10.1109/MWSCAS.2018.8624008.

[3] L. Chua, "Memristor - The Missing Circuit Element," IEEE Transactions on Circuits Theory (IEEE), vol. 18, no. 5, 1971, pp. 507– 519

[4] R. S. Williams, “How We Found the Missing Memristor,” IEEE Spectrum, vol. 45, no. 12, 2008, pp. 28-35

[5] L. Chua and S.M. Kang, “Memristive Device and Systems,” Proceedings of IEEE, Vol. 64, no. 2, 1976, pp. 209-223

[6] Chen, Jau-Tzuoo. "OXYGEN AND SILVER-OXYGEN DEFECTS IN Ge2Se3vELECTROCHEMICAL METALLIZATION BRIDGE MEMRISTORS." (2018).

[7] A. S. Oblea, A. Timilsina, D. Moore and K. A. Campbell, "Silver chalcogenide based memristor devices," *The 2010 International Joint Conference on Neural Networks (IJCNN)*, Barcelona, Spain, 2010, pp. 1-3, doi: 10.1109/IJCNN.2010.5596775.

[8] Cook, Beth Rose, "Electrical Switching Studies of Chalcogenide-Based Ion-Conducting Variable Resistance Devices" (2011). *Boise State University Theses and Dissertations*. 193.

[9] A. Rothenbuhler, *A memristor-based neuromorphic computing application*, 2013.

[10] Memristor. (2021, February 01). Retrieved February 21, 2021, from <https://en.wikipedia.org/wiki/Memristor>

[11] The memristor. (2018, February 03). Retrieved February 21, 2021, from <https://www.americanscientist.org/article/the-memristor>

[12] N. Kamal and J. Singh, "A Highly Scalable Junctionless FET Leaky Integrate-and-Fire Neuron for Spiking Neural Networks," in IEEE Transactions on Electron Devices, vol. 68, no. 4, pp. 1633-1638, April 2021, doi: 10.1109/TED.2021.3061036.

[13]1. Leaky-integrate-and-fire model¶. (n.d.). Retrieved March 30, 2021, from <https://neuronaldynamics-exercises.readthedocs.io/en/latest/exercises/leaky-integrate-and-fire.html>

[14]An introduction to neural networks. Retrieved March 20,2021, from

<https://developer.ibm.com/articles/l-neural/>

[15]F. Caravelli, F. L. Traversa and M. Di Ventra,”Complex dynamics of memristive circuits: Analytical results and universal slow relaxation”, in PHYSICAL REVIEW E 95, 022140 (2017)

DOI: 10.1103/PhysRevE.95.022140

[16]. Hickmott, T. W. J. Appl. Phys. 33, 2669–2682 (1962)

[17]Hu, Xiaolin. *Advances in Neural Networks - ISNN 2015: 12th International Symposium on Neural Networks, ISNN 2015, Jeju, South Korea, October 15-18, 2015, Proceedings*. Springer, 2018.

[18]Published online: 14 May 2018 <https://doi.org/10.1038/s41928-018-0083-3>