Mobile PCI Express Module Electromechanical Specification

Version 3.0
Revision 1.0

June 26, 2008

Revision History

Rev	Resp	Change
1.0	GG	Initial release.

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Chapter 1

Introduction

The Mobile PCI Express Module (MXM) is a standard graphics interface for PCI Express® systems. This specification describes the electrical, mechanical and thermal interfaces for the MXM version 3.0 Graphics Module.

MXM is the ideal solution where there is a need for low power, small form factor, high performance graphics adapter. Typical applications include notebook computers, blade and standard rack mount servers, mobile workstations and alternative form factor PCs including all-in-one, home theater and small form factor PCs.

An MXM version 3.0 module is identified by its type (A or B). Each type has a distinct form factor and is aimed at different performance requirements and power consumption.

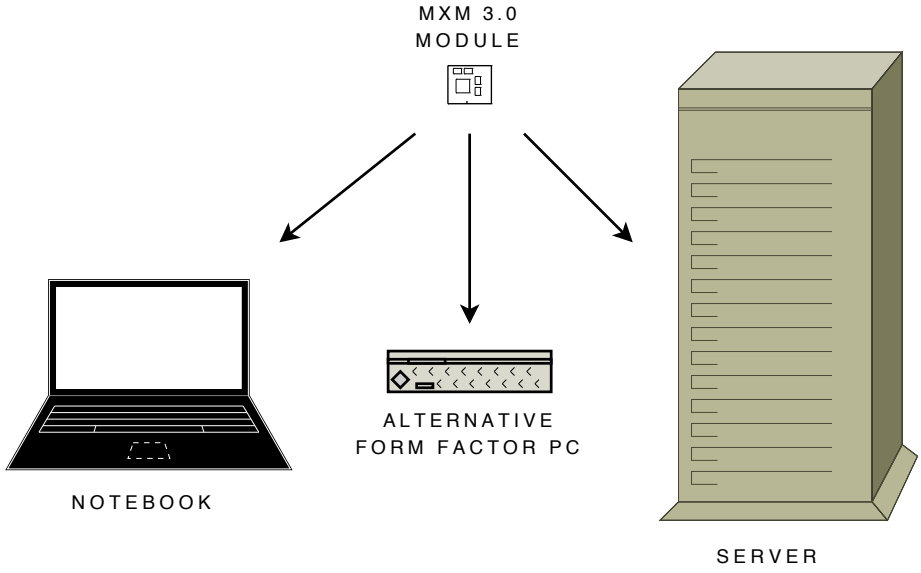


Figure 1.1: MXM Applications

1.1 Background

MXM version 3.0 builds upon the experience gained during several years of implementation of the previous versions of the MXM standard (1.3, 2.0 and 2.1A).

MXM version 3.0 , while physically very similar to the previous standards, is not compatible with any of them, mechanically or electrically. Whereas the previous versions of MXM offered upgrade capability

through installation of an MXM module, mechanical differences between the modules prevented a motherboard from accommodating every module in a particular MXM revision. MXM version 3.0 specifically addresses this by using a single style connector (rather than the previous two) and a single pinout for all modules. Additionally the two form factors specified by MXM version 3.0 have identical 3D forms where they overlap, the larger of the two modules has the same 3D profile as the smaller module plus an extension. This was done to enable systems with a wide range of upgradeability. MXM version 3.0 adopters have the opportunity to design a single thermal solution that could be used with all their MXM version 3.0 designs.

Finally the MXM version 3.0 connector has been developed with controlled impedance contacts. It is the same physical size as the previous MXM version 2.X High End connector yet has almost 25% more signal contacts. This gives MXM version 3.0 module significantly more capability.

1.2 MXM Version 3.0 Benefits

The MXM version 3.0 specification defines two electrically, mechanically and thermally compatible form factors (Type A and Type B). The thermomechanical compatibility allows the use of Type A modules on Type B systems without any modification to the thermal solution or to the system mechanical design.

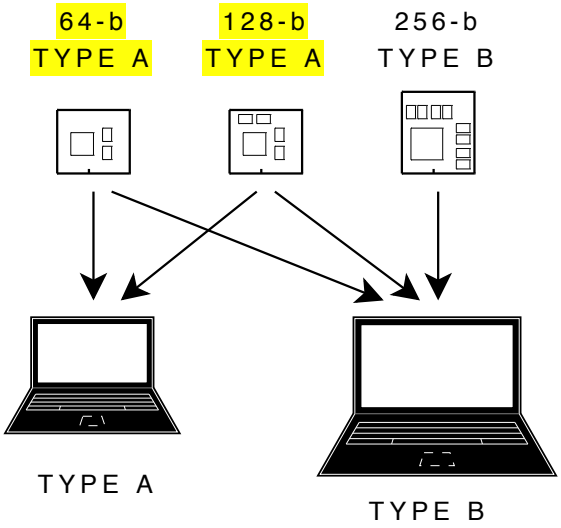


Figure 1.2: MXM Compatibility

MXM version 3.0 supports the following key features:

- Up to 16 lanes PCI Express V2.0
- Up to 8 DDR2, DDR3, GDDR3 or GDDR5 memories
- Up to 4 Dual-mode DisplayPort™ (all support DVI and HDMI™)
- Single 24-bit dual-link LVDS, dual-link DVI and HDMI
- Single VGA and TV-out

1.3 Display Support

This specification allows multiple display configurations depending on the board and GPU features. Table 1.1 shows the minimum required set of displays that a module must support. Any other display is optional on the module. All display outputs are optional on the system (the system is allowed to have no display).

Table 1.1: Required and Optional Display Support

Interface	Description	Module	System	Dual-mode DP
DP_A	DisplayPort	required	optional	required
DP_B	DisplayPort	optional	optional	optional
DP_C	DisplayPort	required	optional	required
DP_D	DisplayPort	optional	optional	optional
DP_A+DP_B	dual-link DVI (MXM specific implementation)	optional	optional	N/A
DP_A+DP_C	dual-link DVI (MXM specific implementation)	optional	optional	N/A
DP_C+DP_D	dual-link DVI (MXM specific implementation)	optional	optional	N/A
LVDS	18 and 24-bit dual-link LVDS	required	optional	N/A
LVDS	dual-link DVI	optional	optional	N/A
LVDS	HDMI	optional	optional	N/A
VGA	VGA RGB interface	required	optional	N/A
VGA	TV Out interface	optional	optional	N/A

Note: DisplayPort A and C interfaces are required to be Dual-mode capable. The system designer may choose to provide a Dual-mode connector or level shift the signals on the system board and provide a native DVI or HDMI connector. Refer to Section 3.4.6 for details. Dual-mode support for DisplayPort B and D is optional.

1.4 Required/Optional Feature Matrix

Table 1.2 shows the summary of the features with implementation requirements on both the module and the system. An MXM version 3.0 compliant module must implement all features marked "required" on the module column. A compliant system must implement all features marked "required" in the System column.

Table 1.2: Required and Optional Feature Matrix

Interface/Signal	Description	Module	System
PCIe	PCI Express interface x1	required	required
PCIe	PCI Express interface x2, x4, x8, x16	optional	optional
PCIe	PCI Express lane reversal	required	optional
PNL_xxx	Internal flat panel control interface	required	optional
GPIOx	General purpose I/O	required	optional
PWR_LEVEL	Power management interface	required	optional
SMB_xxx	System Management Bus interface	required	optional
TH_OVERT#	Thermal shutdown request	required	required
TH_ALERT#	Thermal interrupt request	required	optional
TH_PWM	Thermal PWM	optional	optional
PWR_GOOD	Power sequencing sideband	required	optional
PRSNT_x#	MXM module present detect	required	optional
WAKE#	System wake signal	optional	optional
PWR_EN	Module power enable	required	required
PEX_CLK_REQ#	PCIe clock request	optional	optional
PEX_STD_SW#	PCIe swing control	required	optional
VGA_DISABLE#	Primary/secondary display select	optional	optional
HDMI_CEC	HDMI 1-wire CEC bus	optional	optional

Chapter 2

Mechanical Specification

This chapter describes the MXM version 3.0 form factors and the associated keep-out zones.

Note: Metric dimensions are the controlling dimension. English equivalents given in brackets may be affected by rounding errors and are provided for reference only.

2.1 Form Factors

The two types of MXM modules have their own form factor and compatible mechanical keep-outs. The keep-outs are necessary for system and thermal solution integration compatibility. The keep-outs are a combination of z-height restrictions and surface keep-outs on the MXM module.

The GPU must be placed on the top side at the center of the GPU zone to ensure proper load balancing whereas the memories can be placed anywhere within the memory zone. The minimum GPU height supported by this revision of the specification is 1.75 mm. The following keep-out definitions include a 0.5 mm clearance from the thermal solution in the x and y direction.

The dimensions for each drawing are tabulated in a related table for easier identification. Where a dimension is repeated on another drawing, it is given the same designation as previously used.

Basic dimensions (used for Geometric Dimensioning and Tolerancing) and reference dimensions do not have associated tolerances in the tables. Some reference dimensions are toleranced later in the specification using the same designation while others are obtained from detailed review of the required component.

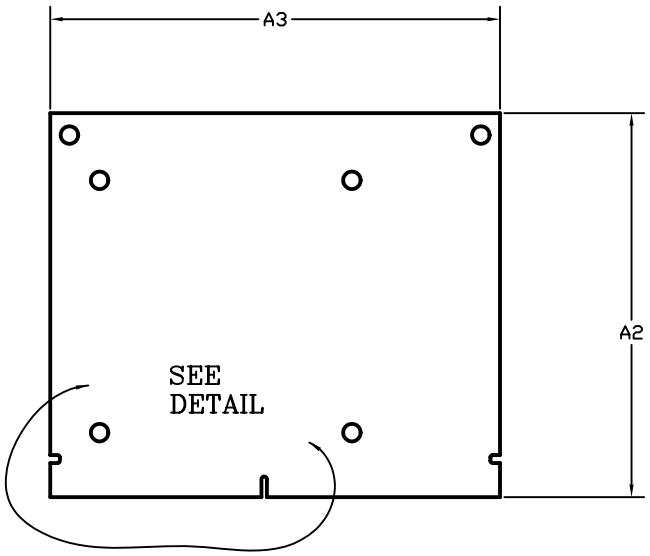
Note: Tolerances unless otherwise stated are +/- 0.13 [0.005]

2.2 MXM Board Outlines

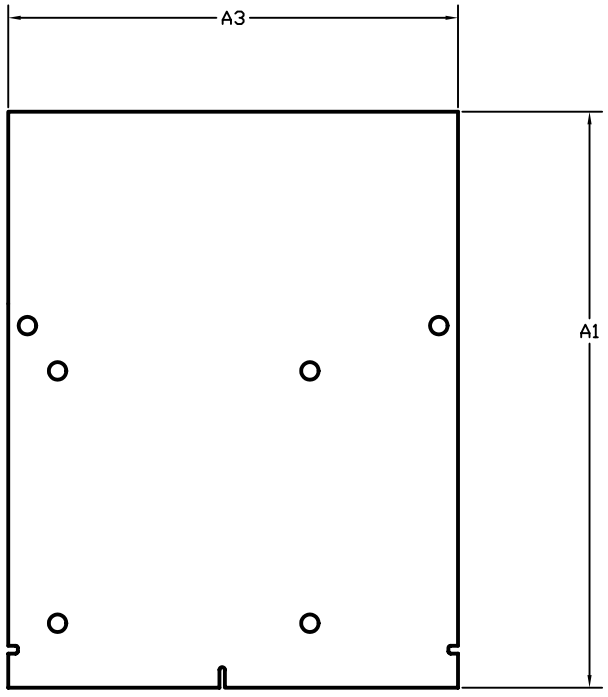
Figure 2.1 shows the board outlines (top side view) for both Type A and Type B MXM modules.

Table 2.1: Board Outline Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
A1	104.87	105.00	105.13	4.129	4.134	4.139
A2	69.87	70.00	70.13	2.751	2.756	2.761
A3	81.87	82.00	82.13	3.223	3.228	3.233



TYPE A



TYPE B

Figure 2.1: Board Outlines

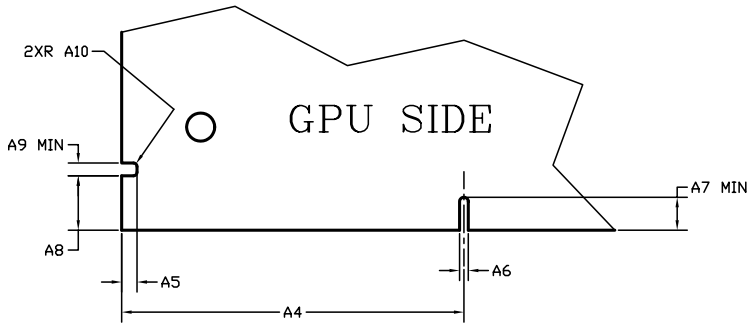


Figure 2.2: Board Slots Detail

Table 2.2: Board Slot Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
A4	38.87	39.00	39.13	1.530	1.535	1.541
A5	1.65	1.80	1.95	0.065	0.071	0.077
A6	0.95	1.00	1.05	0.037	0.039	0.041
A7	3.75			0.148		
A8	6.02	6.20	6.38	0.237	0.244	0.251
A9	1.45			0.057		
A10	0.32	0.50	0.58	0.013	0.020	0.023

2.3 MXM PCB Mounting Holes

All MXM version 3.0 modules have 6 plated holes. Two are used to secure the board to the system and the other four to fasten the thermal solution to the module.

2.3.1 Board Mounting Holes

The two board mounting holes shall be 3.2 mm plated holes with 6 mm grounded pad on both the top and bottom sides of the PCB.

2.3.2 Thermal Solution Mounting

The four holes surrounding the GPU which are used for thermal attachment shall be 3.2 mm plated holes with a 6 mm grounded pad on the top side and a 7 mm grounded pad on the bottom side.

2.3.3 Backing Plate

A system shall provide a backing plate to prevent excessive board warping. The maximum allowed board warpage is measured in accordance with IPC standards (refer to IPC-A-600F). Along the connector edge this amounts to a maximum displacement of 0.615 mm. The system designer has complete

freedom on the design, as longs as it stays within the boundaries defined by the specification. Figure 2.4 shows the area that the backing plate is allowed to contact the board.

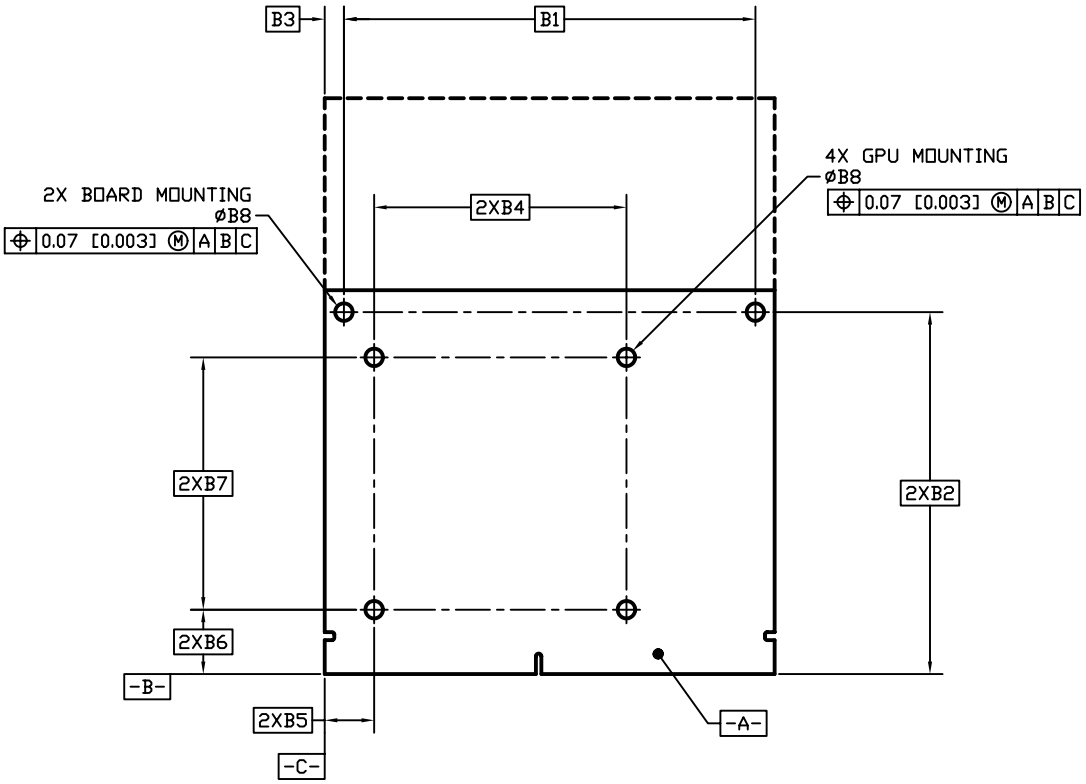


Figure 2.3: Mounting Holes (Type A and Type B)

Table 2.3: Mounting Holes Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
B1		75.00			2.953	
B2		66.00			2.598	
B3		3.50			0.138	
B4		46.00			1.811	
B5		9.00			0.354	
B6		11.75			0.463	
B7		46.00			1.811	
B8	3.07	3.20	3.33	0.121	0.126	0.131

2.4 Board Height Restrictions

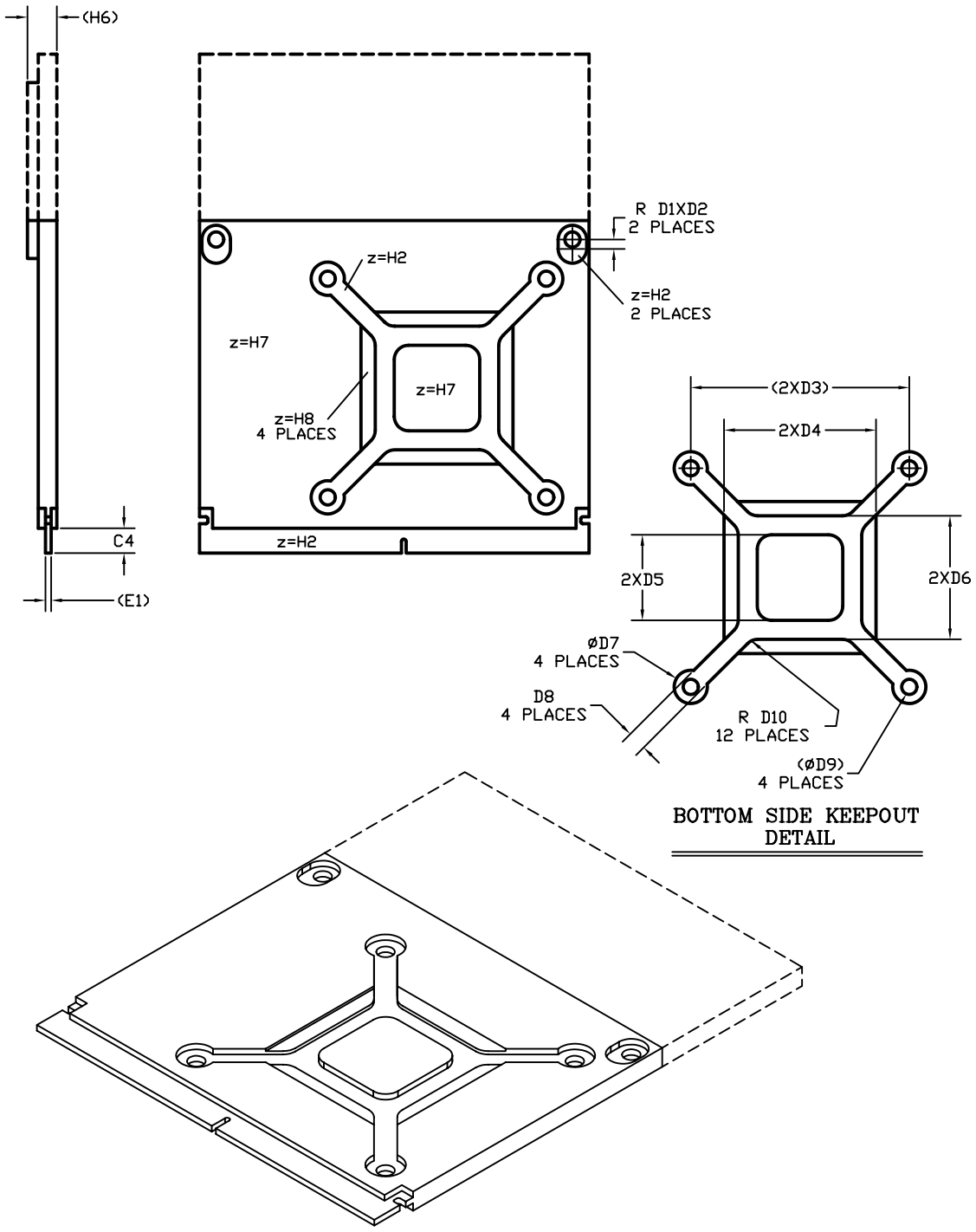


Figure 2.4: Board Bottom Side Height Restrictions (Type A and Type B)

Table 2.4: Board Bottom Side Dimensions

Symbol	[mm]			[in]		
	min	**nom**	**max**	**min**	**nom**	**max**
D1	2.87	3.00	3.13	0.113	0.118	0.123
D2	1.87	2.00	2.13	0.074	0.079	0.084
D3		46.00			1.811	
D4	31.87	32.00	32.13	1.255	1.260	1.265
D5	17.87	18.00	18.13	0.704	0.709	0.714
D6	25.87	26.00	26.13	1.019	1.024	1.029
D7	6.87	7.00	7.13	0.270	0.276	0.281
D8	3.87	4.00	4.13	0.152	0.157	0.163
D9		3.20			0.126	
D10	2.87	3.00	3.13	0.113	0.118	0.123
H2			0.00			0.000
H6			6.40			0.252
H7			1.20			0.047
H8			0.70			0.028
C4	5.12	5.25	5.38	0.202	0.207	0.212
E1		1.20			0.047	

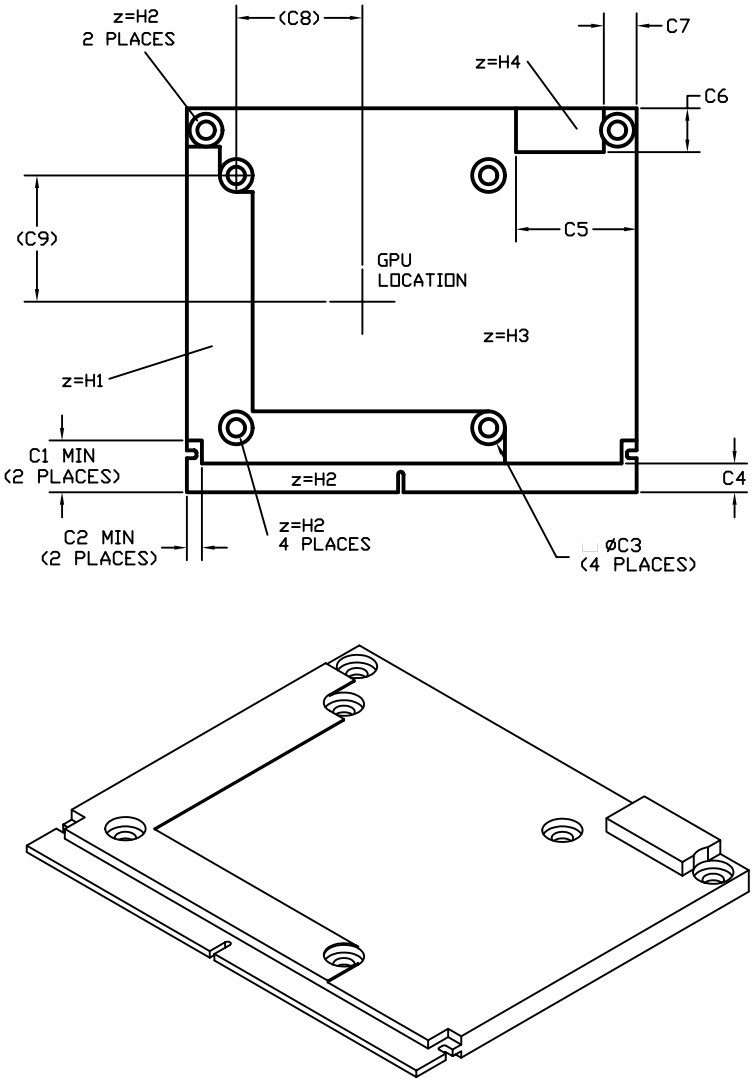


Figure 2.5: Type A Top Side Height Restrictions

Table 2.5: Type A Top Side Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
C1	9.45			0.372		
C2	2.75			0.108		
C3	5.87	6.00	6.13	0.231	0.236	0.241
C4	5.12	5.25	5.38	0.202	0.207	0.212
C5	21.87	22.00	22.13	0.861	0.866	0.871
C6	7.87	8.00	8.13	0.310	0.315	0.320
C7	5.87	6.00	6.13	0.231	0.236	0.241
C8		23.00			0.906	
C9		23.00			0.906	
H1			1.80			0.071
H2			0.00			0.000
H3			1.50			0.059
H4			4.00			0.157

Table 2.6: Type B Top Side Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
C10	24.87	25.00	25.13	0.979	0.984	0.989
C11	5.87	6.00	6.13	0.231	0.236	0.241
C12	31.87	32.00	32.13	1.255	1.260	1.265
C13	31.87	32.00	32.13	1.255	1.260	1.265
C14	5.87	6.00	6.13	0.231	0.236	0.241
C15	42.87	43.00	43.13	1.688	1.693	1.698
C16	17.87	18.00	18.13	0.704	0.709	0.714
C17	5.87	6.00	6.13	0.231	0.236	0.241
C18	21.87	22.00	22.13	0.861	0.866	0.871
H3			1.50			0.059
H4			4.00			0.157
H5			2.20			0.087

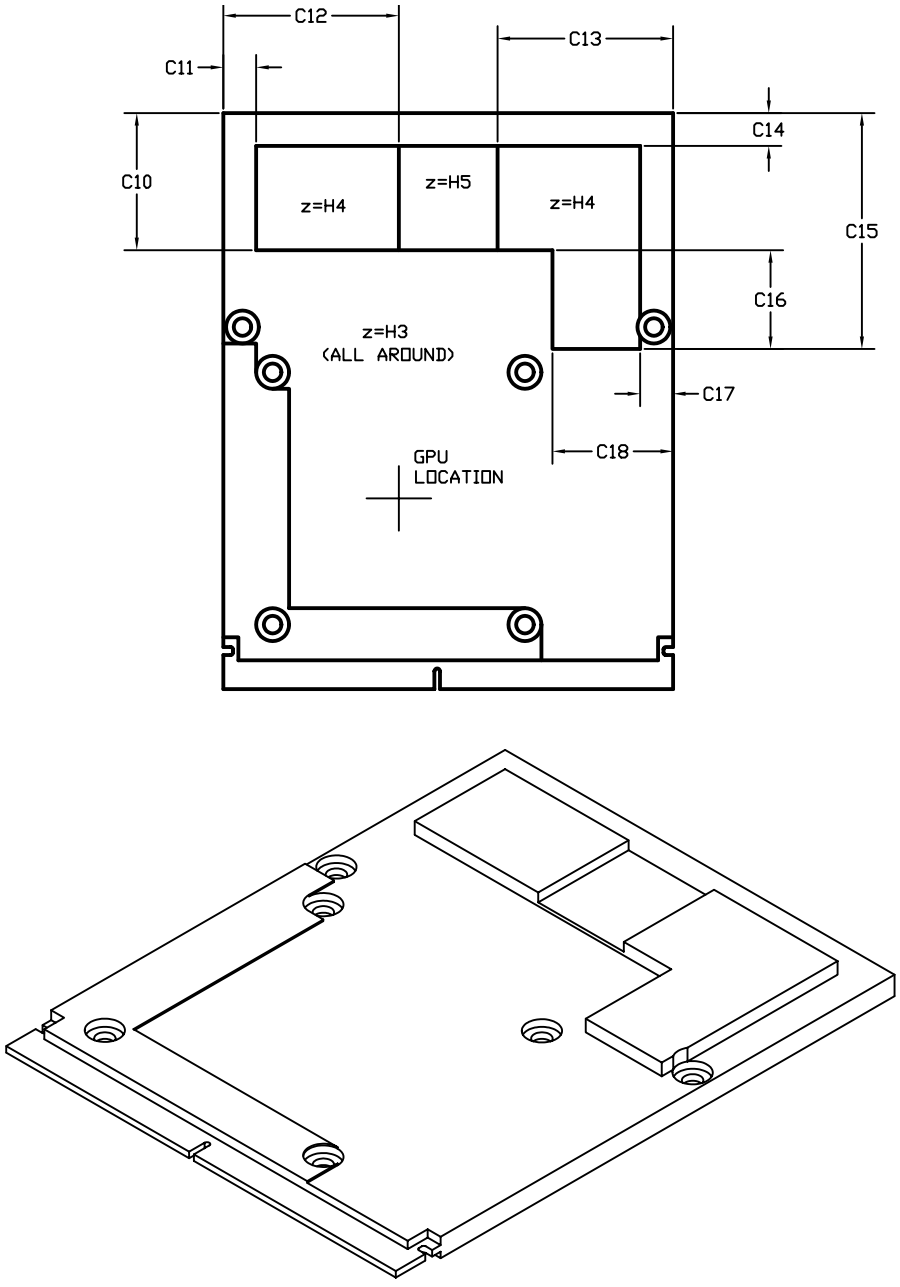


Figure 2.6: Type B Top Side Height Restrictions

2.5 MXM Edge Fingers

MXM utilizes a 0.5 mm pitch, 285-pin, card-edge connection system. Edge fingers on the module are referenced to the PCB slot center with an overall PCB thickness of 1.2±0.1 mm measured across the fingers including plating and/or metallization. Card chamfer is specified in Figure 2.7.

For good electrical performance, all etch on internal layers under the edge fingers shall be removed. A group of n adjacent power fingers are joined together to allow full pin to finger contact on n-1 pins of that particular group. The module edge finger dimensions are shown in Figure 2.8 through Figure 2.10. PCB flatness with respect to the edge fingers shall not induce undue stress nor cause an open connection between the edge fingers and the connector pin. Any surface defect, including scratches, in the edge finger contact area must not expose bare metal as described in the IPC-A-600F specification.

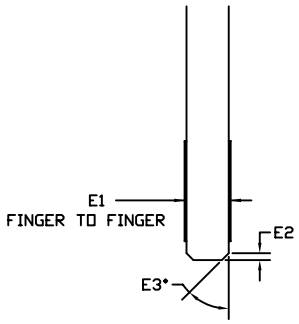


Figure 2.7: Card Thickness and Chamfer

Table 2.7: Card Thickness and Chamfer Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
E1	1.10	1.20	1.30	0.043	0.047	0.051
E2	0.06	0.18	0.30	0.002	0.007	0.012
Symbol	[degrees]			[degrees]		
	min	nom	max	min	nom	max
E3	35	45	55	35	45	55

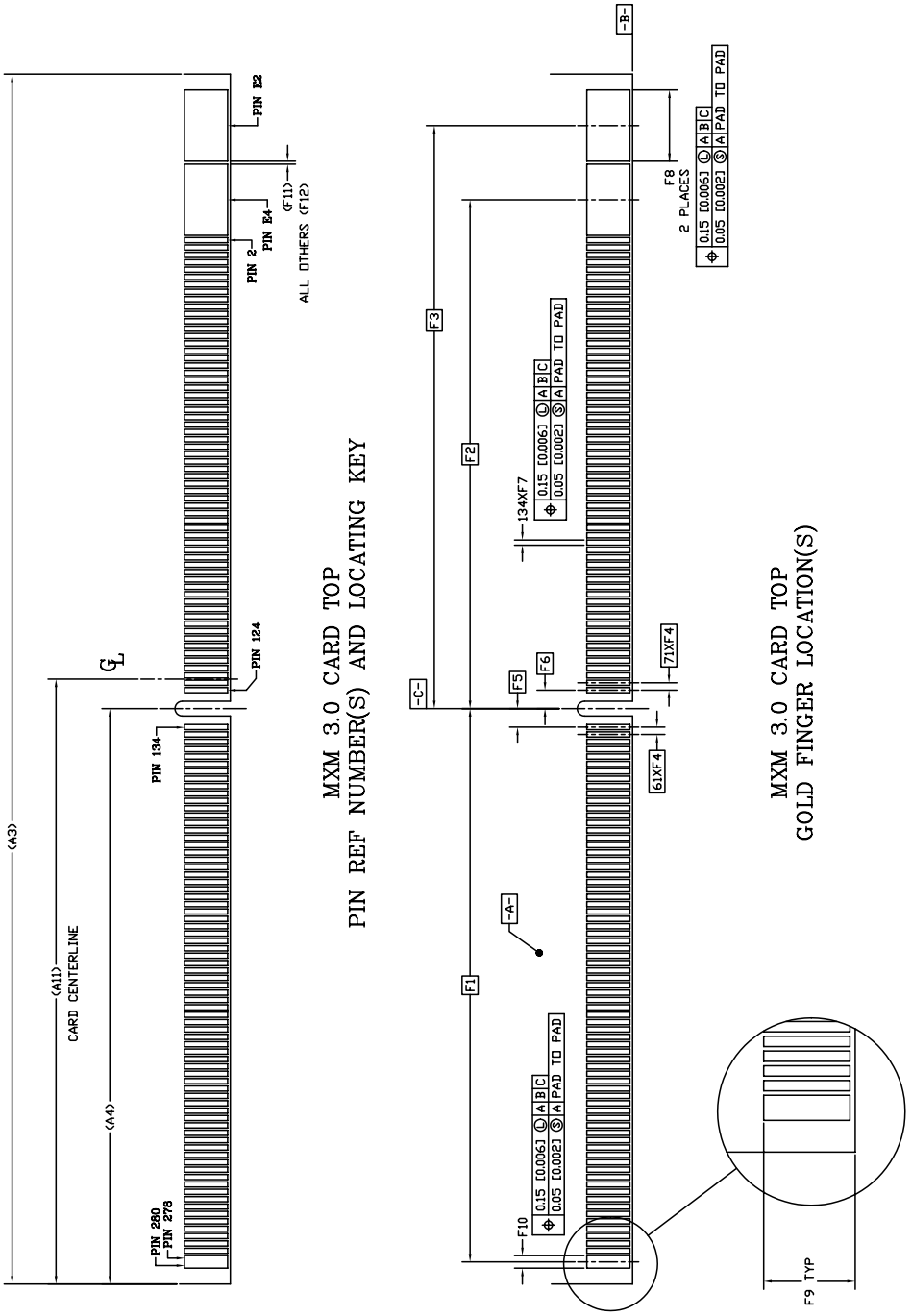


Figure 2.8: Module Edge Finger Top

Table 2.8: Module Edge Finger Top Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
A3		82.00			3.228	
A4		39.00			1.535	
A11		41.00			1.614	
F1		37.50			1.476	
F2		34.49			1.358	
F3		39.51			1.556	
F4		0.50			0.020	
F5		1.25			0.049	
F6		1.25			0.049	
F7	0.32	0.35	0.38	0.013	0.014	0.015
F8	4.79	4.82	4.85	0.189	0.190	0.191
F9	3.02	3.10	3.18	0.119	0.122	0.125
F10	0.82	0.85	0.88	0.032	0.033	0.035
F11		0.20			0.008	
F12		0.15			0.006	

Table 2.9: Module Edge Finger Bottom Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
A4		39.00			1.535	
A11		41.00			1.614	
F4		0.50			0.020	
F7	0.32	0.35	0.38	0.013	0.014	0.015
F8	4.79	4.82	4.85	0.189	0.190	0.191
F9	3.02	3.10	3.18	0.119	0.122	0.125
F11		0.20			0.008	
F12		0.15			0.006	
F13		31.00			1.220	
F14		39.76			1.565	
F15		34.74			1.368	
F16	2.32	2.35	2.38	0.091	0.093	0.094
F17	1.82	1.85	1.88	0.072	0.073	0.074
F18		28.75			1.132	
F19		1.00			0.039	
F20		1.00			0.039	

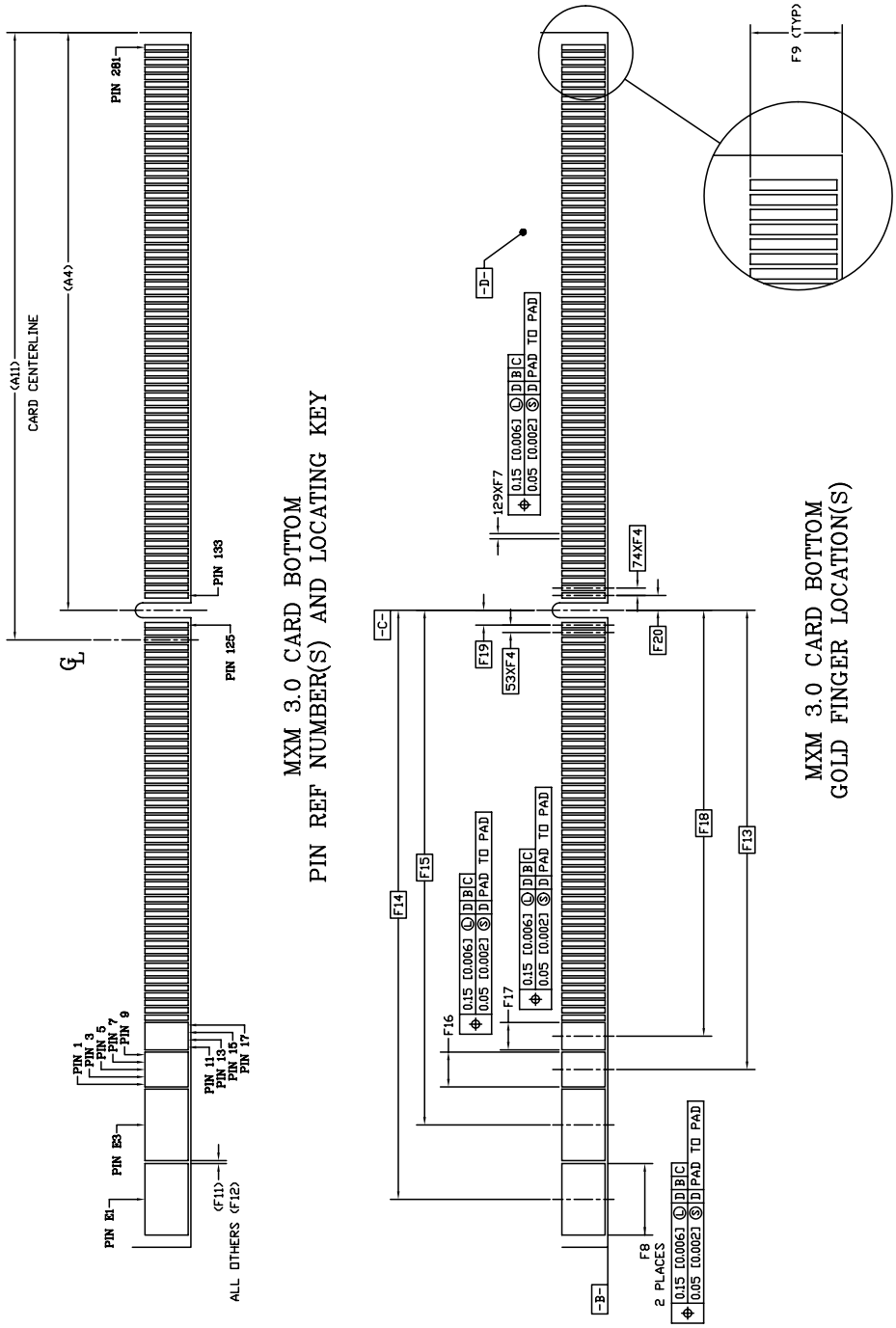


Figure 2.9: Module Edge Finger Bottom

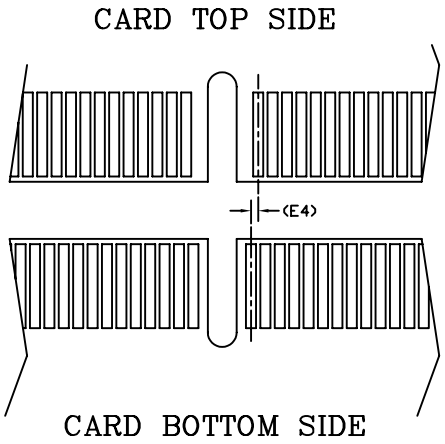


Figure 2.10: Pin Alignment Detail

Table 2.10: Pin Alignment Dimensions

Symbol	[mm]			[in]		
	min	**nom**	**max**	**min**	**nom**	**max**
E4		0.25			0.010	

2.6 MXM Connector

It is not the intention of this specification to detail connector contact and housing designs. Each connector vendor may choose to design an MXM connector of various styles as long as the design meets the form, fit and function of the MXM edge fingers and module volume definitions. This MXM specification suggests 1.5 mm, 2.7 mm and 5.0 mm connector heights (module to system board). This parameter however can be changed to satisfy custom requirements. Refer to the MXM Connector Interoperability Design Guide for details.

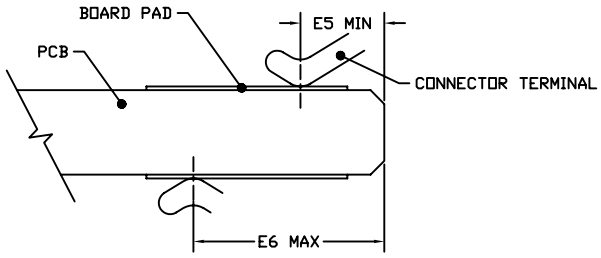


Figure 2.11: Terminal-Board Minimum Engagement

Table 2.11: Terminal-Board Minimum Engagement Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
E5	1.09		2.49	0.043		0.098
E6	1.09		2.49	0.043		0.098

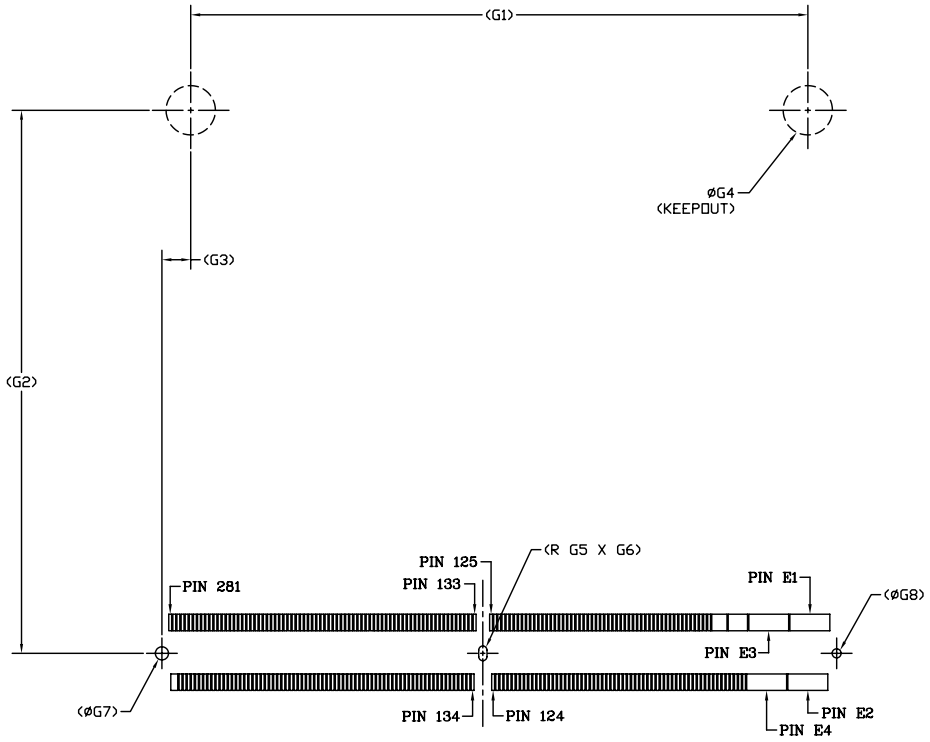


Figure 2.12: Connector Footprint

Table 2.12: Connector Footprint Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
G1		75.00			2.953	
G2		66.00			2.598	
G3		3.50			0.138	
G4	5.87	6.00	6.13	0.231	0.236	0.241
G5		0.50			0.020	
G6		1.80			0.071	
G7		1.60			0.063	
G8		1.10			0.043	

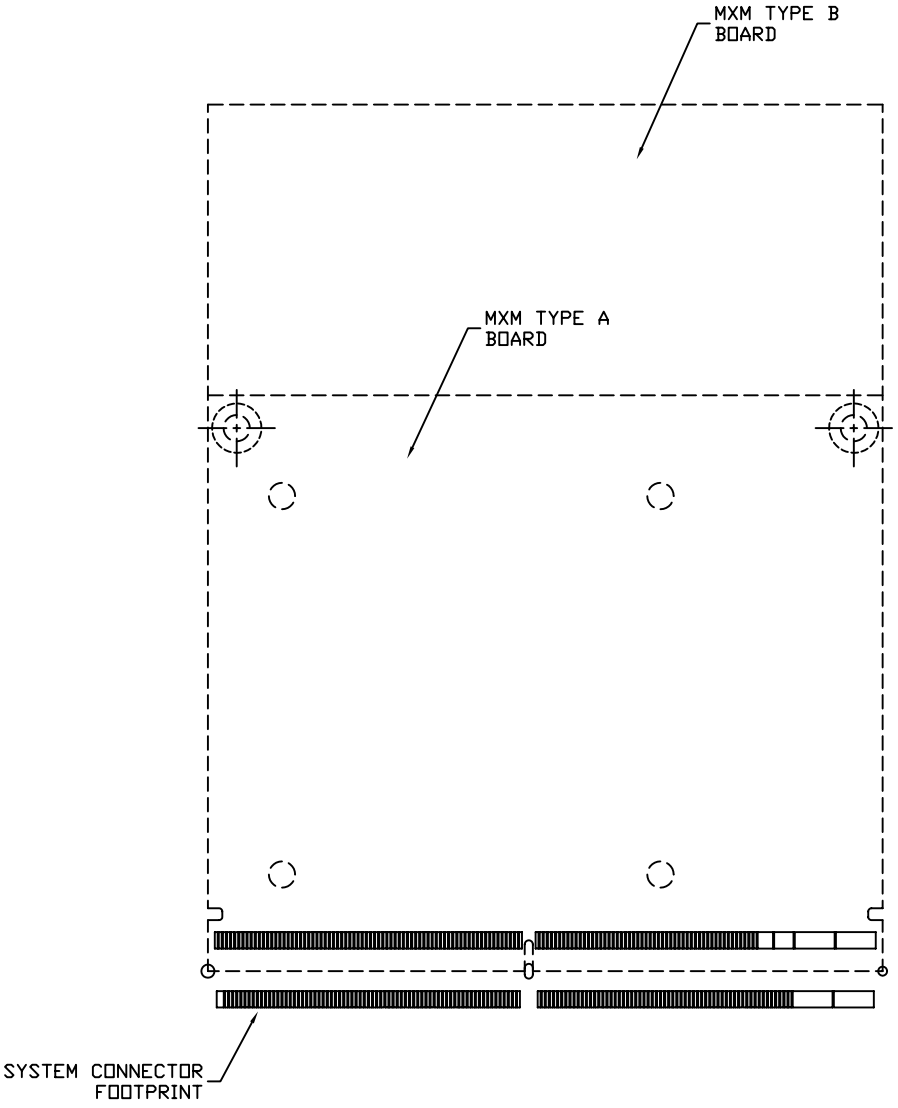


Figure 2.13: Module Location

Table 2.13: Connector Mechanical Performance Requirements

Parameter	**Specification**
Durability	EIA-364-9 30 cycles
Mating and unmating force	EIA-364-13C LIF/angled insertion styled cards: Maximum insertion force: 13 N Maximum extraction force: 16 N Slide-in/side insertion styled cards: Maximum insertion force: 59 N Maximum extraction force: 45 N Note: numbers tabulated using a velocity of 25 mm/min
Vibration	EIA-364-28D – Test condition VII condition D With a 40 x 40 mm block of 100 grams fastened and centered at the GPU center of a Type B PCB
Shock	EIA-364-27B – Test condition A With a 40 x 40 mm block of 100 grams fastened and centered at the GPU center of a Type B PCB

Chapter 3

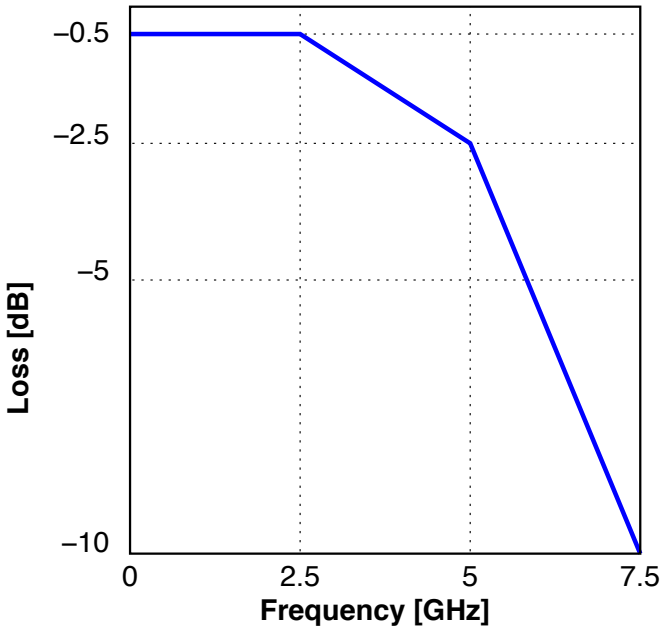
Electrical Specifications

3.1 Electrical Connector

The MXM utilizes a 285-pin card edge connection system. The top side contacts are all even numbered (E2, E4, 2, 4 etc) and the bottom side contacts are all odd numbered (E1, E3, 1, 3...). The connector accommodates a nominal card thickness of 1.2 mm. All power and I/O signals are routed through the MXM connector down to the motherboard. The motherboard should connect these signals to the appropriate circuitry depending on the required feature set. Table 3.1 lists the electrical requirements for the MXM connector.

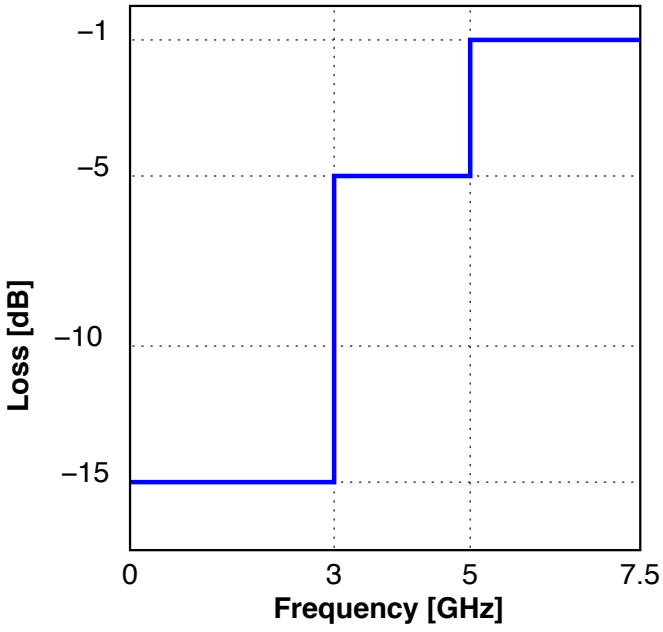
Table 3.1: MXM Connector Electrical Performance Requirements

Parameter	**Specification**
Low Level Contact Resistance	55mΩ MAX
Insulation Resistance	EIA-364-21C Initial testing 250 MΩ. 50 MΩ after other test procedures
Dielectric Withstanding Voltage	EIA-364-20B – Method B on one pair of upper adjacent contacts and on one pair of lower adjacent contacts. Connector is unmated and unmounted. Barometric pressure at sea level. Apply 0.25 KV AC, (50 Hz) for 1 minute. Current leakage 0.5mA MAX
Current Rating	0.5 A per pin MIN
Voltage Rating	50 VDC
Differential Impedance	EIA-364-108 85Ω±12.75Ω at Trise=35ps
Differential Insertion Loss	EIA-364-101 Refer to Figure 3.1
Differential Return Loss	EIA-364-108 Refer to Figure 3.2
Differential Near End Crosstalk	EIA-364-90 Refer to Figure 3.3



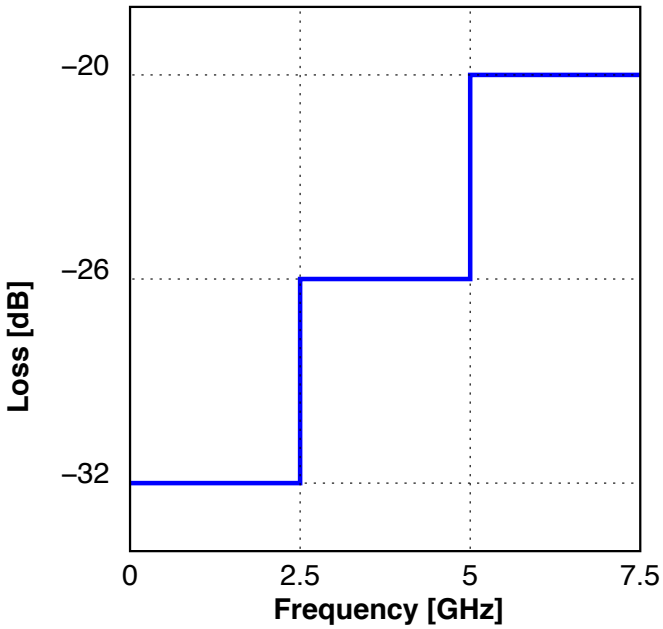
Point	f[GHz]	Loss[dB]
1	0	-0.5
2	2.5	-0.5
3	5.0	-2.5
4	7.5	-10

Figure 3.1: Connector Differential Insertion Loss



Segment	f[GHz]	Loss[dB]
1	0-3	-15
2	3-5	-5
3	5-7.5	-1

Figure 3.2: Connector Differential Return Loss



Segment	f[GHz]	Loss[dB]
1	0-2.5	-32
2	2.5-5	-25
3	5-7.5	-20

Figure 3.3: Connector Differential Near End Cross Talk

3.2 Connector Pinout

Table 3.2 and Table 3.3 list the connector pinout.

Table 3.2: Connector Pinout

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
E1	PWR_SRC	E2	PWR_SRC				
E3	GND	E4	GND				
1	5V	2	PRSNT_R#	71	GND	72	PEX_TX11#
3	5V	4	WAKE#	73	PEX_RX11#	74	PEX_TX11
5	5V	6	PWR_GOOD	75	PEX_RX11	76	GND
7	5V	8	PWR_EN	77	GND	78	PEX_TX10#
9	5V	10	RSVD	79	PEX_RX10#	80	PEX_TX10
11	GND	12	RSVD	81	PEX_RX10	82	GND
13	GND	14	RSVD	83	GND	84	PEX_TX9#
15	GND	16	RSVD	85	PEX_RX9#	86	PEX_TX9
17	GND	18	PWR_LEVEL	87	PEX_RX9	88	GND
19	PEX_STD_SW#	20	TH_OVERT#	89	GND	90	PEX_TX8#
21	VGA_DISABLE#	22	TH_ALERT#	91	PEX_RX8#	92	PEX_TX8
23	PNL_PWR_EN	24	TH_PWM	93	PEX_RX8	94	GND
25	PNL_BL_EN	26	GPIO0	95	GND	96	PEX_TX7#
27	PNL_BL_PWM	28	GPIO1	97	PEX_RX7#	98	PEX_TX7
29	HDMI_CEC	30	GPIO2	99	PEX_RX7	100	GND
31	DVI_HPD	32	SMB_DAT	101	GND	102	PEX_TX6#
33	LVDS_DDC_DAT	34	SMB_CLK	103	PEX_RX6#	104	PEX_TX6
35	LVDS_DDC_CLK	36	GND	105	PEX_RX6	106	GND
37	GND	38	OEM	107	GND	108	PEX_TX5#
39	OEM	40	OEM	109	PEX_RX5#	110	PEX_TX5
41	OEM	42	OEM	111	PEX_RX5	112	GND
43	OEM	44	OEM	113	GND	114	PEX_TX4#
45	OEM	46	GND	115	PEX_RX4#	116	PEX_TX4
47	GND	48	PEX_TX15#	117	PEX_RX4	118	GND
49	PEX_RX15#	50	PEX_TX15	119	GND	120	PEX_TX3#
51	PEX_RX15	52	GND	121	PEX_RX3#	122	PEX_TX3
53	GND	54	PEX_TX14#	123	PEX_RX3	124	GND
55	PEX_RX14#	56	PEX_TX14	125	GND	126	KEY
57	PEX_RX14	58	GND	127	KEY	128	KEY
59	GND	60	PEX_TX13#	129	KEY	130	KEY
61	PEX_RX13#	62	PEX_TX13	131	KEY	132	KEY
63	PEX_RX13	64	GND	133	GND	134	GND
65	GND	66	PEX_TX12#	135	PEX_RX2#	136	PEX_TX2#
67	PEX_RX12#	68	PEX_TX12	137	PEX_RX2	138	PEX_TX2
69	PEX_RX12	70	GND	139	GND	140	GND

Table 3.3: Connector Pinout (continued)

Pin	Signal Name	Pin	Signal Name
141	PEX_RX1#	142	PEX_TX1#
143	PEX_RX1	144	PEX_TX1
145	GND	146	GND
147	PEX_RX0#	148	PEX_TX0#
149	PEX_RX0	150	PEX_TX0
151	GND	152	GND
153	PEX_REFCLK#	154	PEX_CLK_REQ#
155	PEX_REFCLK	156	PEX_RST#
157	GND	158	VGA_DDC_DAT
159	RSVD	160	VGA_DDC_CLK
161	RSVD	162	VGA_VSYNC
163	RSVD	164	VGA_HSYNC
165	RSVD	166	GND
167	RSVD	168	VGA_RED
169	LVDS_UCLK#	170	VGA_GREEN
171	LVDS_UCLK	172	VGA_BLUE
173	GND	174	GND
175	LVDS_UTX3#	176	LVDS_LCLK#
177	LVDS_UTX3	178	LVDS_LCLK
179	GND	180	GND
181	LVDS_UTX2#	182	LVDS_LTX3#
183	LVDS_UTX2	184	LVDS_LTX3
185	GND	186	GND
187	LVDS_UTX1#	188	LVDS_LTX2#
189	LVDS_UTX1	190	LVDS_LTX2
191	GND	192	GND
193	LVDS_UTX0#	194	LVDS_LTX1#
195	LVDS_UTX0	196	LVDS_LTX1
197	GND	198	GND
199	DP_C_L0#	200	LVDS_LTX0#
201	DP_C_L0	202	LVDS_LTX0
203	GND	204	GND
205	DP_C_L1#	206	DP_D_L0#
207	DP_C_L1	208	DP_D_L0
209	GND	210	GND

Pin	Signal Name	Pin	Signal Name
211	DP_C_L2#	212	DP_D_L1#
213	DP_C_L2	214	DP_D_L1
215	GND	216	GND
217	DP_C_L3#	218	DP_D_L2#
219	DP_C_L3	220	DP_D_L2
221	GND	222	GND
223	DP_C_AUX#	224	DP_D_L3#
225	DP_C_AUX	226	DP_D_L3
227	RSVD	228	GND
229	RSVD	230	DP_D_AUX#
231	RSVD	232	DP_D_AUX
233	RSVD	234	DP_C_HPD
235	RSVD	236	DP_D_HPD
237	RSVD	238	RSVD
239	RSVD	240	RSVD
241	RSVD	242	RSVD
243	RSVD	244	GND
245	RSVD	246	DP_B_L0#
247	RSVD	248	DP_B_L0
249	RSVD	250	GND
251	GND	252	DP_B_L1#
253	DP_A_L0#	254	DP_B_L1
255	DP_A_L0	256	GND
257	GND	258	DP_B_L2#
259	DP_A_L1#	260	DP_B_L2
261	DP_A_L1	262	GND
263	GND	264	DP_B_L3#
265	DP_A_L2#	266	DP_B_L3
267	DP_A_L2	268	GND
269	GND	270	DP_B_AUX#
271	DP_A_L3#	272	DP_B_AUX
273	DP_A_L3	274	DP_B_HPD
275	GND	276	DP_A_HPD
277	DP_A_AUX#	278	3V3
279	DP_A_AUX	280	3V3
281	PRSNT_L#	-	-

3.3 Pin Description

This section contains pin descriptions for all signals divided in logical/functional groups. For each signal an input/output classification, a signal type and, when meaningful, a PCB trace impedance are provided. The input/output classification is always relative to the MXM graphics module. Table 3.4 describes all the signal types used in the next sections. Impedance is specified as single ended (SE), differential (diff) or not impedance controlled according to the type of signal.

Table 3.4: Signal Types

Type	Description
Power	Power rail
Diff	Low voltage differential signal (PCIe, LVDS, TMDS or DP)
CMOS	3.3 V push pull CMOS signal
OD	3.3 V open drain signal
Analog	Low voltage analog signal

Note: All impedance controlled signals mentioned in this chapter are assumed to have a ±10% tolerance unless specified explicitly.

3.3.1 Power Group

Table 3.5 shows the MXM module power requirements. The voltage tolerances in the table are specified as measured on the module edge finger. The system must be able to supply the full specified current on all rails (except PWR_SRC) at all times. The current capability of the PWR_SRC rail must be defined by the system in the MXM system information structure. Refer to the MXM version 3.0 Software Specification for details.

Table 3.5: MXM Power Rails

Signal Name	I/O	Type	Impedance	Voltage	Current
PWR_SRC	I	Power	N/A	7-20 V	up to 10 A
5V	I	Power	N/A	5.0 V ±6%	2.5 A
3V3	I	Power	N/A	3.3 V ±6%	1.0 A

Note: PWR_SRC voltage range is assumed to be DC or RMS. However under any circumstances the maximum peak voltage shall not exceed 22 V and the minimum voltage shall not fall below 6.5 V.

3.3.2 PCI Express Signal Group

The MXM version 3.0 supports PCI Express interconnect up to sixteen lanes. It is compliant with PCI Express Base Specification 2.0 or earlier except for power delivery and power management. MXM power requirements supersede PCI Express power specifications. Table 3.6 shows the list of signals for the PCIe group.

Table 3.6: Connector Pin Description (PCIe group)

Signal Name	I/O	Type	Impedance	Description
PEX_TXxx PEX_TXxx#	I	Diff	90Ω diff	PCI Express output from the Root Complex. DC blocking caps must be placed on the system board.
PEX_RXxx PEX_RXxx#	O	Diff	90Ω diff	PCI Express input to the Root Complex. DC blocking caps must be placed on the system board.
PEX_REFCLK PEX_REFCLK#	I	Diff	90Ω diff	PCI Express reference clock.
PEX_RST#	I	CMOS	N/A	PCI Express reset signal.
PEX_CLK_REQ#	O	OD	N/A	PCI Express clock request. Pull-up resistor to 3.3 V is required on the system board if the function is supported.
PEX_STD_SW#	I	OD	N/A	PCI Express swing select pin. Module will default in low swing mode if the pin is no connect on the system board. Must be tied to GND to select standard (desktop) swing level.

3.3.3 DisplayPort Signal Group

The DisplayPort signal group provides the interface for connecting up to four digital displays. Compliant modules are required to support at least port A and port C. Support for the other ports is optional.

Table 3.7: Connector Pin Description (DP group)

Signal Name	I/O	Type	Impedance	Description
DP_A_Lx DP_A_Lx#	O	Diff	90Ω diff	Dual-mode DisplayPort A. DC blocking caps must be placed on the system board.
DP_A_AUX DP_A_AUX#	I/O	Diff / OD	90Ω diff	DisplayPort A auxiliary channel/DDC. DC blocking caps must be placed on the system board. Refer to Section 3.4.5 for Dual-mode support.
DP_A_HPD	I	CMOS	N/A	DisplayPort A hot plug detect. 100KΩ pull-down required on module. Protection circuitry must be placed on the system board.
DP_B_Lx DP_B_Lx#	O	Diff	90Ω diff	DisplayPort B. DC blocking caps must be placed on the system board. Dual-mode support is optional.
DP_B_AUX DP_B_AUX#	I/O	Diff / OD	90Ω diff	DisplayPort B auxiliary channel/optional DDC. DC blocking caps must be placed on the system board.
DP_B_HPD	I	CMOS	N/A	DisplayPort B hot plug detect. 100KΩ pull-down required on module. Protection circuitry must be placed on the system board.
DP_C_Lx DP_C_Lx#	O	Diff	90Ω diff	Dual-mode DisplayPort C. DC blocking caps must be placed on the system board.
DP_C_AUX DP_C_AUX#	I/O	Diff / OD	90Ω diff	DisplayPort C auxiliary channel/DDC. DC blocking caps must be placed on the system board. Refer to Section 3.4.5 for Dual-mode support.
DP_C_HPD	I	CMOS	N/A	DisplayPort C hot plug detect. 100KΩ pull-down required on module. Protection circuitry must be placed on the system board.
DP_D_Lx DP_D_Lx#	O	Diff	90Ω diff	DisplayPort D. DC blocking caps must be placed on the system board. Dual-mode support is optional.
DP_D_AUX DP_D_AUX#	I/O	Diff / OD	90Ω diff	DisplayPort D auxiliary channel/optional DDC. DC blocking caps must be placed on the system board.
DP_D_HPD	I	CMOS	N/A	DisplayPort D hot plug detect. 100KΩ pull-down required on module. Protection circuitry must be placed on the system board.

3.3.4 LVDS Signal Group

The LVDS signal group provides the interface for connecting one legacy digital display (LVDS, DVI or HDMI). Support for 18-bit/24-bit dual-link LVDS is required. HDMI and dual-link DVI support is optional.

Table 3.8: Connector Pin Description (LVDS Group)

Signal Name	I/O	Type	Impedance	Description
LVDS_LTXx LVDS_LTXx#	O	Diff	90Ω diff	LVDS/DVI/HDMI output for single and dual-link displays (lower/odd link)
LVDS_LCLK LVDS_LCLK#	O	Diff	90Ω diff	LVDS/DVI/HDMI clock output for single and dual-link displays (lower/odd link)
LVDS_UTXx LVDS_UTXx#	O	Diff	90Ω diff	LVDS/DVI output for dual-link displays (upper/even link)
LVDS_UCLK LVDS_UCLK#	O	Diff	90Ω diff	LVDS clock output for dual-link displays (upper/even link)
DVI_HPD	I	CMOS	N/A	Hot plug detect dedicated for the LVDS/DVI/HDMI port. 100KΩ pull-down required on module. Protection circuitry must be placed on the system board.
LVDS_DDC_CLK	O	OD	N/A	DDC clock for the LVDS/DVI/HDMI port. 4.7KΩ pull-up to 3.3 V required on module. The MXM serial ROM, if present, must be on this bus. System board must provide a parallel equivalent of 4.3KΩ (±10%). Refer to the MXM system design guide for details.
LVDS_DDC_DAT	I/O	OD	N/A	DDC data for the LVDS/DVI/HDMI port. 4.7KΩ pull-up to 3.3 V required on module. The MXM serial ROM, if present, must be on this bus. System board must provide a parallel equivalent of 4.3KΩ (±10%). Refer to the MXM system design guide for details.

3.3.5 Analog Display Signal Group

The analog display signal group provides the interface for connecting one legacy analog display (CRT/TV). Support for standard CRT is required. Composite, S-Video and Component TV-Out support is optional.

Table 3.9: Connector Pin Description (Analog Display Group)

Signal Name	I/O	Type	Impedance	Description
VGA_RED	O	Analog	50Ω SE	Analog VGA red channel. Multiplexed with S-video chroma (C) or HDTV Pr if TV is supported.
VGA_GREEN	O	Analog	50Ω SE	Analog VGA green channel. Multiplexed with S-video luma (Y) or HDTV Y if TV is supported.
VGA_BLUE	O	Analog	50Ω SE	Analog VGA blue channel. Multiplexed with composite (CVBS) or HDTV Pb if TV is supported.
VGA_VSYNC	O	CMOS	50Ω SE	Analog VGA vertical sync signal. Level shifters on the system board should be used if 5V signaling is desired.
VGA_HSYNC	O	CMOS	50Ω SE	Analog VGA horizontal sync signal. Level shifters on the system board should be used if 5V signaling is desired.
VGA_DDC_CLK	O	OD	N/A	DDC clock for the VGA port. 4.7KΩ pull-up to 3.3 V required on module. System board must provide a parallel equivalent of 4.3KΩ. Refer to the MXM system design guide for details.
VGA_DDC_DAT	I/O	OD	N/A	DDC data for the VGA port. 4.7KΩ pull-up to 3.3 V required on module. System board must provide a parallel equivalent of 4.3KΩ. Refer to the MXM system design guide for details.

3.3.6 Power and Thermal Management Signal Group

Table 3.10: Connector Pin Description (Power and Thermal Management Group)

Signal Name	I/O	Type	Impedance	Description
SMB_CLK	I	OD	N/A	SMBus clock. Pull-up resistor to 3.3 V of appropriate value is required on the system board. Weak 100KΩ pull-up to 3.3 V recommended on module. Refer to Section 3.4.10 for details.
SMB_DAT	I/O	OD	N/A	SMBus data. Pull-up resistor to 3.3 V of appropriate value is required on the system board. Weak 100KΩ pull-up to 3.3 V recommended on module. Refer to Section 3.4.10 for details.
TH_OVERT#	O	OD	N/A	Thermal shutdown request. System must power down the MXM module within 500ms to prevent permanent damage. Pull-up resistor to 3.3 V of appropriate value is required on the system board. Weak 100KΩ pull-up to 3.3 V recommended on module. Refer to Section 3.4.11 for details.
TH_ALERT#	I/O	OD	N/A	Thermal interrupt request. Signal may be used by the system to signal to module to reduce power consumption. The signal may also be used by the module to signal to the system a non critical temperature alert. Pull-up resistor to 3.3 V of appropriate value is required on the system board. Weak 100KΩ pull-up to 3.3 V required on module. Refer to Section 3.4.11 for details.
TH_PWM	O	CMOS	N/A	Thermal PWM. This signal may be used to control a fan connected to the module thermal solution. Refer to Section 3.4.11 for details.
PWR_LEVEL	I	OD	N/A	Signals the module to switch to a lower power state. Modules must reduce the power by at least 20% within 50ms. Weak 100KΩ pull-up to 3.3 V required on module. Power levels may be configured using software. Refer to Section 3.4.12 for details.
PWR_EN	I	CMOS	N/A	Module power enable. System must assert this signal to power on the module. May be asserted only after all input rails are within the specified tolerance. Refer to Section 3.4.1 for timing details.
PWR_GOOD	O	OD	N/A	Power sequencing sideband. The module will assert this signal when all its internal power regulators are within the required tolerance. 10KΩ pull-up required on the system board if the feature is used.

3.3.7 System Management Signal Group

Sideband signals to control an internal panel are also included in this group. The sideband signals may be used in conjunction with any digital display interface (including DisplayPort from the DP group).

Table 3.11: Connector Pin Description (System Management Group)

Signal Name	I/O	Type	Impedance	Description
PNL_PWR_EN	O	CMOS	N/A	Internal panel power enable. Refer to Section 3.4.13 for detailed timing requirements.
PNL_BL_EN	O	CMOS	N/A	Internal panel backlight enable.
PNL_BL_PWM	O	CMOS	N/A	Internal panel PWM brightness control.
GPIOx	I/O	CMOS	N/A	Generic GPIO pins. May be configured using the MXM software. Refer to the MXM Software Specification for details.
HDMI_CEC	I/O	OD	N/A	HDMI 1-wire CEC bus. Pull-up resistor to 3.3 V of appropriate value is required on the system board (if supported). Weak 100KΩ pull-up to 3.3 V recommended on module.
VGA_DISABLE#	I	OD	N/A	GPU PCI class code select pin. Used for multi GPU configurations. Available values are VGA (default) for a primary display adapter or 3D Accelerator (tie to GND) for a secondary adaptor. Refer to Section 3.4.14 for details.
WAKE#	O	OD	N/A	System wake signal. The module may assert this signal to force the system to resume from suspend (ACPI G1-S1, S2, S3, S4) or from soft-off (ACPI G2-S5). If the function is supported pull-up resistor to 3.3 V is required on the system board. Refer to Section 3.4.15 for details.
PRSNT_R# PRSNT_L#	O	OD	N/A	MXM module present detect. Weak pull-up required on system if module detection is desired. Module must connect to ground.
OEM (8 pins)	I/O	N/A	N/A	OEM reserved pins. System may connect these pins to extend the MXM functionality or to obtain cost reductions. Compliant MXM modules must not connect to any of the OEM pins. Refer to Section 3.4.16 for details.
RSVD (24 pins)	I/O	N/A	N/A	Reserved pins for future use. System must not connect any of these pins to ensure compatibility with future MXM versions. MXM version 3.0 modules must not connect to these pins.

3.4 System Requirements

This section describes the system requirements necessary to support MXM version 3.0 modules.

Note: In all timing diagrams signals should be considered unstable/unknown in gray shaded areas.

3.4.1 Power Sequencing

There is no power sequencing requirement for the input voltages to the MXM module. However the PWR_EN signal may be asserted only after all power rails are within specified tolerance. The state of PWR_GOOD is undefined until all rails are fully ramped. Refer to Figure 3.4 for details.

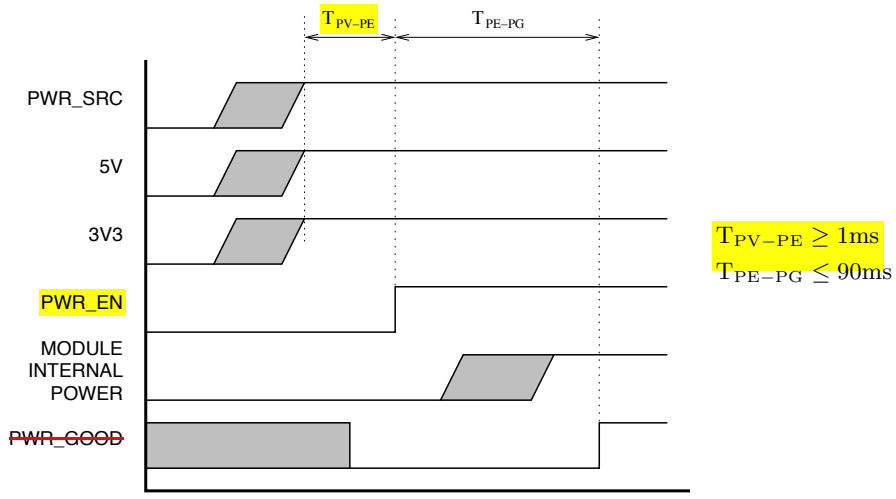


Figure 3.4: Power Sequencing

Note: No voltage shall be applied to any MXM module signal pin (except power pins and open drain signals specified in Table 3.12) until PWR_GOOD is asserted.

Table 3.12: Signals Exempted from Gating Requirement

Group	Signals
Power and Thermal	SMB_CLK, SMB_DAT TH_OVER#, TH_ALERT# PWR_GOOD
System Management	WAKE#, PEX_CLK_REQ#
Display	DP_x_HDP, DVI_HDP

3.4.2 Module Power Down and Power Up

The MXM module may be powered down using the PWR_EN signal. The system designer may choose to shut down or keep the input power while the module is powered down. Refer to Figure 3.5 for details.

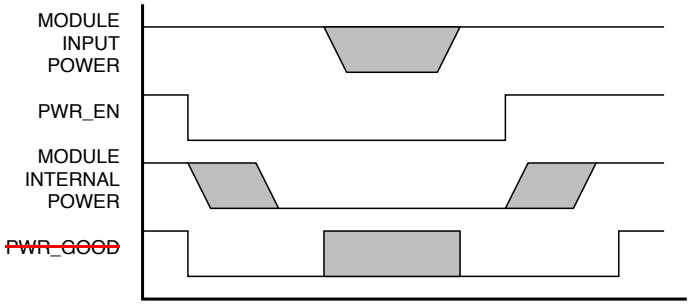


Figure 3.5: Module Power Down

Note: All output signals from the MXM module are undefined when PWR_GOOD is deasserted or undefined. The system is reccomended to gate critical signals using an appropriate qualifier.

3.4.3 Reset Requirements

System reset may be deasserted only after the assertion of the PWR_GOOD signal. Figure 3.6 shows the reset requirements relative to the PWR_EN and PWR_GOOD signals. This sequence must be followed on initial power on, system reset and resume from suspend/hibernate.

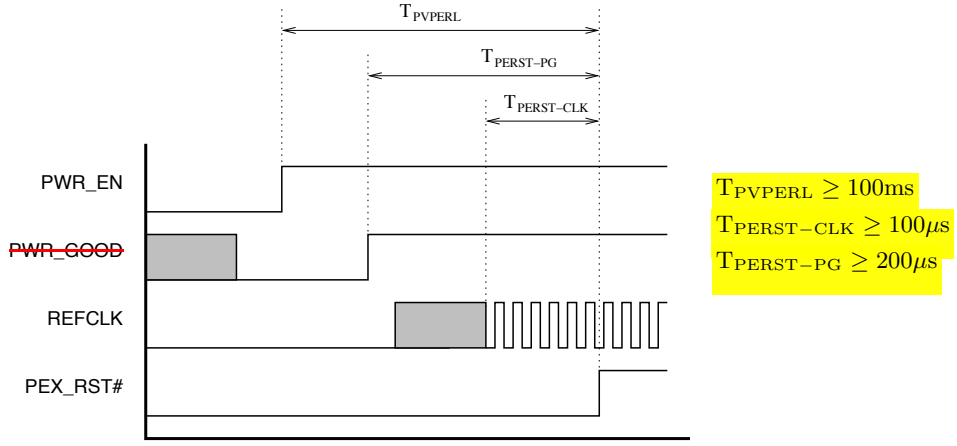


Figure 3.6: Reset Sequencing

Note: In order to reduce boot time, a system that monitors the PWR_GOOD signal, is allowed to violate the T_{PVPERL} specification as long as the $T_{PERST-PG}$ timing is still met.

3.4.4 PCI Express Interface

PCIe traces must be routed with the impedance specified by Table 3.6. DC blocking capacitors for both TX and RX lines must be placed on the system board. Refer to the PCI Express Specification for specific capacitors requirements.

3.4.5 DisplayPort Interface

DisplayPort traces must be routed with the impedance specified by Table 3.7. DC blocking capacitors must be placed on the system board. In addition the MXM implementation of Dual-mode DisplayPort requires the circuit in Figure 3.7 on the AUX lines for proper dongle detection. The HPD signal conditioning must also be placed on the system board.

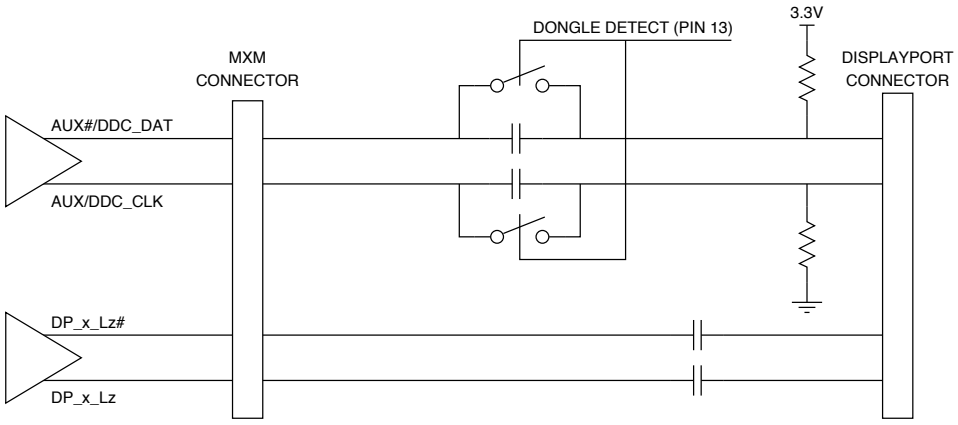


Figure 3.7: Dual-mode DisplayPort Implementation

3.4.6 DVI/HDMI on DP Interface

Native DVI or HDMI connector support can be implemented using a display port interface. Additional circuitry is required on the system and the proper signal mapping must be observed. As Figure 3.8 shows, 499Ω 1% pull-down resistors to ground on the DP lane signals must be placed on the connector side of the AC coupling capacitors gated by a FET to limit the leakage. Additionally level shifting circuits must also be implemented on DDC Data and CLK, refer to the MXM version 3.0 System Design Guide for specific details.

Table 3.13 shows the mapping to connect the signals from the MXM connector to the HDMI/DVI connector.

Table 3.13: DisplayPort Multiplexed Signal Definition

DisplayPort	DVI/HDMI
DP_x_L0 DP_x_L0#	TX_x_D2 TX_x_D2#
DP_x_L1 DP_x_L1#	TX_x_D1 TX_x_D1#
DP_x_L2 DP_x_L2#	TX_x_D0 TX_x_D0#
DP_x_L3 DP_x_L3#	TX_x_CLK TX_x_CLK#
DP_x_AUX	DDC_x_CLK
DP_x_AUX#	DDC_x_DATA

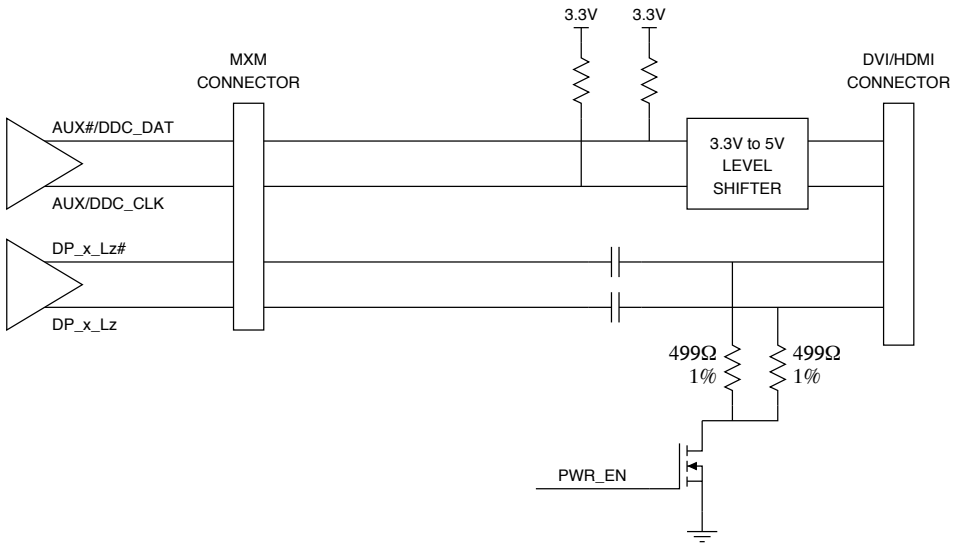


Figure 3.8: DVI/HDMI Implementation using DP Interface

3.4.7 DVI/HDMI on LVDS Interface

The MXM module can optionally provide DVI/HDMI output through the LVDS signal port. The signal mapping for this multifunctional port is defined in Table 3.14.

Table 3.14: LVDS Multi Function Signal Definition

Pin Name	HDMI	Dual-link DVI
LVDS_LTX0 LVDS_LTX0#	TX_D0 TX_D0#	TX_D0 TX_D0#
LVDS_LTX1 LVDS_LTX1#	TX_D1 TX_D1#	TX_D1 TX_D1#
LVDS_LTX2 LVDS_LTX2#	TX_D2 TX_D2#	TX_D2 TX_D2#
LVDS_LTX3 LVDS_LTX3#	N/A	N/A
LVDS_LCLK LVDS_LCLK#	TX_CLK TX_CLK#	TX_CLK TX_CLK#
LVDS_UTX0 LVDS_UTX0#	N/A	TX_D3 TX_D3#
LVDS_UTX1 LVDS_UTX1#	N/A	TX_D4 TX_D4#
LVDS_UTX2 LVDS_UTX2#	N/A	TX_D5 TX_D5#
LVDS_UTX3 LVDS_UTX3#	N/A	N/A
LVDS_UCLK LVDS_UCLK#	N/A	N/A

3.4.8 VGA Interface

The system motherboard should route all VGA signals (R, G, B, and Sync) with 50Ω impedance. A 150Ω termination resistor to ground should be placed at the end of the trace as close as possible to the output filters as depicted in Figure 3.9.

The MXM module must route all VGA signals with 50Ω impedance as well and place a 150Ω termination resistor to ground as close as possible to the signal driver as shown in Figure 3.9.

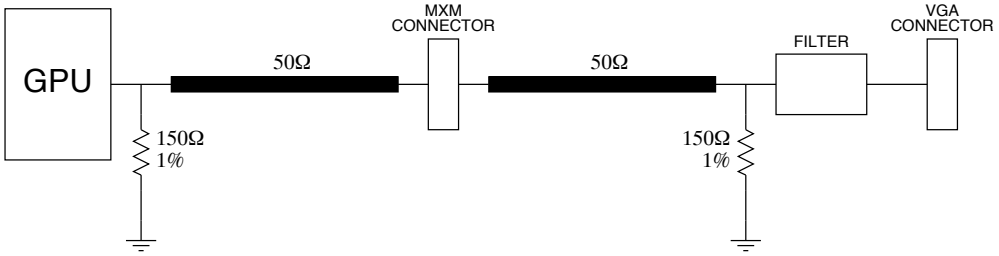


Figure 3.9: VGA Implementation

3.4.9 TV Out Implementation

The VGA and TV signals share the same pins at the MXM connector. Therefore, a demultiplexer is needed on the motherboard if the system supports both VGA and TV out. Refer to Figure 3.10 for a simplified schematics.

The motherboard should route all signals with 50Ω impedance. A 150Ω termination resistor to ground should be placed at the end of the trace before the demultiplexer as shown in Figure 3.10.

The MXM module should route the VGA and TV signals with 50Ω impedance and place a 150Ω termination resistor to ground as close as possible to the signal driver as shown in Figure 3.10.

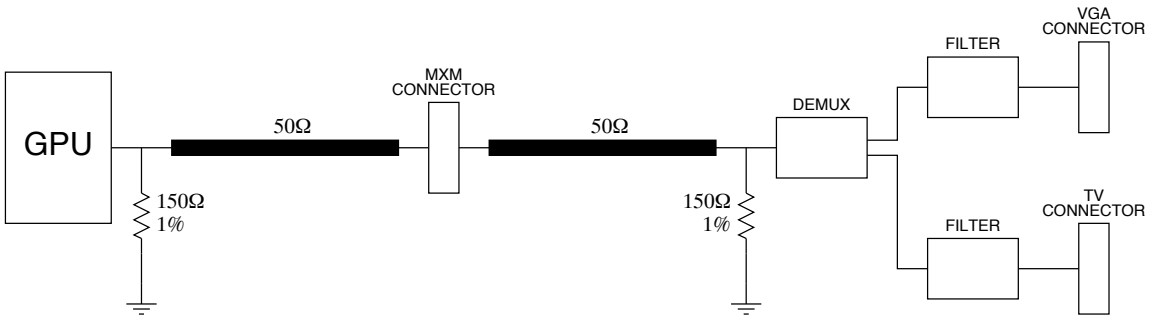


Figure 3.10: TV Implementation

3.4.10 SMBus interface

The MXM version 3.0 module shall connect a thermal sensor, compatible to the MAX6649 or LM99, to the SMBus for reading the GPU die temperature. The system must be able to access the GPU die temperature at any of the four possible SMBus addresses 0x98, 0x9E, 0x56, or 0x32. The module must respont to at least one of the addresses but may at the designer option respond to multiple or all of them. The SMBus address shown here is the 8-bit address, where the 7 most significant bits are the address and the least significant bit is the read/write bit.

Table 3.15: Module SMBus Address

SMBus Address	7-bit Address	Write Address	Read Address
0x98	1001100	0x98	0x99
0x9E	1001111	0x9E	0x9F
0x56	0101011	0x56	0x57
0x32	0011001	0x32	0x33

Note: No SMBus system devices are allowed to respond to the MXM reserved addresses. Separate SMBus buses or isolation circuitry is required to avoid conflicts.

3.4.11 Thermal and Power Management Interface

The thermal and power management interface of the MXM module consists of 3 main control signals, in addition to the SMBus interface used to read temperature and control various inputs to the temperature and power management interface.

The 3 control signals can be described as system thermal and power protection (TH_OVERT#) and thermal and power system optimization (TH_ALERT# and TH_PWM).

TH_OVERT# is a required open drain output from the MXM module which alerts the system that a critical temperate threshold has been crossed and the system must be shut down with 500 ms in order to prevent physical damage. The temperature threshold is defined as the minimum value of the module and the system limits (refer to the MXM version 3.0 Software Specification for details). This feature is a failsafe and should not occur during normal operation.

TH_ALERT# is an optional open drain input/output of the MXM module. On the MXM module side, the module will assert this signal to notify the system that its ALERT temperature has been crossed and it is taking steps to reduce the temperature and power of the module. On the system side, if the system determines the MXM module is operating in a temperature and power range it should not be, the system can assert the TH_ALERT# input to invoke the same temperature reduction mechanism to lower the temperature and power of the module.

TH_PWM is an optional output of the MXM module which can be used to control a fan to optimize the MXM module performance and acoustic characteristics. The PWM frequency must be programmable between 10 and 30,000Hz with duty cycle steps of no more than 1%. Refer to the MXM Version 3.0 Software Specification for details.

3.4.12 PWR_LEVEL Signal

The purpose of this pin is to give the system a hardware method for signaling the module to reduce power consumption. The logic states are defined as 1 for full power and 0 for reduced power. These two states may correspond to two power levels defined in the MXM System Information Structure (input power substructure). Refer to the MXM version 3.0 Graphics Module Software Specification for more information on this substructure. Alternatively the module implementer may choose to associate the pin states with other methods of power reduction. In any case the support of this feature is required for the module and must provide at least 20% power reduction from full power to reduced power. The use of this feature is optional for the system (may be left unconnected).

When PWR_LEVEL transitions from 1 to 0, the module must reduce power consumption within 50ms. In transitions from 0 to 1 the module shall return to the full power state within 250ms.

The system should determine the values of the two power levels in the structure based on the considerations of the maximum allowable current (10A) through the PWR_SRC rail limited by the capability of the MXM connector, and the maximum allowable current of the battery. The system should drive PWR_LEVEL low whenever a condition occurs that may cause the current through PWR_SRC to exceed 10A, or the total current drawn from the battery to exceed its limit. An example would be that the AC adapter is inadvertently unplugged and the battery is running at a lower voltage. In this case, the module, maintaining its higher power level, may draw a current greater than 10A and damage the connector. Another example is a system that contains more than one MXM module and operates at full power of each module. When the AC adapter is unplugged in this case, the individual module may not draw current more than 10A but the total current drawn from the battery may exceed its limit. If the modules do not transition from high to low power in time, the battery may be damaged.

3.4.13 Internal Flat Panel Interface

The flat panel sideband signals may be used for any type of internal panel (LVDS/TMDS/DP). Modules must meet the timing specification detailed in Figure 3.11.

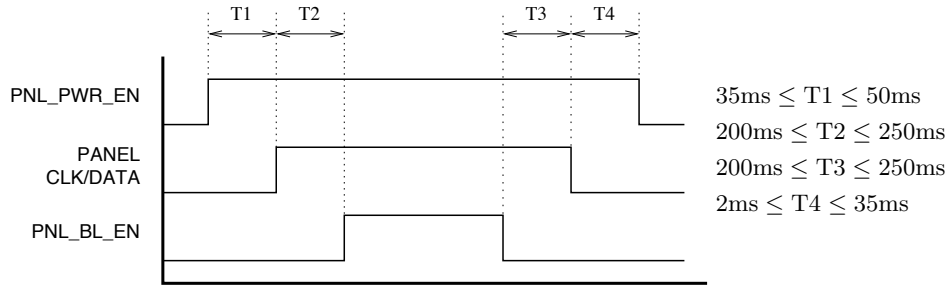


Figure 3.11: Internal Flat Panel Timing

3.4.14 VGA_DISABLE# Signal

This signal may be used in a system containing more than one graphics controller. The support of this feature is optional for both the system and the module.

In a system that contains more than one graphics controller, the system may choose to use the MXM module as a 3D accelerator only and not to use it as a boot display device. In that case, the system can disable the MXM module as a primary display controller by tying this signal to ground. The MXM module will configure itself as a PCI display device with subclass being "VGA-compatible controller" or "3D controller" depending on the logic state of this signal.

3.4.15 WAKE Functionality

The WAKE# pin is an open drain output which has been provided as a mechanism for the MXM module to wake the system from a suspend or soft-off state. To initiate and complete a WAKE event, the module must assert WAKE# and then wait for PEX_RST# to deassert which will signal the end of the electrical portion of the WAKE event. As an example, this feature can be used in conjunction with the HDMI CEC feature to wake the system on CEC events received by the MXM module while the system is in one of the suspend states or soft-off states. Another example use of this feature would be to have one of the HPD (hot plug detect) events wake the system from a suspend or soft off state when a display is connected to the MXM module.

3.4.16 OEM Modules

In the MXM version 3.0 connector interface, eight pins have been allocated for OEM customization of system features. An MXM version 3.0 compliant system can use these pins for any functions it defines. It achieves these functions by using an OEM customized module. This OEM module is not MXM version 3.0 compliant and can not be used in any other systems and be guaranteed to function correctly. On the other hand, any MXM version 3.0 compliant module will work correctly in any MXM version 3.0 compliant system even if the system uses OEM pins. This is achieved by requiring any MXM version 3.0 compliant module not to connect to any of the OEM pins.

3.5 Signal Integrity

The MXM specification, to ensure module interoperability, defines requirements for both the module and the system interconnect.

For graphics modules, the MXM signal integrity specification is based on the published specifications of each interface. Eye diagram requirements are redefined to account for the different configuration.

For system boards, the MXM signal integrity specification is based on the total interconnect performance including the MXM connector, PCB traces, and any other connector. Insertion and return loss budgets in the form of S-parameter masks are provided for each interface. The use of S-parameters masks allows the designer to determine the best tradeoffs based on the system requirements.

MXM specific test boards are required for both module and system validation. Section 3.5.1 describes the requirements for the module and Section 3.5.2 describes the requirements for the system. Subsequent sections describe the details for each interface.

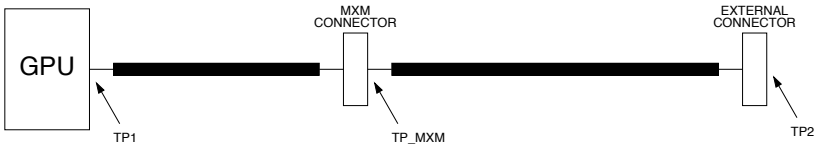


Figure 3.12: MXM Module and System

3.5.1 Module Specification

The compliance measurements for all interfaces must be taken at test point TP_MXM. TP_MXM is defined as the SMP connector on the Compliance Base Board (CBB). Refer to Figure 3.13 for a simplified diagram of the validation setup and Table 3.16 for the CBB specifications.

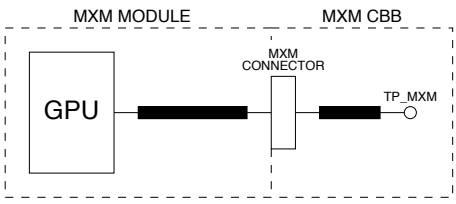


Figure 3.13: Module Validation Test Setup

Table 3.16: TP_MXM CBB Specification

Interface	Impedance	Trace Length	Spacing	AC CAP	Termination	Connector
DP	100Ω diff	50 mm ±1	4X	0.1μF	50Ω PD	SMP
TMDS	100Ω diff	50 mm ±1	4X	N/A	50Ω PU	SMP
LVDS	100Ω diff	50 mm ±1	4X	N/A	100Ω Diff	SMP
PCIe	85Ω diff	75 mm ±1	4X	0.1μF	50Ω PD	SMP
RGB	50Ω SE	50 mm ±1	4X	N/A	50Ω PD	SMP

3.5.2 System Specification

Two test fixtures are required to measure the signal quality of the display outputs. These test fixtures are called Compliance Load Board (CLB) and External Load Board (ELB). For PCIe compliance only one the CLB is required. Figure 3.14 shows the setup for the display outputs validation and Figure 3.15 shows the setup for PCIe validation.

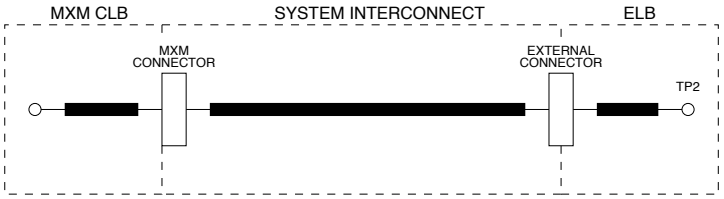


Figure 3.14: System Validation Test Setup (Display Interfaces)

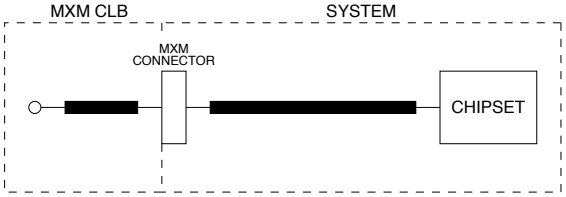


Figure 3.15: System Validation Test Setup (PCIe Interface)

Table 3.17: MXM CLB Specification

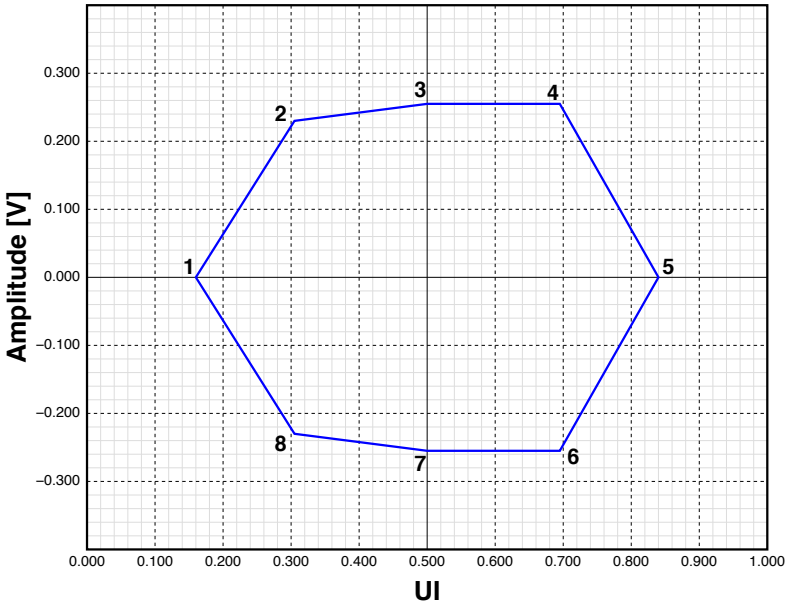
Interface	Impedance	Trace Length	Spacing	AC CAP	Termination	Connector
DP	100Ω diff	50 mm ±1	4X	N/A	N/A	SMP
TMDS	100Ω diff	50 mm ±1	4X	N/A	N/A	SMP
LVDS	100Ω diff	50 mm ±1	4X	N/A	N/A	SMP
PCIe	85Ω diff	50 mm ±1	4X	N/A	N/A	SMP
RGB	50Ω SE	50 mm ±1	4X	N/A	N/A	SMP

Table 3.18: ELB Specification

Interface	Impedance	Trace Length	Spacing	AC CAP	Termination	Connector
DP	100Ω diff	25 mm ±1	4X	N/A	N/A	SMP
TMDS	100Ω diff	25 mm ±1	4X	N/A	N/A	SMP
LVDS	100Ω diff	25 mm ±1	4X	N/A	N/A	SMP
RGB	50Ω SE	25 mm ±1	4X	N/A	N/A	SMP

3.5.3 DisplayPort

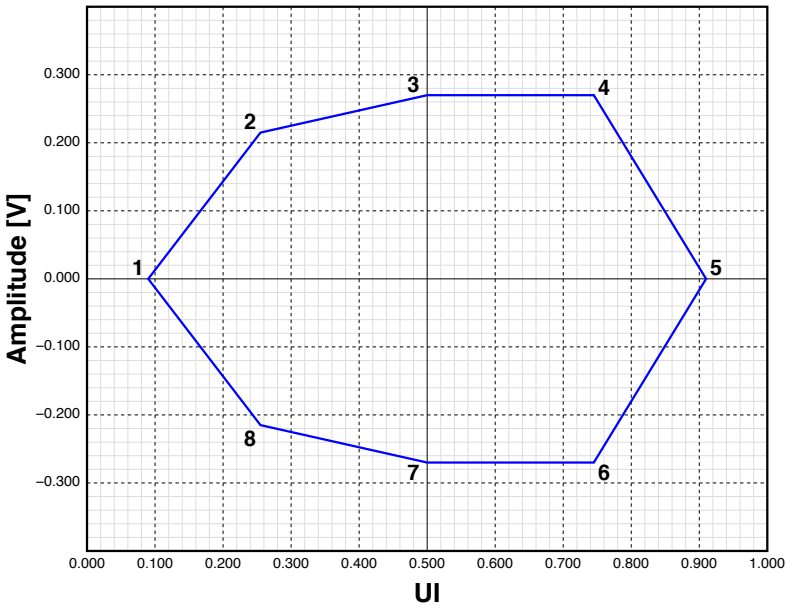
MXM compliant modules must meet the specification in Figure 3.16 for High Bit Rate (HBR) and Figure 3.17 for Reduced Bit Rate (RBR) at TP_MXM for all supported DisplayPorts.



Point	X	A [V]
1	0.160	0.000
2	0.305	0.230
3	0.500	0.255
4	0.695	0.255
5	0.840	0.000
6	0.695	-0.255
7	0.500	-0.255
8	0.305	-0.230

Jitter	
Non-ISI	0.265
TJ	0.320

Figure 3.16: DisplayPort HBR TP_MXM Eye Diagram



Point	X	A [V]
1	0.092	0.000
2	0.256	0.216
3	0.500	0.270
4	0.744	0.270
5	0.908	0.000
6	0.744	-0.270
7	0.500	-0.270
8	0.256	-0.216

Jitter	
Non-ISI	0.165
TJ	0.200

Figure 3.17: DisplayPort RBR TP_MXM Eye Diagram

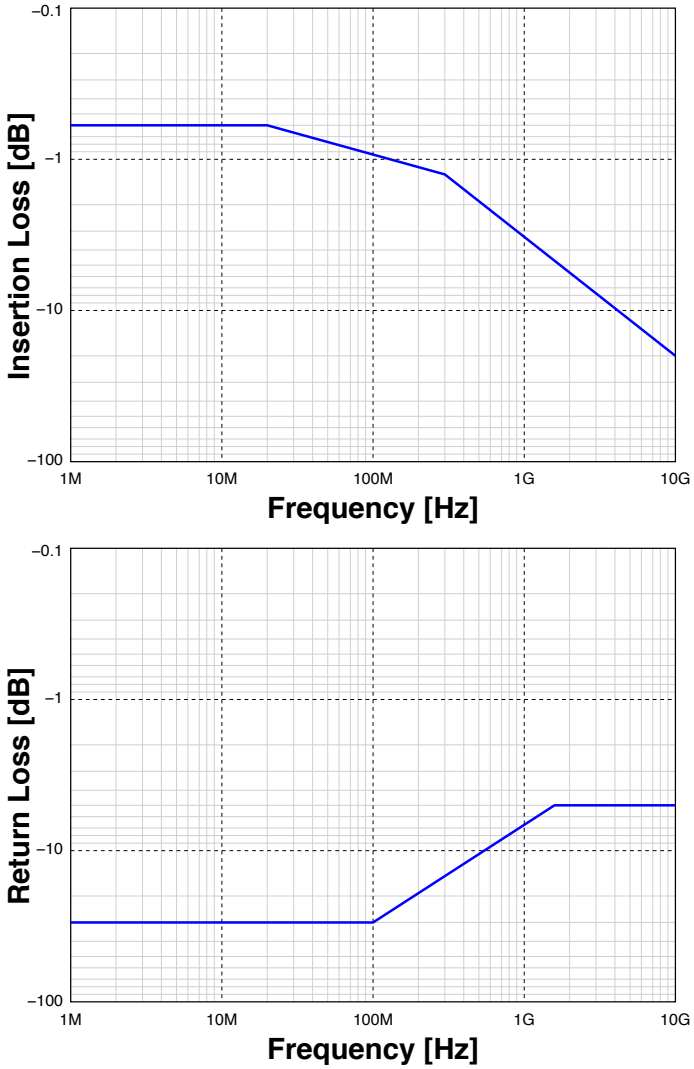
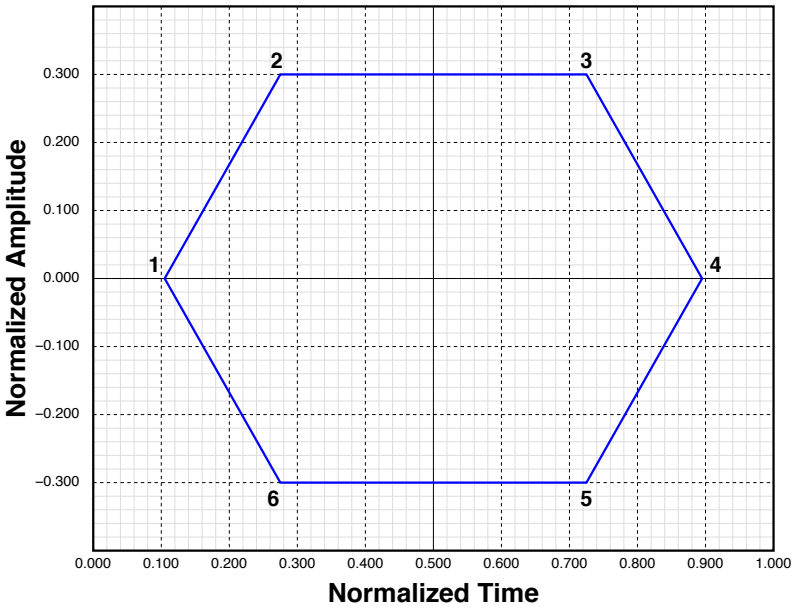


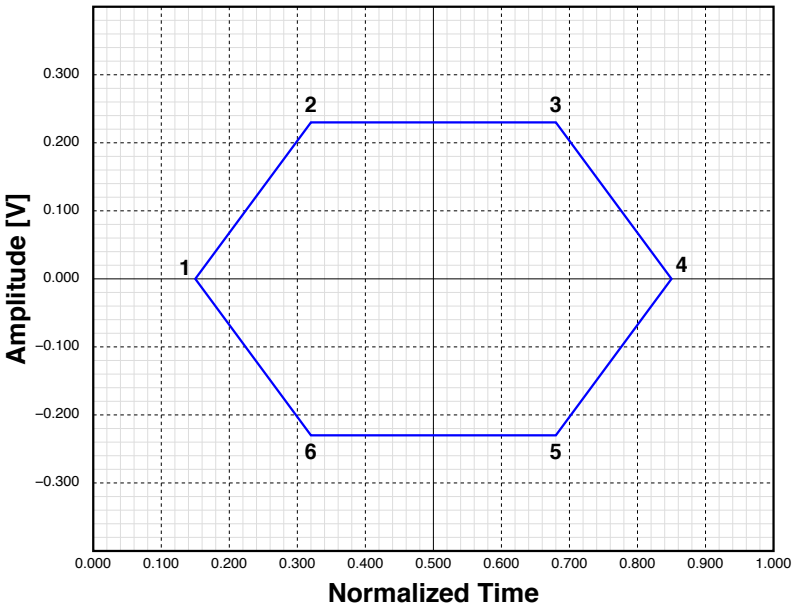
Figure 3.18: System Board Insertion and Return Loss Requirements for DisplayPort

3.5.4 TMDS and LVDS



Point	X	A
1	0.105	0.000
2	0.275	0.300
3	0.725	0.300
4	0.895	0.000
5	0.725	-0.300
6	0.275	-0.300

Figure 3.19: TMDS TP_MXM Eye Diagram



Point	X	A [V]
1	0.150	0.000
2	0.320	0.225
3	0.680	0.225
4	0.850	0.000
5	0.680	-0.225
6	0.320	-0.225

Figure 3.20: LVDS TP_MXM Eye Diagram

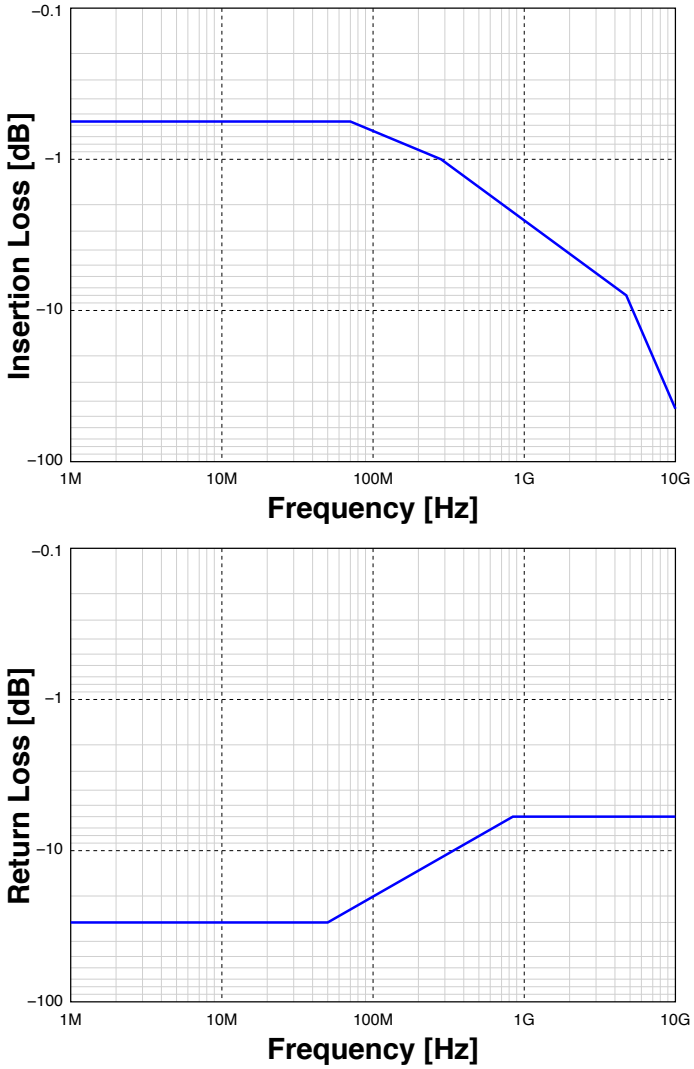
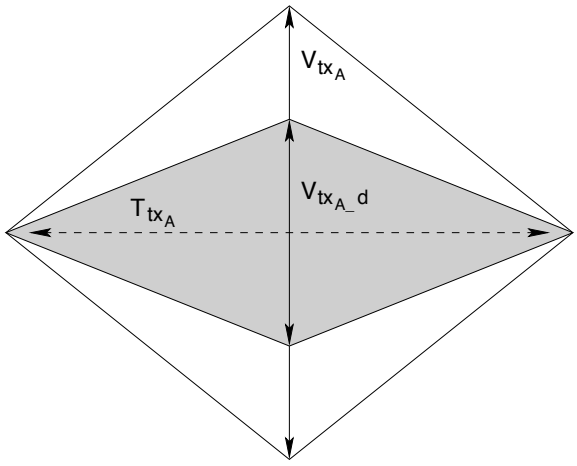


Figure 3.21: System Board Insertion an Return Loss Requirements for TMDS

3.5.5 PCI Express

Figure 3.22 shows the eye diagram requirement for the MXM module validation. The specification assumes an ideal reference clock without jitter and all links active while generating the eye diagram. All specifications are for 5GT/s at 3.5 dB de-emphasis.

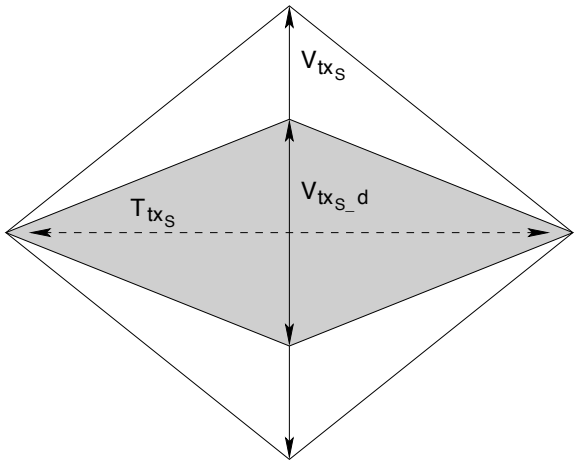


Parameter	Min	Max	Unit
V_{tx_A}	170	600	mV
$V_{tx_{A\_d}}$	170	600	mV
T_{tx_A}	123		ps

Jitter [ps]	
Deterministic Jitter (Dj)	57
Total Jitter (Tj)	77

Figure 3.22: MXM Module Transmitter Path Compliance Eye Diagram

Figure 3.23 shows the eye diagram requirement for the system validation. The specification assumes an ideal reference clock without jitter and all links active while generating the eye diagram. All specifications are for 5GT/s at 3.5 dB de-emphasis.



Parameter	Min	Max	Unit
V_{tx_S}	170	600	mV
$V_{tx_{S\_d}}$	170	600	mV
T_{tx_S}	95		ps

Jitter [ps]	
Deterministic Jitter (Dj)	57
Total Jitter (Tj)	105

Figure 3.23: System Board Transmitter Path Compliance Eye Diagram

3.6 DC Specifications

Table 3.19: CMOS and Open Drain Signals DC Specifications

Symbol	Parameter	Conditions	Min	Max	Units
CMOS Outputs					
V_{OL}	Output Low Voltage	I_{out} = 8 mA		0.3	V
V_{OH}	Output High Voltage	I_{out} = -8 mA	V_{3V3}-0.3		V
I_{out}	Output Current	V_{3V3} = 3.3 V	-8	8	mA
Open Drain Outputs					
V_{OL}	Output Low Voltage	I_{out} = 8 mA		0.3	V
I_{sink}	Sink Current			8	mA
PEX_RST# and PWR_LEVEL Inputs					
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{3V3}+0.5	V
C_{in}	Input Capacitance			30	pF
I_{In}	Input Leakage Current	0 to 3.3V	-100	100	μA
All other CMOS Inputs					
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{3V3}+0.5	V
I_{In}	Input Leakage Current	0 to 3.3V	-1	1	mA
Open Drain Inputs					
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{3V3}+0.5	V

Chapter 4

Thermal Specification

The MXM version 3.0 thermal and mechanical specifications enable interchangeability of MXM graphics cards from alternate manufacturers with a single thermal solution. A notebook system integrator will be able to design a single thermal solution and be assured that it is mechanically and thermally compatible with all MXM graphics cards provided the module is also MXM version 3.0 compliant and of the same or lower Total Graphics Power (TGP). An example of this interchangeability concept is presented in Figure 4.1.

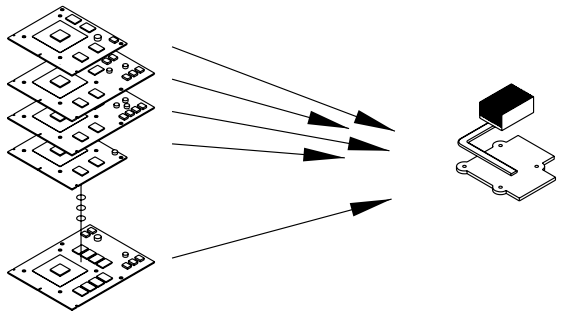


Figure 4.1: MXM Thermal Compatibility

4.1 Thermal Specification Philosophy

The thermal specification utilizes definitions of thermal regions with known graphics subsystem power to impose thermal constraints on the computer system, MXM module (PCB and Components), and the thermal solution that enables the MXM version 3.0 concept of one cooler for multiple boards.

4.1.1 System Thermal Components

A MXM compliant computer system, from a thermal perspective, can be subdivided into three separate components:

- ❑ MXM module
- ❑ System housing
- ❑ Thermal solution

The three components are shown graphically in Figure 4.2.

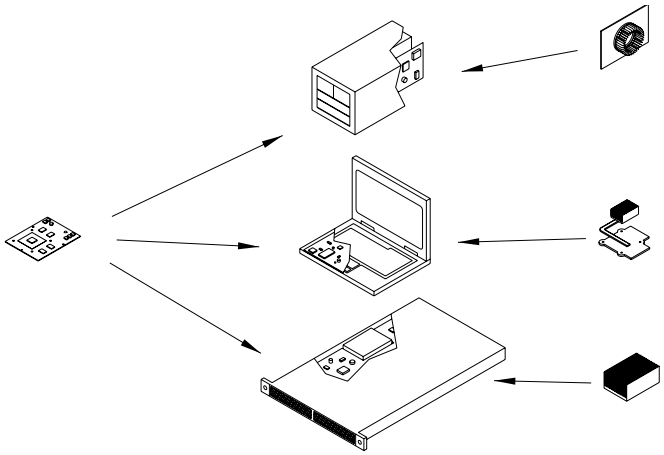


Figure 4.2: MXM System Thermal Components

The MXM version 3.0 specification defines distinct requirements on each of these three components. The system housing requirements are defined by an ambient temperature restriction. The MXM module component is defined by a thermal budget based on the maximum allowable temperatures of all non-GPU components. The thermal solution component is specified by temperatures on the heat spreader/thermal plate as well as the overall TGP.

4.1.2 Power Sources

A key part of deriving the thermal specification is having an understanding of the amount of power that each component on the graphics card will dissipate. Components are grouped into two types. A group that requires direct cooling and a group that does not. Components that require direct cooling must only be placed on the top side of the MXM module and include the graphics processor, power supply regulators, inductors, and MOSFETs. Memory placed on the top side of the PCB is also required to have direct cooling. All components positioned on the bottom of the module should be assessed to determine if they may need to be moved to the top and receive direct cooling. The manufacturer's data sheets should be consulted to make this placement assessment in conjunction with the typical power distribution breakdown given in Table 4.1. The power dissipated per component will vary significantly depending on the total board power. However, the distribution of power between power consuming components is relatively constant and even then when the distribution does vary, the changes will primarily impact spreading resistance in the cooler plate rather than overall cooling capacity.

Table 4.1: MXM Assumptions on Power Distribution

Component/Group	Zone	% of Module TGP
GPU	1	70±5
Memory	2	17±5
Power Supply	3	17±5

4.2 Thermal Requirements

4.2.1 System Requirements

The system requirements are summarized in Table 4.2. The internal ambient temperatures near the module are measured from the locations near the bottom of the MXM PCB shown in Figure 4.3. The maximum allowable average temperature is 65 C, and the highest of any of the three must be less than or equal to 75 C. The height of the temperature measurement locations is 4 mm from the bottom of the MXM module. If the required clearance is not available because of mechanical assembly (for example the system board or the system chassis are closer than 4 mm from the module), then the temperature of the surface adjacent to the module should be measured.

Table 4.2: Ambient Temperature Specification

Internal Average Ambient Temperature	$T_{A(int)} = (T_{A1} + T_{A2} + T_{A3})/3 \leq 65C$
Internal Individual Ambient Temperature	$(T_{A1}, T_{A2}, T_{A3}) \leq 75C$

Table 4.3: Ambient Temperature Measurement Locations Dimensions

Symbol	**[mm]**			**[in]**		
	min	**nom**	**max**	**min**	**nom**	**max**
K1	79.74	80.00	80.26	3.139	3.150	3.160
K2	59.74	60.00	60.26	2.352	2.362	2.372
K3	34.74	35.00	35.26	1.368	1.378	1.388
K4	29.74	30.00	30.26	1.171	1.181	1.191
K5	67.74	68.00	68.26	2.667	2.677	2.687
K6	72.74	73.00	73.26	2.864	2.874	2.884
K7	50.74	51.00	51.26	1.998	2.008	2.018
K8	65.74	66.00	66.26	2.588	2.598	2.609
K9	65.74	66.00	66.26	2.588	2.598	2.609
K10	64.74	65.00	65.26	2.549	2.559	2.569

4.2.2 Module Thermal Requirements

It is the responsibility of the board designer to assess whether components will be adequately cooled on the board given the guidance from the MXM specification. The MOSFETs and inductors also have clearly defined maximum operational limits on which the system integrator can impose additional deratings if they so choose. To ensure proper placement and height considerations, the module designer shall always be fully responsible for specifying the thermal interface material needed to cool board components. Thermal interface materials must be selected such that when the thermal solution is mounted to the MXM module that there is no deflection beyond allowable mechanical limits specified in the MXM 3.0 specification, Section 2.3.3. The module designer must select interface materials for all non-GPU components given the two sets of bounding temperatures and the power distribution estimates obtained using Table 4.1 and Table 4.4. In all situations except what is outlined in the following paragraph, the non-GPU thermal interface pads shall accompany the MXM module and be part of the BOM of the MXM module.

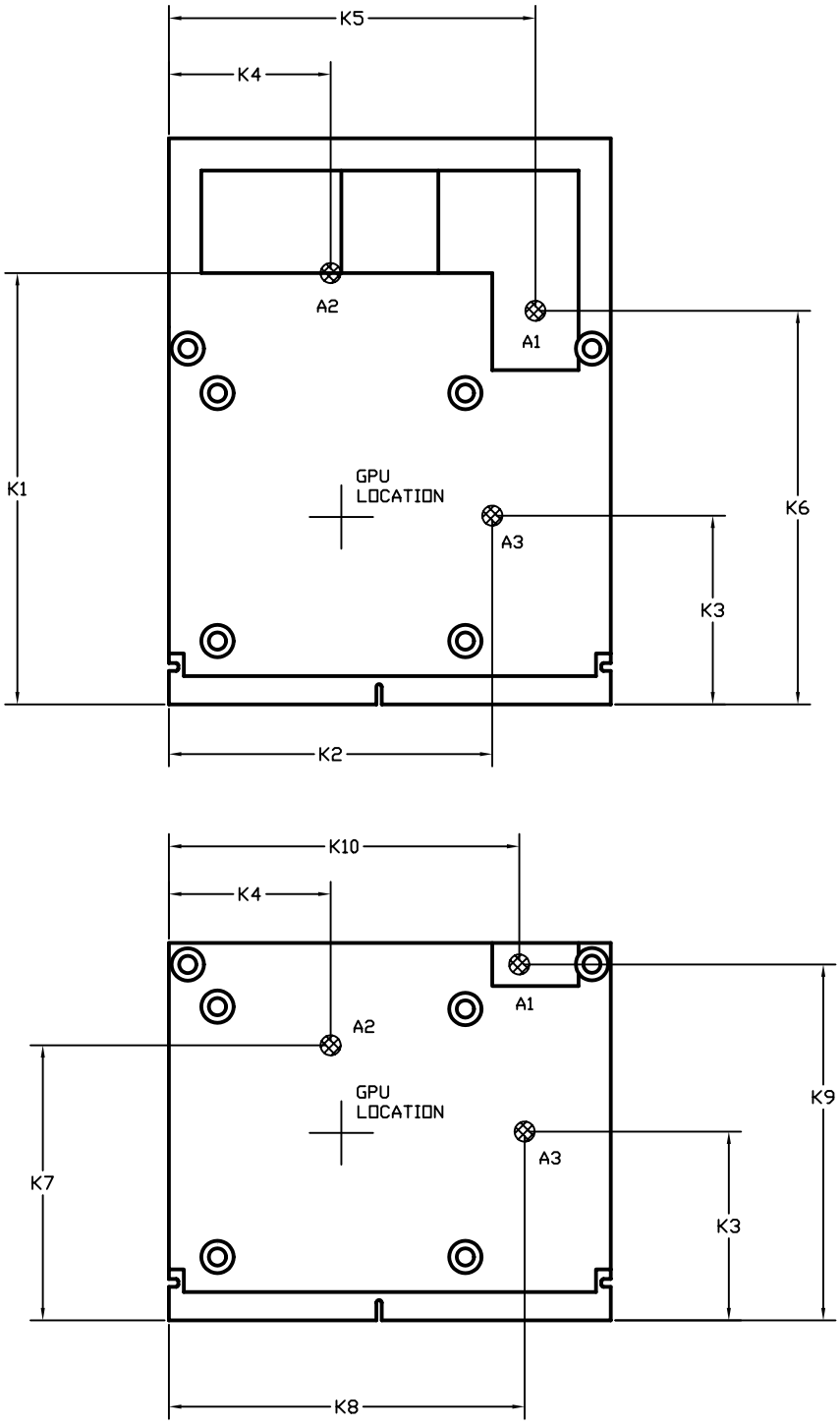


Figure 4.3: Type A and Type B Ambient Temperature Measurement Locations

The only exception to the above requirement is if a system integrator has adequate control over the graphics card design and supply chain such that the integrator can manage the acquisition and assembly of the interface material separately from the board acquisition. However, even if the system integrator assumes responsibility for thermal interface material acquisition and assembly, the graphics board supplier is still responsible for specifying the interface material. After the system has been assembled, and if an MXM board is to be replaced with a new module, then the thermal interface materials for that new board must accompany that replacement MXM module.

The memory is a special case because there will be designs that require memory to be on the back of MXM modules. The memory on the top will be cooled directly by the thermal solution, and the memory on the back will not have any direct cooling. In both the cooled and uncooled case, the maximum allowable memory case temperature is 115 C.

Note: No critical power components other than memory are allowed on the back side of the PCB.

4.2.3 Thermal Solution Requirements

The thermal solution for the MXM version 3.0 graphics board includes the GPU thermal interface material, thermal spreader, heat transport mechanism and heat exchanger to the external ambient thermal sink. The cooler shall maintain all critical component temperatures below their maximum values. The mechanical attachment of the cooler will be GPU die referenced with center loading. All non-GPU thermal interface material is part of the MXM Module as described in Section 4.2.2. The thermal conditions outlined in the specification must be met with no forced air flow across the MXM PCB. It is left to the system and thermal solution designers to determine appropriate external ambient and/or fan inlet temperatures based on their respective design criteria.

Note: Regardless of the operational mode of the MXM module, all board components shall not exceed the derated critical temperatures set by the MXM module designer and secondarily, the manufacturer's temperature limits.

The spreading capability of the thermal solution is assured by maintaining required temperatures within each of three thermal spreader zones. These zones are shown in Figure 4.4 and Figure 4.5. Zone #1 is for the GPU, Zone #2 is for the memory, Zone #3 for the power supply. It is highly recommended that MOSFETs for the power supply be located along the periphery of the power supply zone for Type-B in the 1.5 mm PCB keep-in zone to ensure the best possible cooling.

The temperature of a specific thermal zone must meet the temperature requirements defined in Table 4.4 while keeping each component within their respective thermal limits. In order to meet or exceed the minimum thermal requirements, the thermal solution designer has the flexibility to customize the cooler provided that the temperature limits are met and the physical height restrictions on the MXM module are respected.

Table 4.5: Thermal Solution Spreader Bottom Side Profile Step Requirements

Top Side Height Restriction	Spreader Plate Profile Requirement
1.5 mm	Base Height (Datum)
1.8 mm	+0.6 mm Step
2.2 mm	+1.0 mm Step
4.0 mm	+2.8 mm Step

Table 4.4: Maximum Spreader Plate Temperatures

Component/Group	Zone	Symbol	Maximum Temperature
GPU	1	T_1	90C
Memory	2	T_2	90C
Power Supply	3	T_3	90C

The cooler spreader plate must maintain a certain profile due to the variation in GPU heights and to preserve the physical compatibility with MXM cards and ensure optimal thermal interface materials selection. The cooler profile requirements are described in Table 4.5. These requirements only apply to the bottom of the spreader. The top of the spreader is not restricted by these requirements. The first column references the PCB top side height restrictions described in Figure 2.5 and Figure 2.6. The second column describes the cooler profile in terms of the step increases away from the PCB relative to the 1.5 mm board height zone which is used as a plane datum for the step increases.

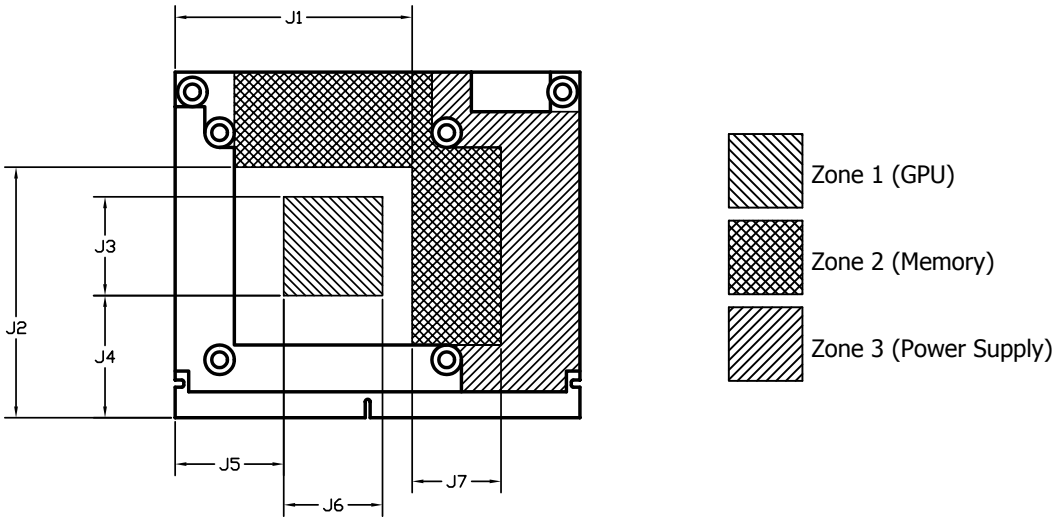


Figure 4.4: Type A Thermal Zones

Table 4.6: Type A Thermal Zones Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
J1	47.87	48.00	48.13	1.885	1.890	1.895
J2	50.62	50.75	50.88	1.993	1.998	2.003
J3	19.87	20.00	20.13	0.782	0.787	0.793
J4	24.62	24.75	24.88	0.969	0.974	0.980
J5	21.87	22.00	22.13	0.861	0.866	0.871
J6	19.87	20.00	20.13	0.782	0.787	0.793
J7	18.00	18.00	18.00	0.709	0.709	0.709

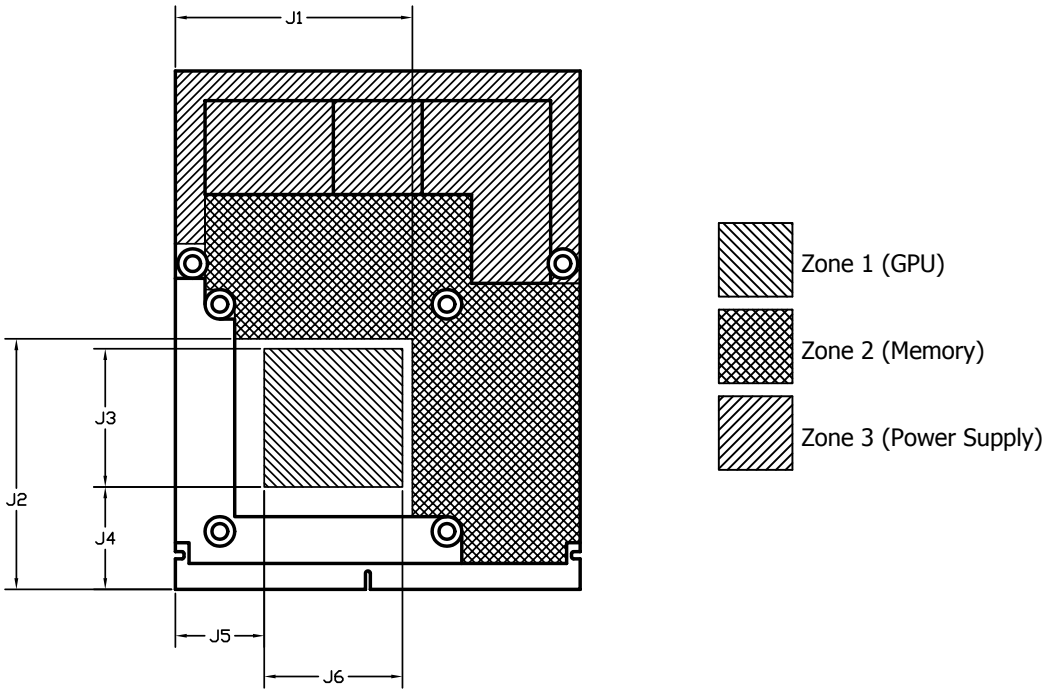


Figure 4.5: Type B Thermal Zones

Table 4.7: Type B Thermal Zones Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
J1	47.87	48.00	48.13	1.885	1.890	1.895
J2	50.62	50.75	50.88	1.993	1.998	2.003
J3	27.87	28.00	28.13	1.097	1.102	1.107
J4	20.62	20.75	20.88	0.812	0.817	0.822
J5	17.87	18.00	18.13	0.704	0.709	0.714
J6	27.87	28.00	28.13	1.097	1.102	1.107

4.3 Thermal Specification Summary

The MXM Thermal specification is summarized in Table 4.8. The specification makes specific assumptions described in Table 4.1 on the power distribution on the module. Refer to the appropriate sections for detailed explanations.

Table 4.8: Thermal Specification Summary

Thermal Region	Specification	Notes
System	$T_{A(int)} \leq$ 65C	The average temperature of three locations (Section 4.2.1).
System	$(T_{A1}, T_{A2}, T_{A3}) \leq$ 75C	Maximum temperature at any of the locations.
Memory	$T_{Case} \leq$ 115C	For memory on the front or back side.
Zone 1	$T_1 \leq$ 90C	Temp. of spreader directly above the GPU (Section 4.2.3).
Zone 2	$T_2 \leq$ 90C	Temp. of spreader in the zone over the memory (Section 4.2.3).
Zone 3	$T_3 \leq$ 90C	Temp. of spreader in the power supply zone (Section 4.2.3).

Applicable Documents

The following documents contain provisions which through reference in this text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. However, users of this standard are advised to ensure they have the latest versions of referenced standards and documents.

- ❑ MXM Software Specification, Version 3.0
- ❑ MXM Graphics Module Tolerance Analysis and Design Suggestions, Version 3.0
- ❑ MXM Version 3.0 Connector Interoperability Design Guide, Release 1.0
- ❑ MXM Version 3.0 Dual-Link DVI Implementation Application Note, Release 1.0
- ❑ PCI Express Base Specification, Revision 2.0
- ❑ PCI Express Card Electromechanical Specification, Revision 2
- ❑ VESA DisplayPort Standard, Version 1.1
- ❑ SMBus Specification, Revision 2.0
- ❑ Advanced Configuration and Power Interface (ACPI) Specification, Revision 3.0
- ❑ SPWG Notebook Panel Specification, Version 3.0
- ❑ Digital Visual Interface (DVI), Version 1.0
- ❑ HDMI 1.3 – High-Definition Multimedia Interface (HDMI) Specification
- ❑ VESA Enhanced Display Data Channel (EDDC) Standard Version 1.2
- ❑ DisplayPort Interoperability Guideline Version 1.1
- ❑ IPC-A-600F – Acceptability of Printed Circuit Boards
- ❑ IPC-A-610D – Acceptability of Electronic Assemblies
- ❑ EIA-364-9 – Durability Test Procedure for Electrical Connectors and Contacts
- ❑ EIA-364-28D – Vibration Test Procedure for Electrical Connectors and Sockets
- ❑ EIA-364-27B – Mechanical Shock (Specified Pulse) Test Procedure for Electrical Connectors
- ❑ EIA-364-23B – Low Level Contact Resistance Test Procedure for Electrical Connectors and Sockets

- EIA-364-13C – Mating and Unmating Forces Test Procedure for Electrical Connectors
- EIA-364-21C – Insulation Resistance Test Procedure for Electrical Connectors, Sockets and Coaxial Contacts
- EIA-364-20C – Withstanding Voltage Test Procedure for Electrical Connectors, Sockets and Coaxial Contacts
- EIA-364-108 – Impedance, Reflection Coefficient, Return Loss and VSWR Measured in the Time and Frequency Domain Test Procedure for Electrical Connectors, Cable Assemblies or Interconnection Systems
- EIA-364-101 – Attenuation Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems
- EIA-364-90 – Crosstalk Ratio Test Procedures for Electrical Connectors, Sockets, Cable Assemblies or Interconnect Systems
- EIA-364-1000.1 – Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications
- ASME Y14.5M – Dimensioning and Tolerancing Standard

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