**Satck 6T SRAM**

.tran 10n 80n

vs vdd GND 5

v1 bl GND BIT ({1100})

v2 blbar GND BIT ({0011})

v3 wl GND BIT ({11111})

.power vs 0n 100n

.print tran v(bl) v(blbar) v(wl) v(q) v(qbar)

**D FLIPFLOP**

.tran 10n 80n

vs vdd GND 5

v1 d GND BIT ({11111})

v2 clk GND BIT ({11111})

.power vs 0n 100n

.print tran v(d) v(clk) v(q) v(qbar)

**RIPPLE CARRY ADDER**

.tran 10n 80n

vs vdd GND 5

v1 a0 GND BIT ({1111})

v2 b0 GND BIT ({1111})

v3 a1 GND BIT ({0000})

v4 b1 GND BIT ({0000})

v5 a2 GND BIT ({0011})

v6 b2 GND BIT ({0011})

v7 a3 GND BIT ({1100})

v8 b3 GND BIT ({1100})

v9 cin GND BIT ({1100})

.power vs 0n 100n

.print tran v(a0) v(b0) v(cin) v(a1) v(b1) v(a2) v(b2) v(a3) v(b3) v(s0) v(s1) v(s2) v(s3) v(cout)

**FULL SUBTRACTOR**

.tran 10n 80n

vs vdd GND 5

v1 a GND BIT ({001})

v2 b GND BIT ({000})

v3 c GND BIT ({111})

.power vs 0n 100n

.print tran v(a) v(b) v(c) v(difference) v(borrow)

**HALF SUBTRACTOR**

.tran 10n 80n

vs vdd GND 5

v1 a GND BIT ({11})

v2 b GND BIT ({11})

.power vs 0n 100n

.print tran v(a) v(b) v(difference) v(borrow)

**FULL ADDER**

.tran 10n 80n

vs vdd GND 5

v1 a GND BIT ({111})

v2 b GND BIT ({111})

v3 c GND BIT ({111})

.power vs 0n 100n

.print tran v(a) v(b) v(c) v(sum) v(carry)

**HALF ADDER**

.tran 10n 80n

vs vdd GND 5

v1 a GND BIT ({11})

v2 b GND BIT ({11})

.power vs 0n 100n

.print tran v(a) v(b) v(s) v(c)

**XOR GATE**

.tran 10n 80n

vs vdd GND 5

v1 a GND BIT ({1})

v2 b GND BIT ({1})

.power vs 0n 100n

.print tran v(a) v(b) v(c)

**OR GATE**

.tran 10n 80n

vs vdd GND 5

v1 a GND BIT ({0000})

v2 b GND BIT ({1111})

.power vs 0n 100n

.print tran v(a) v(b) v(c)

**AND GATE**

.tran 10n 80n

vs vdd GND 5

v1 a GND BIT ({1111})

v2 b GND BIT ({1111})

.power vs 0n 100n

.print tran v(a) v(b) v(c)

**NOR GATE**

.tran 10n 80n

vs vdd GND 5

v1 a GND BIT ({1111})

v2 b GND BIT ({1111})

.power vs 0n 100n

.print tran v(a) v(b) v(c)

**NAND GATE**

.tran 10n 80n

vs vdd GND 5

v1 a GND BIT ({1111})

v2 b GND BIT ({1111})

.power vs 0n 100n

.print tran v(a) v(b) v(c)

**INVERTER**

.tran 10n 80n

vs vdd GND 5

v1 in GND BIT ({1111})

.power vs 0n 100n

.print tran v(in) v(out)