**6T SRAM**

**.**tran 10n 80n

vs vdd GND 5

v1 bl GND BIT ({111000})

v2 blbar GND BIT ({010101})

v3 wl GND BIT ({111111})

.power vs 0n 100n

.print tran v(bl) v(blbar) v(wl)

**Power Results**

vs from time 0 to 1e-007

Average power consumed -> 2.272421e-003 watts

Max power 1.647981e-002 at time 4.1e-008

Min power 1.343802e-009 at time 0

**MODIFIED 6T**

.tran 10n 80n

vs vdd GND 5

v1 bl GND BIT ({1100})

v2 blbar GND BIT ({0011})

v3 wl GND BIT ({1100})

.power vs 0n 100n

.print tran v(bl) v(blbar) v(wl) v(q) v(qbar)

**Power Results**

vs from time 0 to 1e-007

Average power consumed -> 2.112913e-003 watts

Max power 1.007261e-002 at time 4.1e-008

Min power 1.069875e-009 at time 0

**7T SRAM**

.tran 10n 80n

vs vdd GND 5

v1 wbl GND BIT ({111})

v2 wblb GND BIT ({000})

v3 rwl GND BIT ({111})

v4 wl GND BIT ({111})

.power vs 0n 100n

.print tran v(wbl) v(wblb) v(rwl) v(wwl) v(q) v(qbar)

**Power Results**

vs from time 0 to 1e-007

Average power consumed -> 2.234654e-003 watts

Max power 2.793318e-003 at time 6e-008

Min power 2.793318e-003 at time 2.6875e-008

**8T SRAM**

.tran 10n 80n

vs vdd GND 5

v1 wbl GND BIT ({11})

v2 wbbl GND BIT ({00})

v3 rwl 1 BIT ({11})

v4 rbl 1 BIT ({00})

v5 wwl 1 BIT ({11})

.power vs 0n 100n

.print tran v(wwl) v(wbl) v(wbbl) v(rwl) v(rbl) v(q) v(qbar)

**Power Results**

vs from time 0 to 1e-007

Average power consumed -> 3.202073e-003 watts

Max power 4.002591e-003 at time 0

Min power 4.002591e-003 at time 6.25e-010

**9T SRAM**

.tran 10n 80n

vs vdd GND 5

v1 bl GND BIT ({1100})

v2 blb GND BIT ({0011})

v3 rd GND BIT ({0011})

v4 wl GND BIT ({1100})

.power vs 0n 100n

.print tran v(bl) v(blb) v(rd) v(wl) v(q) v(qbar)

**Power Results**

vs from time 0 to 1e-007

Average power consumed -> 1.075040e-009 watts

Max power 1.343800e-009 at time 2e-008

Min power 1.343800e-009 at time 0

**STACK 9T SRAM**

.tran 10n 80n

vs vdd GND 5

v1 bl GND BIT ({11})

v2 blbar GND BIT ({00})

v3 wl GND BIT ({00})

v4 rd GND BIT ({01})

.power vs 0n 100n

.print tran v(bl) v(blbar) v(wl) v(rd) v(q) v(qbar)

**Power Results**

vs from time 0 to 1e-007

Average power consumed -> 8.559002e-010 watts

Max power 1.069875e-009 at time 2e-008

Min power 1.069875e-009 at time 0

**BIT LINE 9T**

.tran 10n 80n

vs vdd GND 5

v1 wbl GND BIT ({1100})

v2 wblb GND BIT ({0011})

v3 wwl GND BIT ({1111})

v4 rwl GND BIT ({0000})

v5 rbl GND BIT ({0000})

.power vs 0n 100n

.print tran v(wbl) v(wblb) v(wwl) v(rbl) v(rwl)

**Power Results**

vs from time 0 to 1e-007

Average power consumed -> 1.075042e-009 watts

Max power 1.343802e-009 at time 2e-008

Min power 1.343802e-009 at time 0

**Proposed 9T**

.tran 10n 80n

vs vdd GND 5

v1 bl GND BIT ({1100})

v2 blb GND BIT ({0011})

v3 wl GND BIT ({1111})

v4 rwl GND BIT ({0000})

v5 rbl GND BIT ({0000})

v6 wr GND BIT ({1111})

.power vs 0n 100n

.print tran v(bl) v(blb) v(wl) v(rwl) v(rbl) v(wr)

**Power Results**

vs from time 0 to 1e-007

Average power consumed -> 6.937375e-005 watts

Max power 8.671719e-005 at time 0

Min power 8.671719e-005 at time 6.25e-008

**SF-9T SRAM**

.tran 10n 80n

vs vdd GND 5

v1 wbl GND BIT ({111})

v2 wblb GND BIT ({000})

v3 wwl GND BIT ({111})

v4 rbl GND BIT ({000})

v5 rwl GND BIT ({000})

.power vs 0n 100n

.print tran v(wbl) v(wblb) v(wwl) v(rwl) v(rbl) v(q) v(qbar)

**Power Results**

vs from time 0 to 1e-007

Average power consumed -> 7.772715e-010 watts

Max power 9.715893e-010 at time 6.25e-008

Min power 9.715893e-010 at time 3.25e-008

**Read Stability**

.tran 10n 80n

vs vdd GND 5

v1 bl GND BIT ({1100})

v2 blb GND BIT ({0011})

v3 ctrl GND BIT ({0011})

v4 rd GND BIT ({0011})

v5 wr GND BIT ({1100})

.power vs 0n 100n

.print tran v(bl) v(blb) v(rd) v(ctrl) v(wr)

**Power Results**

vs from time 0 to 1e-007

Average power consumed -> 8.098175e-005 watts

Max power 1.012272e-004 at time 2e-008

Min power 1.012272e-004 at time 0

**New design 1**

**write**

.tran 10n 80n

vs vdd GND 5

v1 wr GND BIT ({1100})

v2 bl GND BIT ({1100})

v3 blb GND BIT ({0011})

v4 rd GND BIT ({0011})

v5 ctrl GND BIT ({0011})

.power vs 0n 100n

.print tran v(wr) v(bl) v(blb) v(rd) v(ctrl)

**read**

.tran 10n 80n

vs vdd GND 5

v1 wr GND BIT ({0011})

v2 bl GND BIT ({0011})

v3 blb GND BIT ({1100})

v4 rd GND BIT ({1100})

v5 ctrl GND BIT ({1100})

.power vs 0n 100n

.print tran v(wr) v(bl) v(blb) v(rd) v(ctrl)

**Power results**

vs from time 0 to 1e-007

Average power consumed -> 2.680574e-005 watts

Max power 1.002972e-004 at time 2.1e-008

Min power 3.070449e-011 at time 5.90251e-008

**Delay cal**

.tran 10n 100n

vs vdd GND 5

v1 bl GND BIT ({1010} pw=20n lt=9n ht=9n rt=1n ft=1n)

v2 blb GND BIT ({0101} pw=20n lt=9n ht=9n rt=1n ft=1n)

v3 wr GND BIT ({1111} pw=20n lt=9n ht=9n rt=1n ft=1n)

.print tran v(bl) v(blb) v(wr) v(q) v(qbar)

.MEASURE TRAN FallTime TRIG v(bl) VAL='2.5' TD=0 Fall=1 TARG v(qbar) VAL='2.5' TD=0 Rise=1 ON

.MEASURE TRAN RiseTime TRIG v(bl) VAL='2.5' TD=0 Rise=1 TARG v(qbar) VAL='2.5' TD=0 Fall=1 ON

.MEASURE TRAN propogationDelay PARAM='(Falltime + Risetime)/2.0' ON

**Result**

MEASUREMENT RESULTS

FallTime = 8.6372e-011

Trigger = 9.5000e-009

Target = 9.5864e-009

RiseTime = -5.5373e-011

Trigger = 1.8500e-008

Target = 1.8445e-008

propogationDelay = 1.5499e-011

**read and write (ref:cell 1)**

.tran 10n 500n

vs vdd GND 5

v1 wr GND BIT ({101} pw=200n lt=100n ht=100n)

v2 bl GND BIT ({100} pw=200n lt=100n ht=100n)

v3 blb GND BIT ({011} pw=200n lt=100n ht=100n)

v4 rd GND BIT ({010} pw=200n lt=100n ht=100n)

v5 ctrl GND BIT ({010} pw=200n lt=100n ht=100n)

.power vs 0n 100n

.print tran v(wr) v(bl) v(blb) v(q) v(qbar)

**sense amplifier**

.tran 10n 1000n

vs vdd GND 5

v1 bl GND BIT ({10} pw=500n lt=250n ht=250n)

v2 blb GND BIT ({01} pw=500n lt=250n ht=250n)

v3 sae GND BIT ({11} pw=500n lt=250n ht=250n)

v4 pre GND BIT ({00} pw=500n lt=250n ht=250n)

.power vs 0n 100n

.print tran v(bl) v(blb) v(pre) v(sae) v(out) v(outb)

**2 i/p decoder**

.tran 10n 500n

vs vdd GND 5

v1 a0 GND BIT ({01} pw=100n lt=50n ht=50n)

v2 a1 GND BIT ({01} pw=100n lt=50n ht=50n)

v3 p GND BIT ({00})

.print tran v(a0) v(a1) v(p) v(wl0) v(wl3)

**.tran 10n 1000n**

**vs vdd GND 5**

**v1 a0 GND BIT ({0011} pw=200n lt=100n ht=100n)**

**v2 a1 GND BIT ({0101} pw=100n lt=100n ht=100n)**

**.print tran v(a0) v(a1) v(wl0) v(wl1) v(wl2) v(wl3)**

**3i/p decoder**

.tran 10n 500n

vs vdd GND 5

v1 a0 GND BIT ({01} pw=100n lt=50n ht=50n)

v2 a1 GND BIT ({01} pw=100n lt=50n ht=50n)

v3 a2 GND BIT ({01} pw=100n lt=50n ht=50n)

v4 p GND BIT ({0} pw=100n lt=50n ht=50n)

.print tran v(a0) v(a1) v(a2) v(p) v(wl0) v(wl7)

**4 i/p decoder**

.tran 10n 500n

vs vdd GND 5

v1 a0 GND BIT ({01} pw=100n lt=50n ht=50n)

v2 a1 GND BIT ({01} pw=100n lt=50n ht=50n)

v3 a2 GND BIT ({01} pw=100n lt=50n ht=50n)

v4 a3 GND BIT ({01} pw=100n lt=50n ht=50n)

v5 p GND BIT ({00} pw=100n lt=50n ht=50n)

.print tran v(a0) v(a1) v(a2) v(a3) v(p) v(wl0) v(wl15)

**SR flipflop**

.tran 10n 80n

vs vdd GND 5

v1 s GND BIT ({10})

v2 r GND BIT ({01})

v3 clk GND BIT ({11})

.print tran v(s) v(r) v(clk) v(q) v(qbar)

**Array 2 (ref:cell 9)**

.tran 10n 2000n

vs vdd GND 5

v1 r/w GND BIT ({01} pw=200n lt=100n ht=100n)

v2 din GND BIT ({11} pw=200n lt=100n ht=100n)

v3 a0 GND BIT ({11} pw=200n lt=100n ht=100n)

v4 wl0 GND BIT ({11} pw=200n lt=100n ht=100n)

v5 rd GND BIT ({01} pw=200n lt=100n ht=100n)

v6 ctrl GND BIT ({01} pw=200n lt=100n ht=100n)

v7 wl1 GND BIT ({11} pw=200n lt=100n ht=100n)

v8 rd1 GND BIT ({01} pw=200n lt=100n ht=100n)

v9 ctrl1 GND BIT ({01} pw=200n lt=100n ht=100n)

v10 clk GND BIT ({11} pw=200n lt=100n ht=100n)

v11 bl0 GND BIT ({10} pw=200n lt=100n ht=100n)

v12 b0 GND BIT ({10} pw=200n lt=100n ht=100n)

.power vs 0n 100n

.print tran v(r/w) v(din) v(a0) v(q) v(q1) v(dout)

**Array 4\*4(ref:13)**

.tran 10n 2000n

vs vdd GND 5

v1 r/w GND BIT ({01} pw=200n lt=100n ht=100n)

v2 din GND BIT ({11} pw=200n lt=100n ht=100n)

v3 wl0 GND BIT ({11} pw=200n lt=100n ht=100n)

v4 rd GND BIT ({01} pw=200n lt=100n ht=100n)

v5 ctrl GND BIT ({01} pw=200n lt=100n ht=100n)

v6 wl1 GND BIT ({11} pw=200n lt=100n ht=100n)

v7 rd1 GND BIT ({01} pw=200n lt=100n ht=100n)

v8 ctrl1 GND BIT ({01} pw=200n lt=100n ht=100n)

v9 clk GND BIT ({11} pw=200n lt=100n ht=100n)

v10 bl0 GND BIT ({10} pw=200n lt=100n ht=100n)

v11 wl2 GND BIT ({11} pw=200n lt=100n ht=100n)

v12 wl3 GND BIT ({11} pw=200n lt=100n ht=100n)

.power vs 0n 100n

.print tran v(r/w) v(din) v(bl0) v(dout)

**Array 2 using sense amplifier(ref:cell 18)**

.tran 10n 2000n

vs vdd GND 5

v1 r/w GND BIT ({01} pw=200n lt=100n ht=100n)

v2 din GND BIT ({11} pw=200n lt=100n ht=100n)

v3 a0 GND BIT ({11} pw=200n lt=100n ht=100n)

v4 wl0 GND BIT ({11} pw=200n lt=100n ht=100n)

v5 rd GND BIT ({01} pw=200n lt=100n ht=100n)

v6 ctrl GND BIT ({01} pw=200n lt=100n ht=100n)

v7 wl1 GND BIT ({11} pw=200n lt=100n ht=100n)

v8 rd1 GND BIT ({01} pw=200n lt=100n ht=100n)

v9 ctrl1 GND BIT ({01} pw=200n lt=100n ht=100n)

v10 clk GND BIT ({11} pw=200n lt=100n ht=100n)

v11 bl0 GND BIT ({10} pw=200n lt=100n ht=100n)

v12 b0 GND BIT ({10} pw=200n lt=100n ht=100n)

v13 sae GND BIT ({11} pw=200n lt=100n ht=100n)

v14 ymux GND BIT ({00} pw=200n lt=100n ht=100n)

.power vs 0n 100n

.print tran v(r/w) v(bl0) v(out) v(sae)v(dout)

**Array 4 using sense amp(ref : cell 19)**

.tran 10n 2000n

vs vdd GND 5

v1 r/w GND BIT ({01} pw=200n lt=100n ht=100n)

v2 din GND BIT ({11} pw=200n lt=100n ht=100n)

v3 wl0 GND BIT ({11} pw=200n lt=100n ht=100n)

v4 rd GND BIT ({01} pw=200n lt=100n ht=100n)

v5 ctrl GND BIT ({01} pw=200n lt=100n ht=100n)

v6 wl1 GND BIT ({11} pw=200n lt=100n ht=100n)

v7 rd1 GND BIT ({01} pw=200n lt=100n ht=100n)

v8 ctrl1 GND BIT ({01} pw=200n lt=100n ht=100n)

v9 clk GND BIT ({11} pw=200n lt=100n ht=100n)

v10 bl0 GND BIT ({10} pw=200n lt=100n ht=100n)

v11 wl2 GND BIT ({11} pw=200n lt=100n ht=100n)

v12 wl3 GND BIT ({11} pw=200n lt=100n ht=100n)

v13 sae GND BIT ({11} pw=200n lt=100n ht=100n)

v14 ymux GND BIT ({00} pw=200n lt=100n ht=100n)

.power vs 0n 100n

.print tran v(r/w) v(din) v(bl0) v(dout)

**Array 2\*2 using 6T (ref:cell20)**

.tran 10n 2000n

vs vdd GND 2.5

v1 r/w GND BIT ({01} pw=200n lt=100n ht=100n)

v2 din GND BIT ({11} pw=200n lt=100n ht=100n)

v3 a0 GND BIT ({11} pw=200n lt=100n ht=100n)

v4 wl0 GND BIT ({11} pw=200n lt=100n ht=100n)

v5 wl1 GND BIT ({11} pw=200n lt=100n ht=100n)

v6 clk GND BIT ({11} pw=200n lt=100n ht=100n)

v7 bl0 GND BIT ({10} pw=200n lt=100n ht=100n)

v8 b0 GND BIT ({10} pw=200n lt=100n ht=100n)

.power vs 0n 100n

.print tran v(r/w) v(din) v(bl0) v(dout)

**Array 4\*4 using 6T(ref : cell 22)**

.tran 10n 2000n

vs vdd GND 2.5

v1 r/w GND BIT ({01} pw=200n lt=100n ht=100n)

v2 din GND BIT ({11} pw=200n lt=100n ht=100n)

v3 wl0 GND BIT ({11} pw=200n lt=100n ht=100n)

v4 wl1 GND BIT ({11} pw=200n lt=100n ht=100n)

v5 clk GND BIT ({11} pw=200n lt=100n ht=100n)

v6 bl0 GND BIT ({10} pw=200n lt=100n ht=100n)

v7 wl2 GND BIT ({11} pw=200n lt=100n ht=100n)

v8 wl3 GND BIT ({11} pw=200n lt=100n ht=100n)

.power vs 0n 100n

.print tran v(r/w) v(din) v(bl0) v(dout)

**Array 2 using sense amp(6T) (ref : cell 23)**

.tran 10n 2000n

vs vdd GND 5

v1 r/w GND BIT ({01} pw=200n lt=100n ht=100n)

v2 din GND BIT ({11} pw=200n lt=100n ht=100n)

v3 a0 GND BIT ({11} pw=200n lt=100n ht=100n)

v4 wl0 GND BIT ({11} pw=200n lt=100n ht=100n)

v5 clk GND BIT ({11} pw=200n lt=100n ht=100n)

v6 bl0 GND BIT ({10} pw=200n lt=100n ht=100n)

v7 b0 GND BIT ({10} pw=200n lt=100n ht=100n)

v8 sae GND BIT ({11} pw=200n lt=100n ht=100n)

v9 ymux GND BIT ({00} pw=200n lt=100n ht=100n)

.power vs 0n 100n

.print tran v(r/w) v(bl0) v(out) v(sae)v(dout)

**Array4 using sense amp(6T) (ref : cell 24)**

.tran 10n 2000n

vs vdd GND 2.5

v1 r/w GND BIT ({01} pw=200n lt=100n ht=100n)

v2 din GND BIT ({11} pw=200n lt=100n ht=100n)

v3 wl0 GND BIT ({11} pw=200n lt=100n ht=100n)

v4 wl1 GND BIT ({11} pw=200n lt=100n ht=100n)

v5 clk GND BIT ({11} pw=200n lt=100n ht=100n)

v6 bl0 GND BIT ({10} pw=200n lt=100n ht=100n)

v7 wl2 GND BIT ({11} pw=200n lt=100n ht=100n)

v8 wl3 GND BIT ({11} pw=200n lt=100n ht=100n)

v9 sae GND BIT ({11} pw=200n lt=100n ht=100n)

v10 ymux GND BIT ({00} pw=200n lt=100n ht=100n)

v11 a0 GND BIT ({11} pw=200n lt=100n ht=100n)

v12 b0 GND BIT ({10} pw=200n lt=100n ht=100n)

.power vs 0n 100n

.print tran v(r/w) v(din) v(bl0) v(dout)