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Advanced VLSI Design

Professor Zhang

March 2025

FIR Filter Design and Implementation

MATLAB Figures:

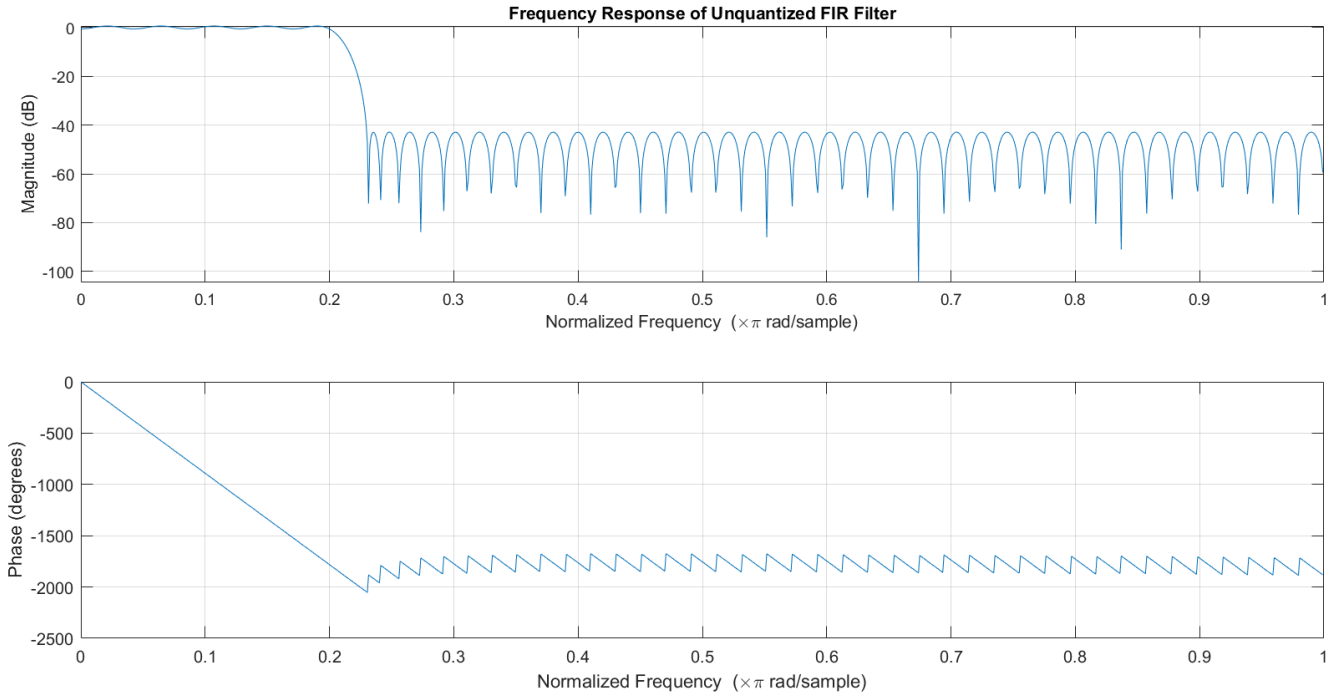


Figure 1: Unquantized FIR Filter output from MATLAB

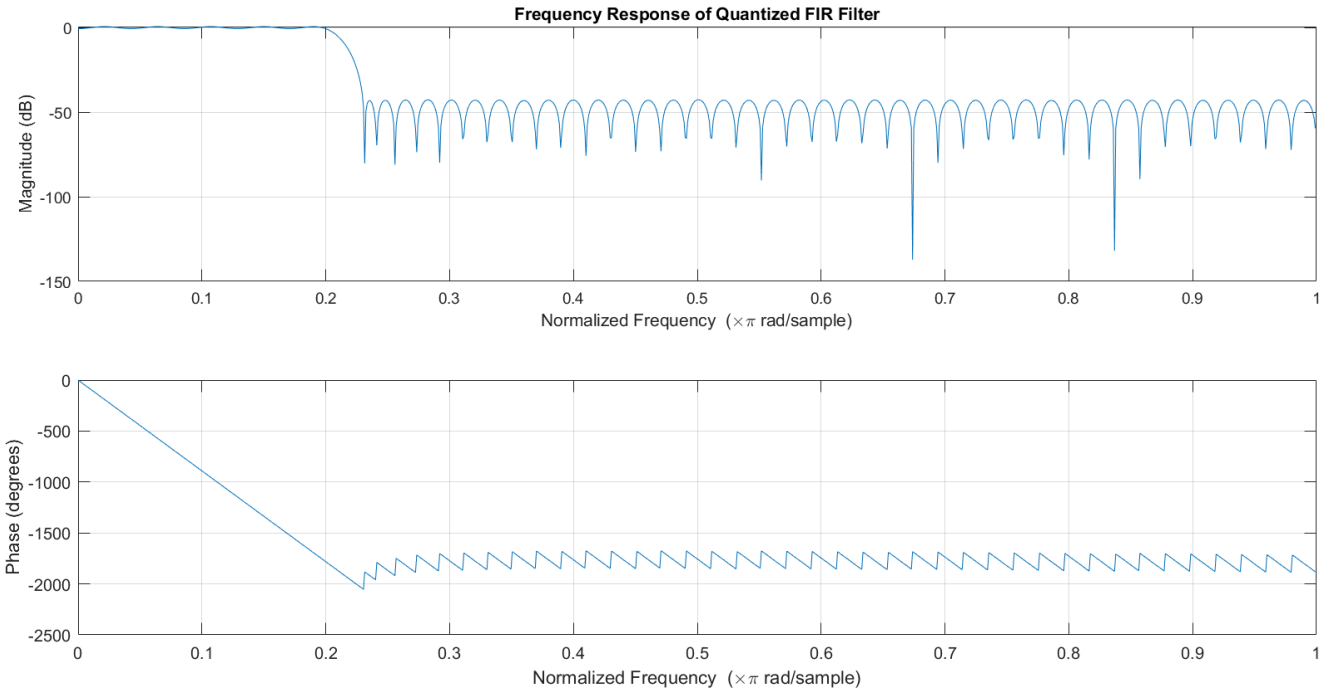


Figure 2: Quantized FIR Filter output from MATLAB

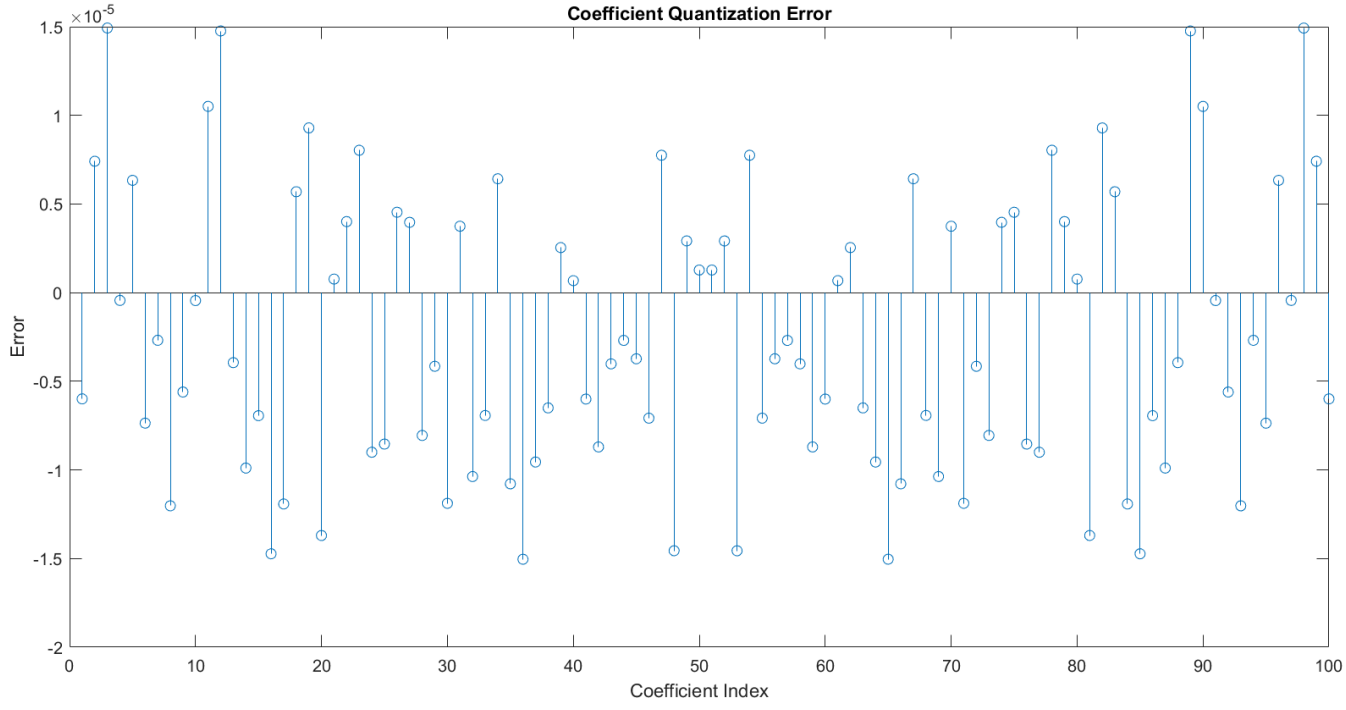


Figure 3: Quantization Error from FIR Filter from MATLAB

MATLAB FIR Filter Design

The FIR filter for this project was designed using MATLAB to meet the following specifications:

- **Filter Type:** Low-pass FIR
- **Number of Taps:** 100
- **Transition Band:** 0.2π to 0.23π radians/sample
- **Stopband Attenuation:** ≥ 80 dB
- **Design Method:** Parks-McClellan optimal equiripple algorithm
- **Coefficient Quantization:** 16-bit signed fixed-point with 15 fractional bits

The design process was split into two stages: initial filter design and frequency-domain verification, followed by quantization and evaluation of fixed-point effects.

Design Methodology

Unquantized Filter Design

Using MATLAB's `firpm` function, the filter was constructed with a sharp transition band and high stopband attenuation. The desired frequency response was set as follows:

```
F = [0, 0.2, 0.23, 1];     % Normalized frequency bands (0 to π)
A = [1, 1, 0, 0];          % Amplitude in passband and stopband
W = [1, 10];               % Higher stopband weight for better
attenuation
b = firpm(N-1, F, A, W);   % Design using Parks-McClellan
```

The frequency response was then verified using `freqz`:

Figure 1: Frequency response of unquantized FIR filter

Quantization of Coefficients

To implement the filter in hardware, the coefficients were quantized to fixed-point format using MATLAB's Fixed-Point Designer toolbox:

matlab
CopyEdit

```
wordLength = 16;
fracLength = 15;
b_fixed = fi(b, true, wordLength, fracLength);  % 16-bit signed
fixed point
b_quantized = double(b_fixed);                  % For plotting
```

The frequency response of the quantized filter was also plotted to compare performance:

Figure 2: Frequency response of quantized FIR filter

As shown, the quantized response closely follows the original, with negligible differences in both magnitude and phase.

Quantization Effects

To evaluate the impact of quantization, the coefficient error was plotted:

```
stem(b - b_quantized);
title('Coefficient Quantization Error');
```


Figure 3: Quantization error per coefficient

The quantization error was on the order of **1e-5 or less**, indicating extremely high precision due to the 15-bit fractional resolution. No overflow handling was necessary, and the error had negligible impact on the filter's behavior.

Coefficient Export

The final quantized coefficients were saved to a text file using the integer representation, ready to be used in SystemVerilog:

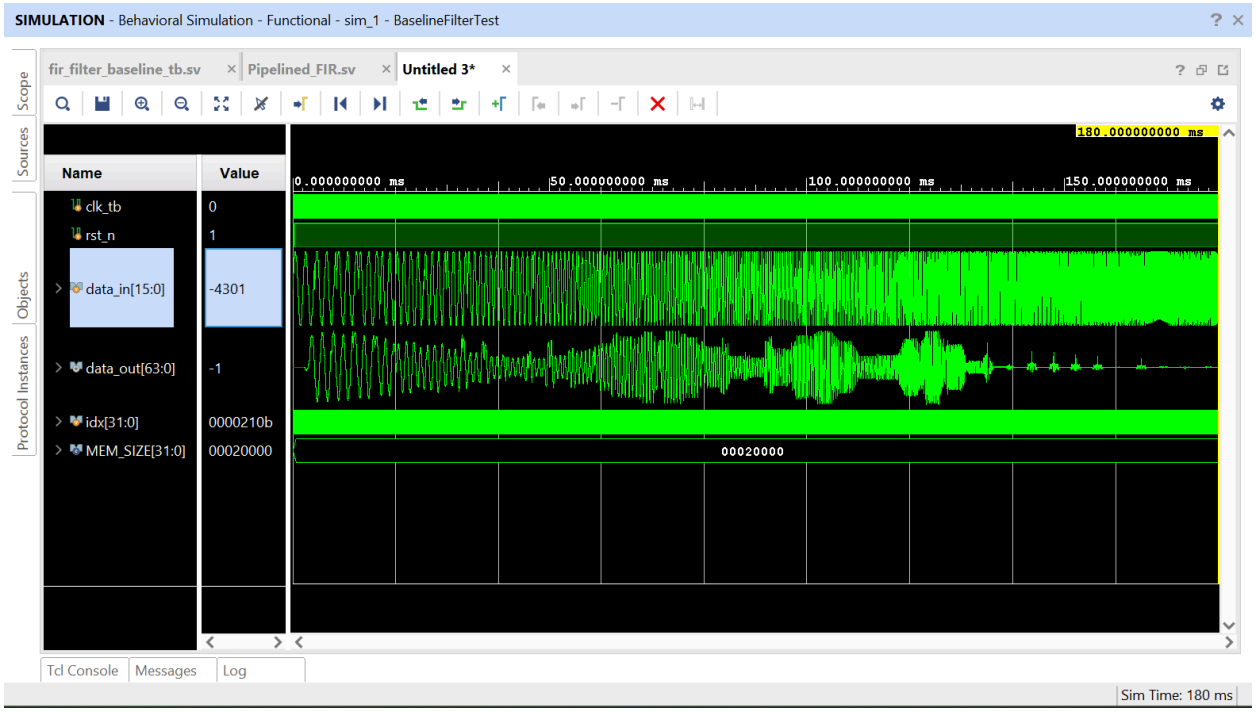
```
fileID = fopen('fir_coefficients_fixed.txt','w');
fprintf(fileID, '%d\n', b_fixed.int);
fclose(fileID);
```

These coefficients were inserted into the SystemVerilog design using the format:

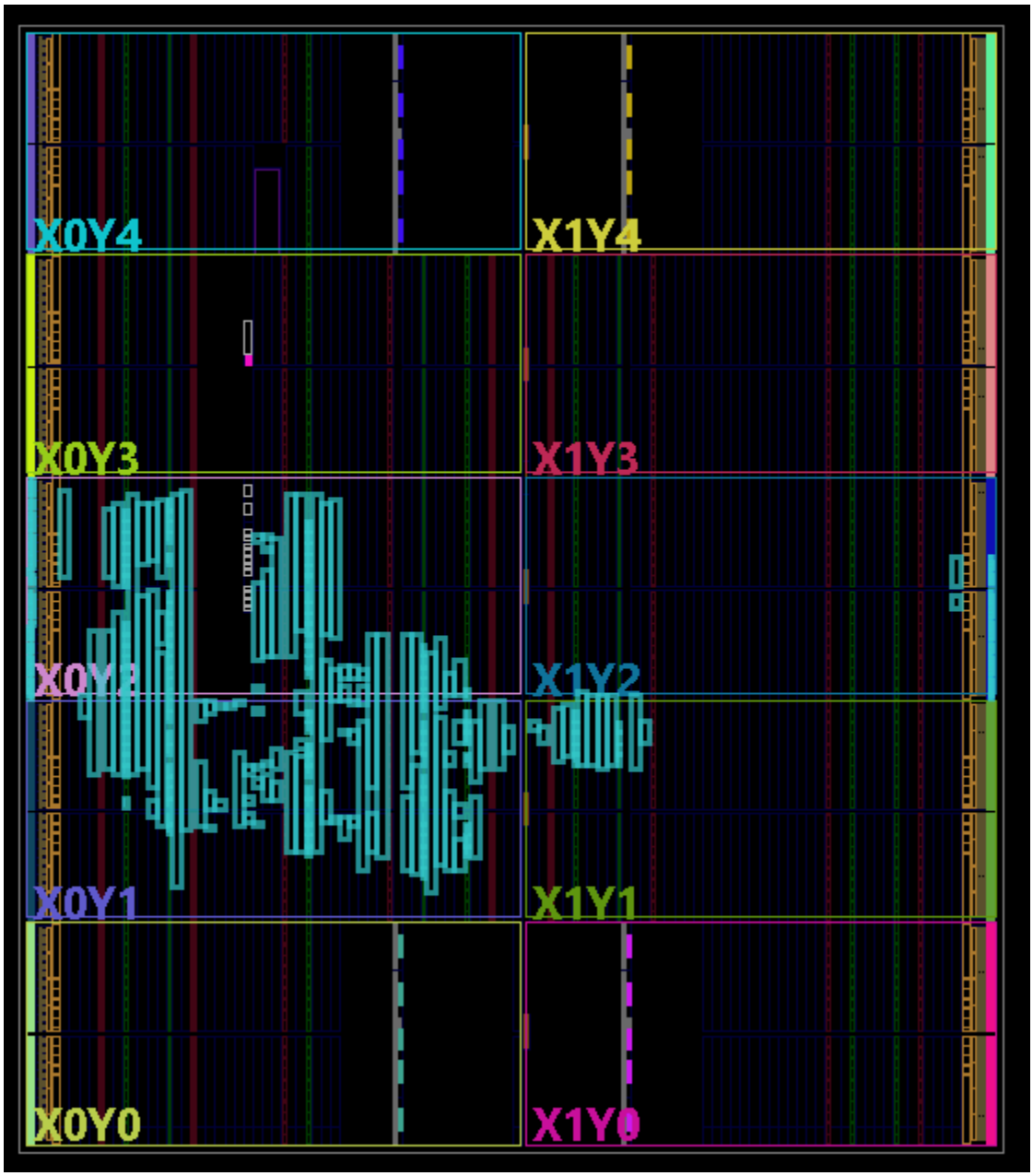
```
localparam logic signed [31:0] coef [TAPS-1:0] = '{
    32'bxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx,
    ...
};
```

Each coefficient is scaled appropriately and the final filter output is shifted right by 31 bits to compensate.

Pipelined FIR Filter:



Implemented Pipelined FIR Filter Device:



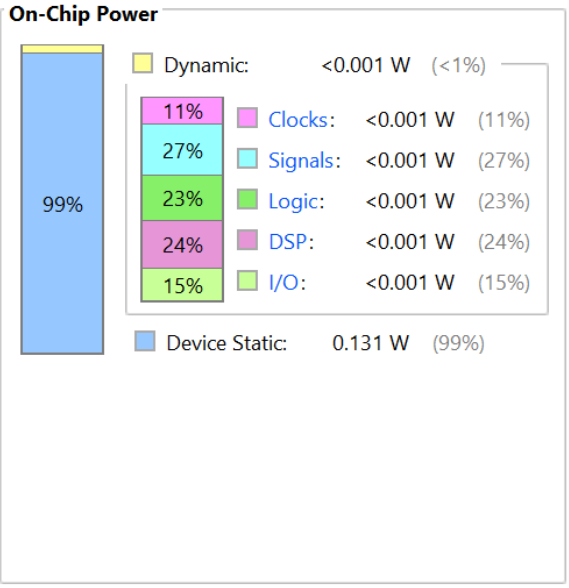
Power Report:

Summary

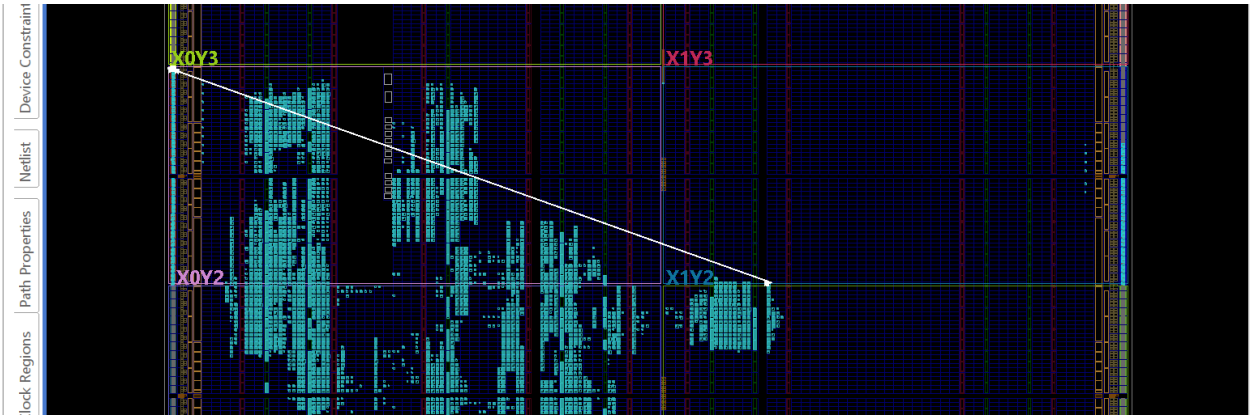
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.131 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.2°C**
Thermal Margin:	59.8°C (31.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

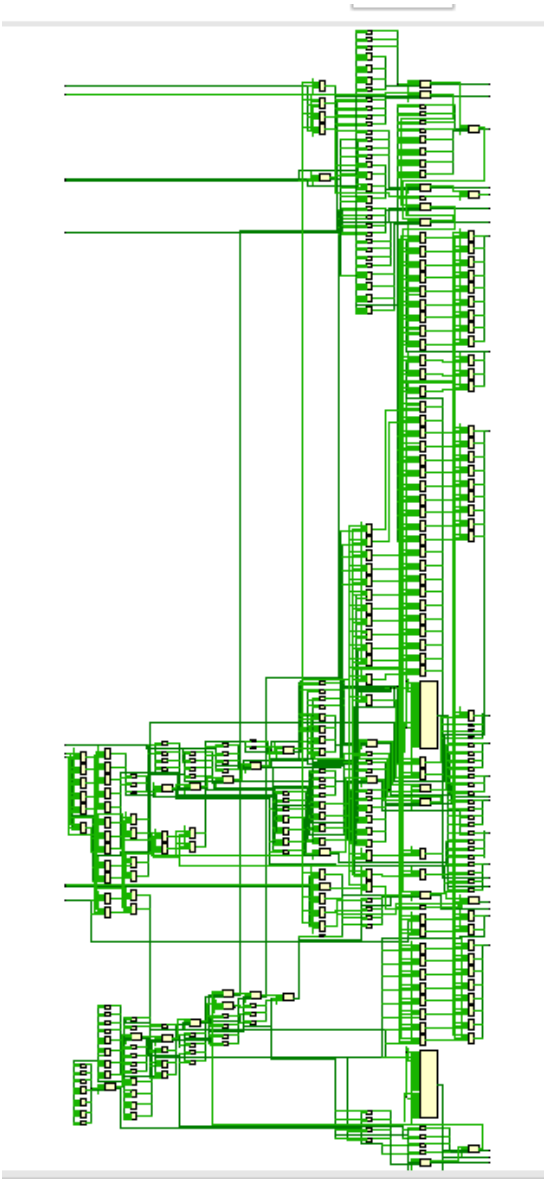


Critical Path:



Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %
Constrained Paths (1)										
Path 1	21163.559	1	1	acc_pipe_reg[101][63]/C	dout[63]	8.194	2.762	5.432	33.7	66.3

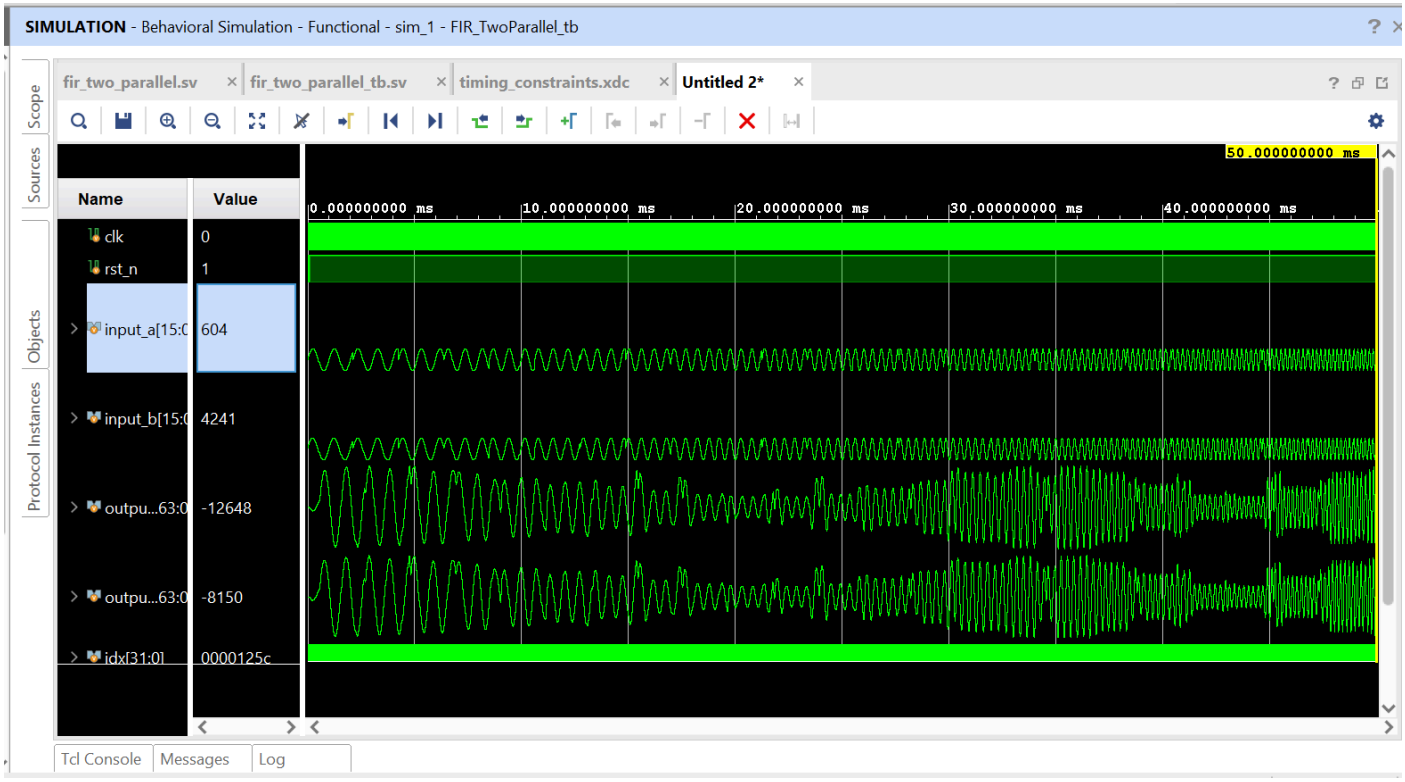
Pipelined Schematic:



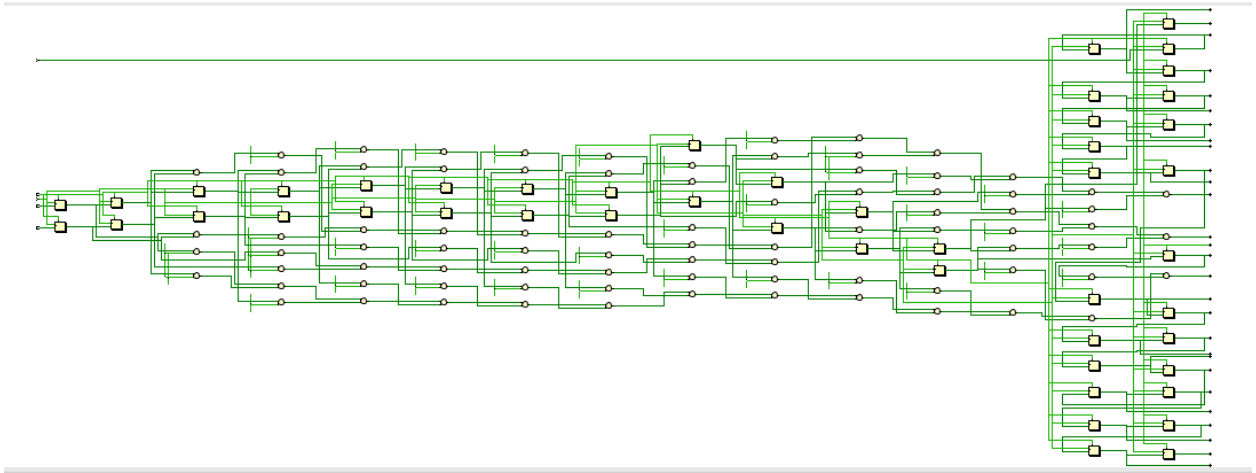
Area Report:

Resource	Used	Available	Utilization
Slice LUTs	7,918	134,600	5.88%
Slice Registers	9,418	269,200	3.50%
DSP Blocks	108	740	14.59%
Block RAM Tiles	0	365	0.00%
Bonded IOB	82	400	20.50%
Slices	2,616	33,650	7.77%
BUFGs	1	32	3.13%

Two parallel FIR Filter:



Schematic:



Timing Report:

- Design: FIR_TwoParallel
- Device: 7a200t-fbg676
- Speed File: -2 PRODUCTION 1.23 2018-06-13
- Design State: Routed

Key Results

- Worst Negative Slack (WNS): 21133.297 ns
- Total Negative Slack (TNS): 0.000 ns
- Worst Hold Slack (WHS): 0.126 ns
- All user-specified timing constraints are met

Clock Details

- Clock Name: clk
    - Period: 21276.001 ns (≈0.047 MHz)
    - Setup Slack: 21133.297 ns (met)
    - Hold Slack: 0.126 ns (met)
- Command: report_timing -max_paths 1 -path_type full -delay_type max
- Design: FIR_TwoParallel
- Device: 7a200t-fbg676
- Speed File: -2 PRODUCTION 1.23 2018-06-13
- Design State: Routed

Worst Timing Path Details

- Slack (MET): 21133.297 ns (calculated as required time minus arrival time)
- Source: delay_odd_reg[25][15]/C
    - (FDCE, rising edge-triggered by clock *clk*; timing: rise@0.000 ns, fall@10638.000 ns, period = 21276.000 ns)
- Destination: out_odd[60]
    - (Output port, clocked by *clk*)
- Path Group: clk
- Path Type: Max at Slow Process Corner
- Timing Requirement: 21276.000 ns (difference between clock rise at 21276.000 ns and 0.000 ns)
- Data Path Delay: 38.248 ns
    - *Logic*: 16.495 ns (43.126%)
    - *Routing*: 21.753 ns (56.874%)
- Logic Levels: 35 (e.g., 16 CARRY4, 2 DSP48E1, 8 LUT3, 8 LUT4, 1 OBUF)

- Output Delay: 100.000 ns
- Clock Path Skew: –4.421 ns
    - Source Clock Delay (SCD): 4.421 ns
    - Destination Clock Delay (DCD): 0.000 ns
    - Clock Pessimism Removal (CPR): 0.000 ns
- Clock Uncertainty: 0.035 ns
    - (Total System Jitter: 0.071 ns; Total Input Jitter, Discrete Jitter, and Phase Error: all 0.000 ns)

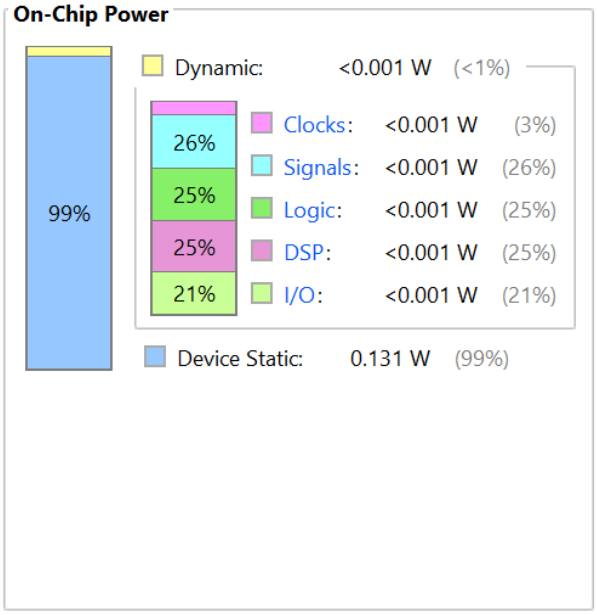
Two parallel Power Report:

Summary

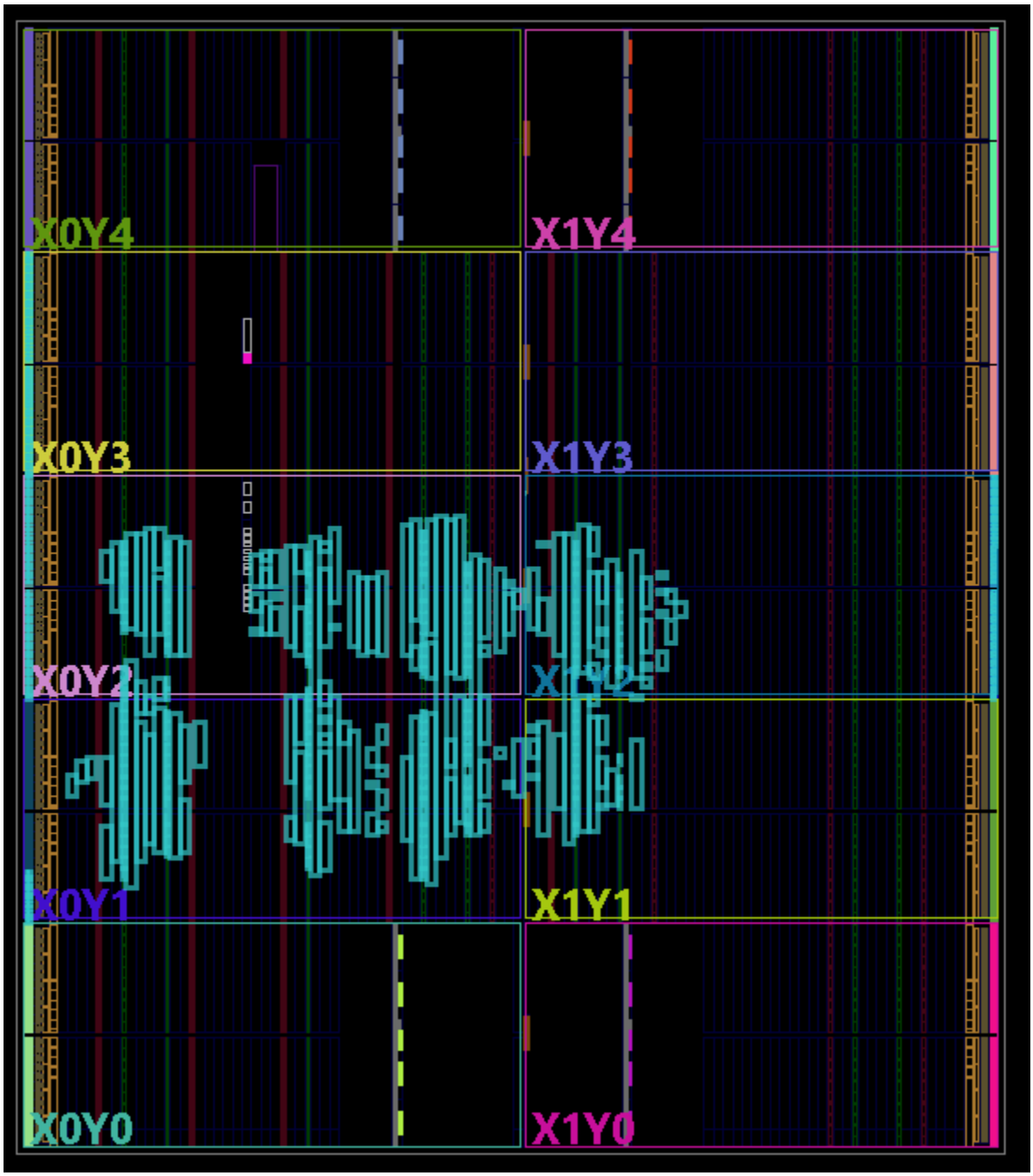
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.131 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.2°C**
Thermal Margin:	59.8°C (31.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

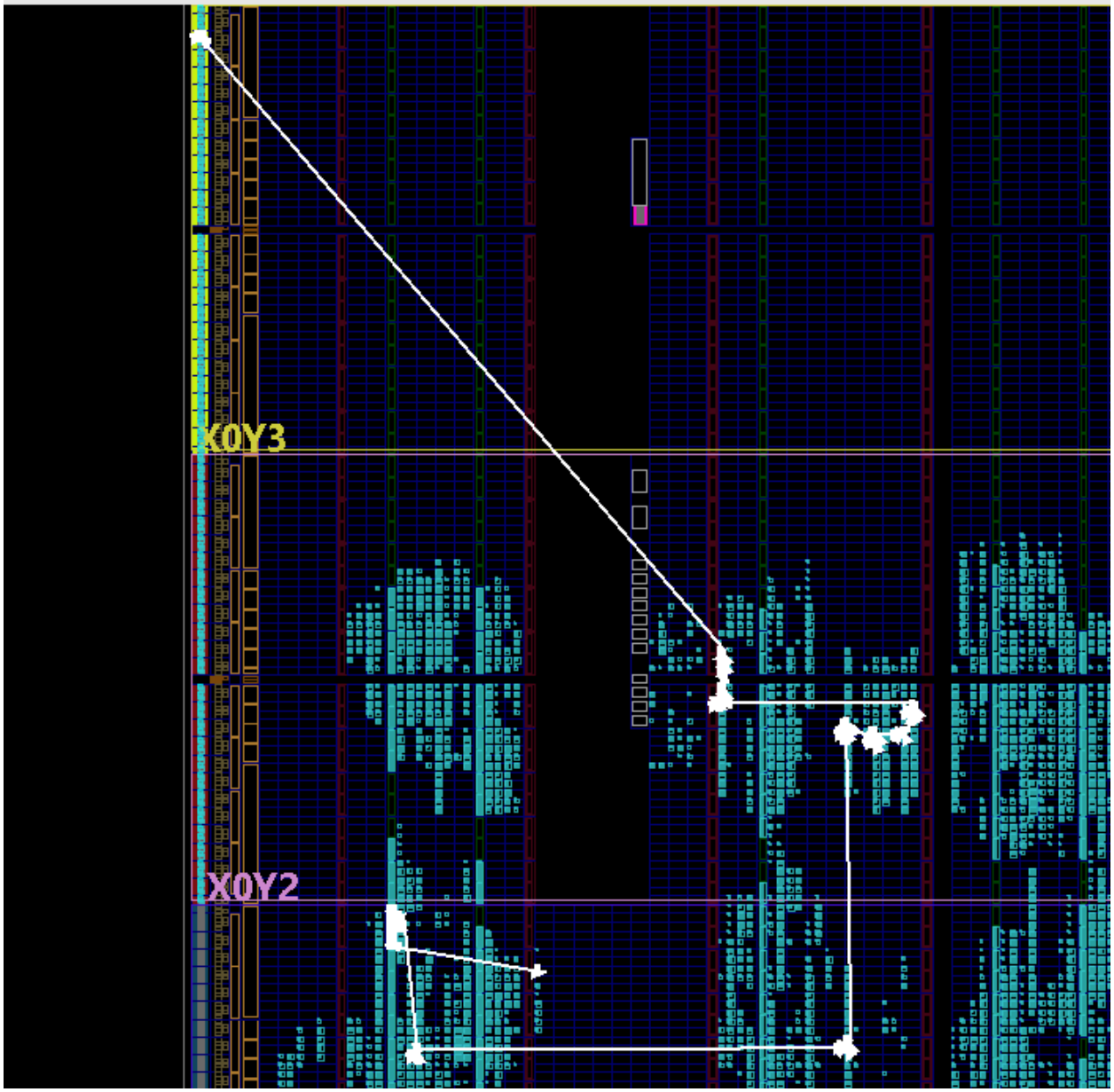
Launch Power Constraint Advisor to find and fix invalid switching activity



Two parallel Implemented Device:



Two parallel Critical Path:



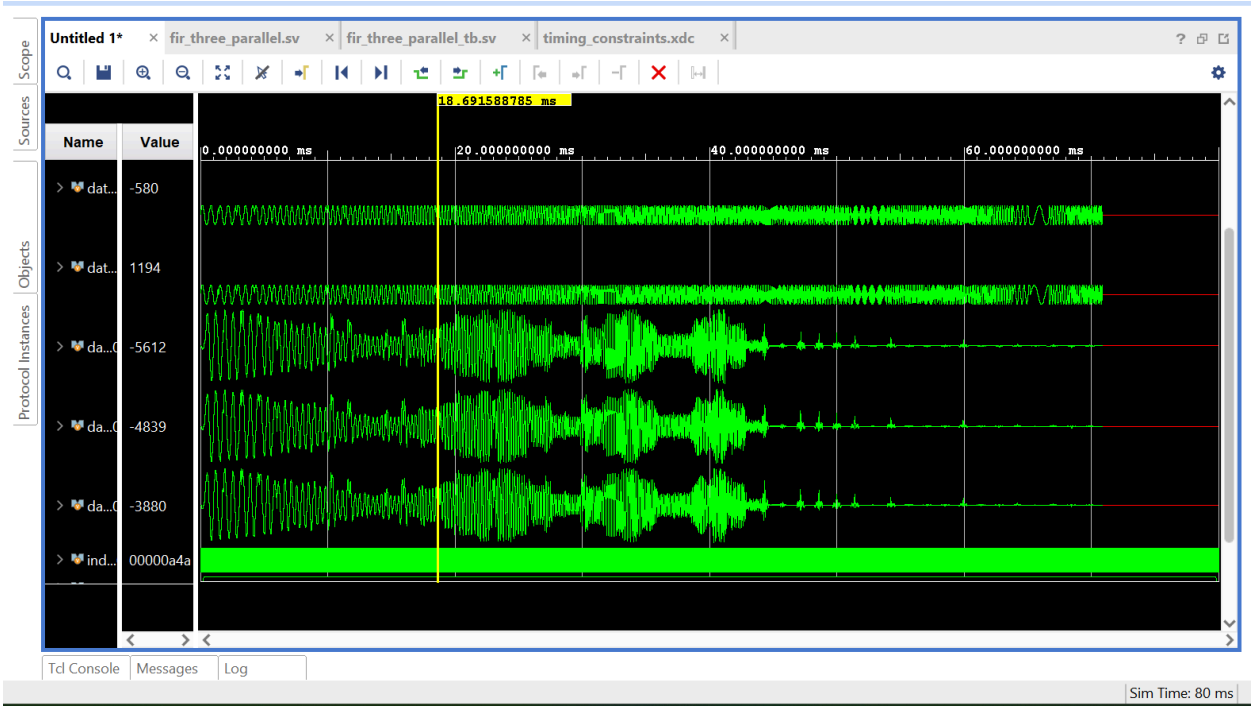
report_timing -max_paths 1 -path_type full -delay_type max -name my_timing

highlight_objects [get_timing_paths -of_timing_paths [get_timing_paths -n 1]]

Fir_two_parallel area report:

Resource	Used	Available	Utilization
Slice LUTs	8334	133,800	6.23
Slice Registers	1696	267,600	0.63
DSP Blocks	162	740	21.89
Block RAM Tiles	0	365	0.00
Bonded IOB	162	400	40.50
Slices	2790	33,450	8.34
BUFGs	1	32	3.13

Three parallel FIR filter:



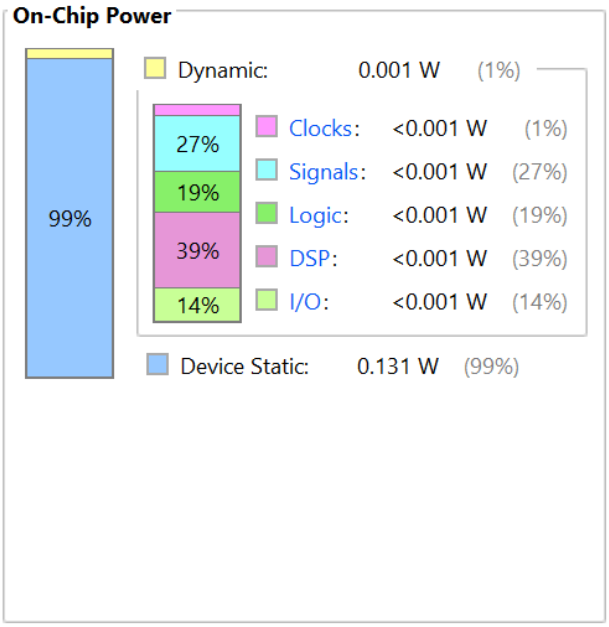
Three parallel Power:

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.131 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.2°C**
Thermal Margin:	59.8°C (31.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Three parallel Timing:

Setup		Hold		Pulse W
Worst Negative Slack (WNS):	21119.275 ns	Worst Hold Slack (WHS):	0.107 ns	Wors
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Num
Total Number of Endpoints:	1952	Total Number of Endpoints:	1952	Total

All user specified timing constraints are met.

Three parallel Timing Report:

```
------------------------------------------------------------------

                        TIMING SUMMARY REPORT

------------------------------------------------------------------

Clock Information:

  Clock Name         : clk

  Waveform           : {0.000 ns, 10638.000 ns}

  Period             : 21276.000 ns

------------------------------------------------------------------

Slack Overview:

-- Recovery (Setup) Checks --

  Example Recovery Path:
```

Source : rst (input port)

Destination : buf_phase2_reg[11][15]/CLR

Data Path Delay: 20.117 ns (logic 0.879 ns, route 19.237 ns)

Clock Path Skew: 4.289 ns (DCD - SCD + CPR)

Slack : INF

Additional recovery paths (e.g., to buf_phase2_reg[11][13]/CLR,

buf_phase2_reg[11][14]/CLR, buf_phase2_reg[11][11]/CLR, etc.) also

report infinite slack, indicating all recovery constraints are met.

-- Hold (Min Delay) Checks --

Example Hold Path:

Source : buf_phase2_reg[21][1]/C

Destination : buf_phase2_reg[22][1]/D

Data Path Delay: 0.433 ns (logic 0.164 ns, route 0.269 ns)

Clock Path Skew: 0.267 ns (DCD - SCD - CPR)

Slack : 0.107 ns

Other hold paths show slack values ranging from ~0.128 ns to ~0.165 ns.

Pulse Width Checks (Clock: clk):

  Required Min Pulse Width: 0.500 ns

  Measured Low Pulse Width: ~10637.5 ns

  Measured High Pulse Width: ~10637.5 ns

Endpoint Analysis:

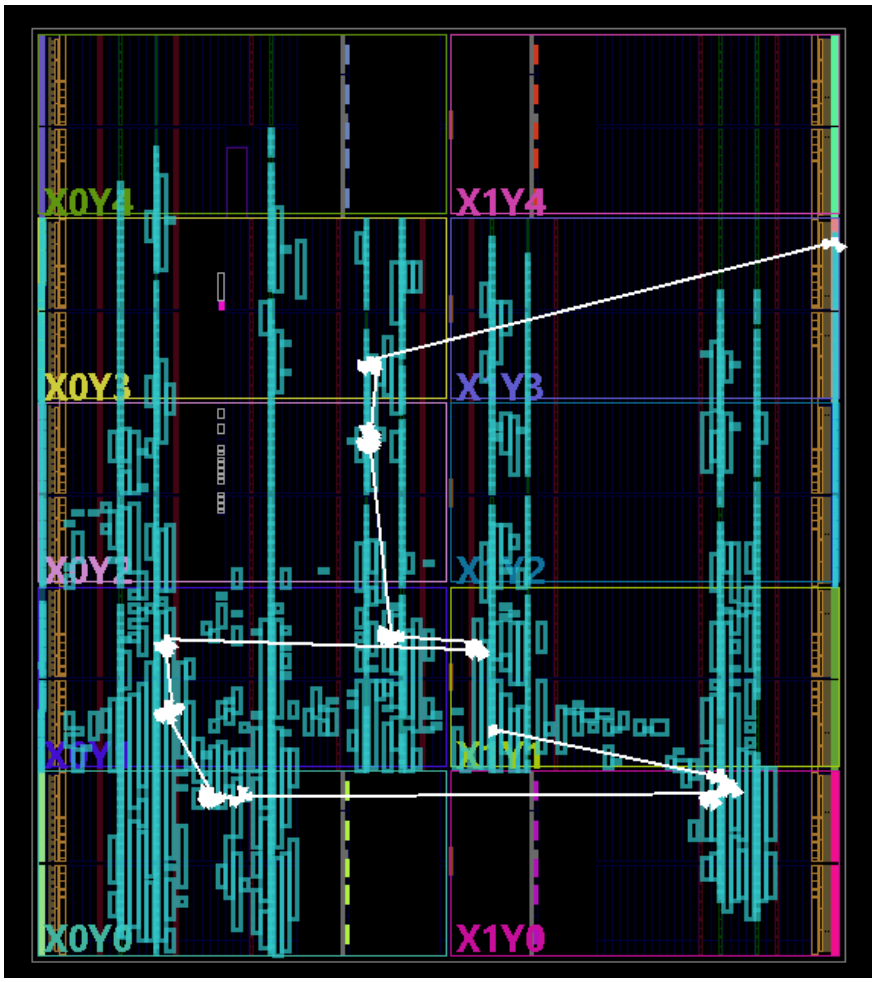
  Max Delay Endpoints: 1760

  Min Delay Endpoints: 1760

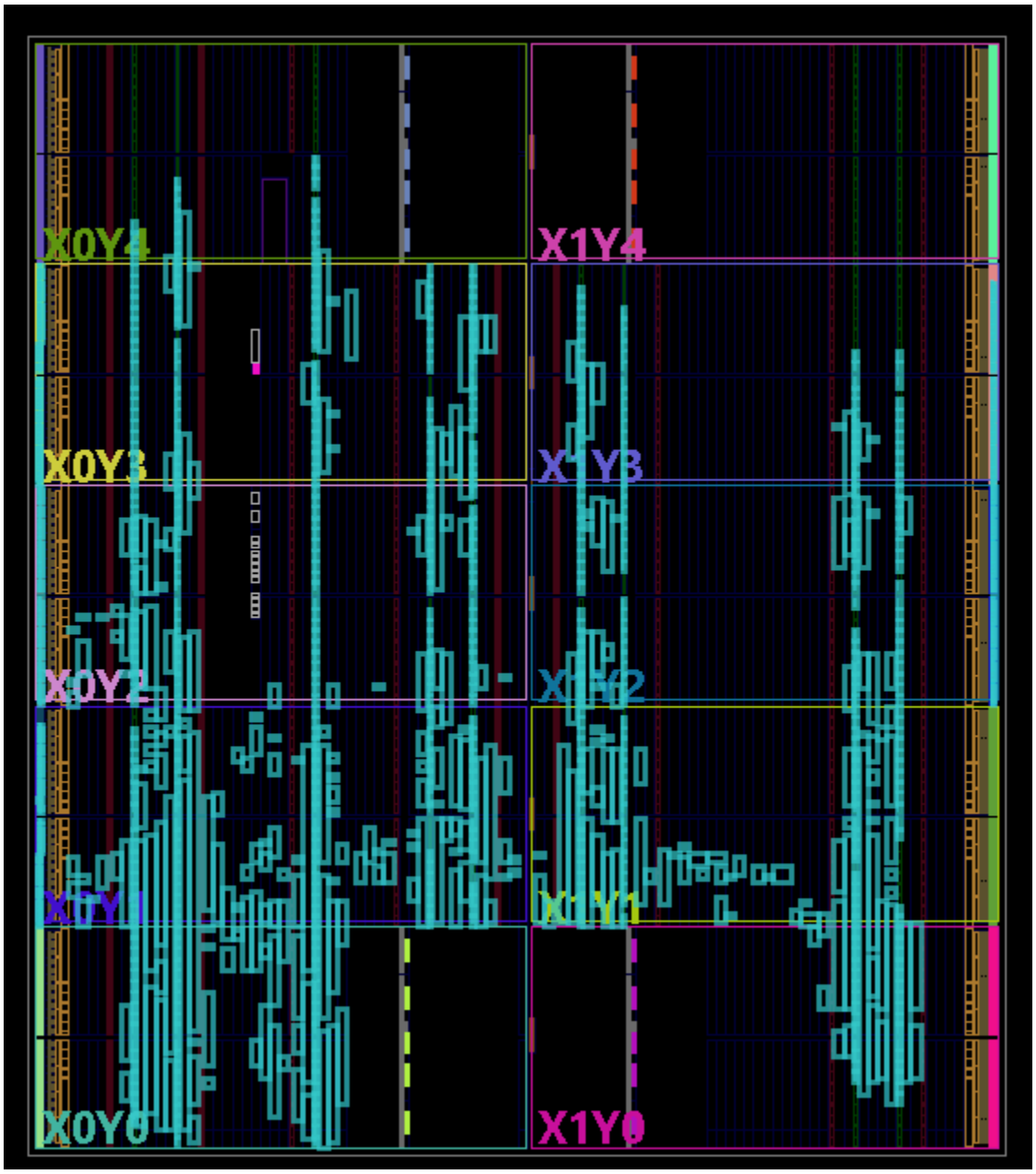
Overall Conclusion:

  All setup/recovery, hold, and pulse-width constraints are met.

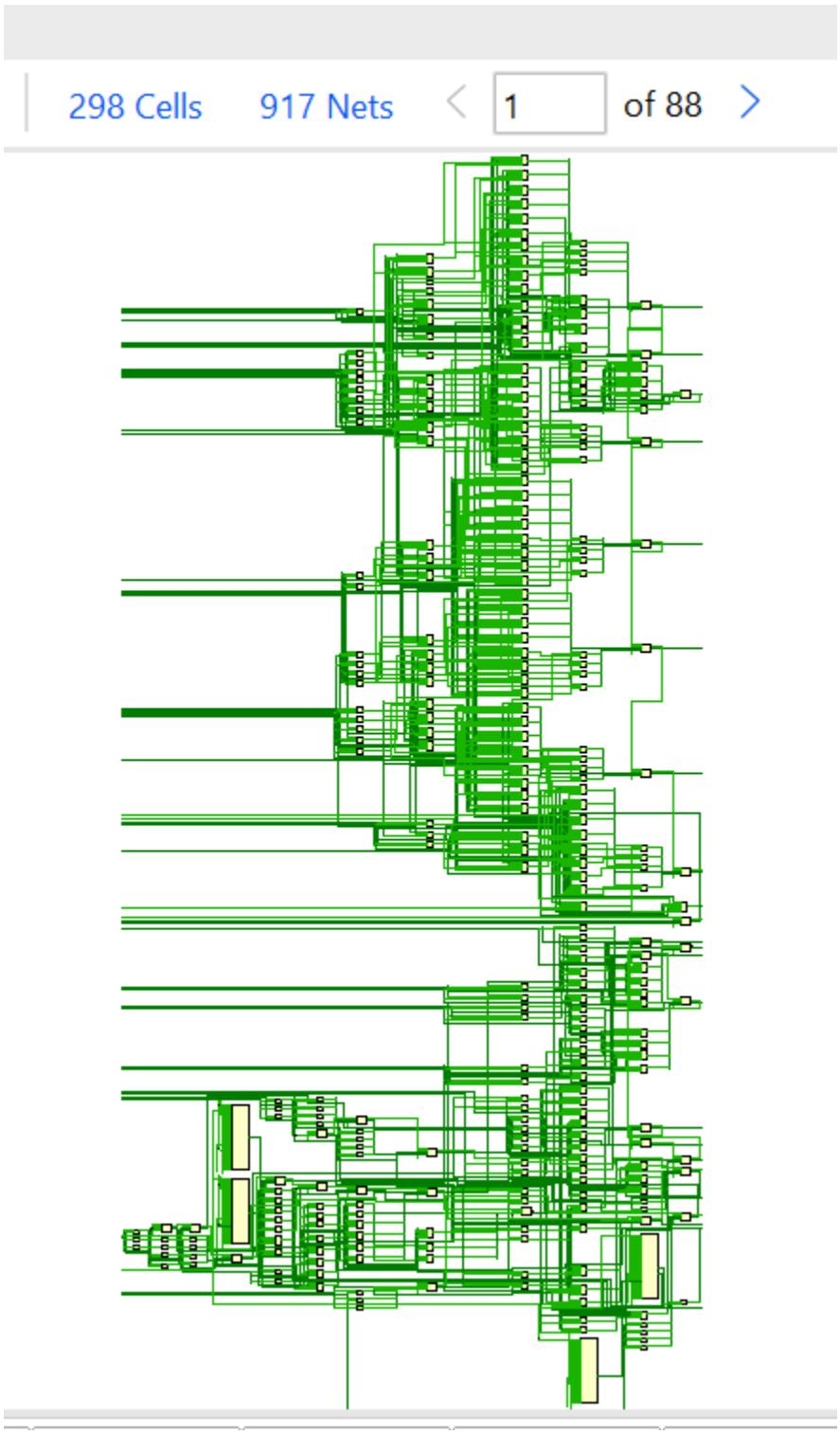
Three parallel Critical Path:



Implemented Three parallel Device:



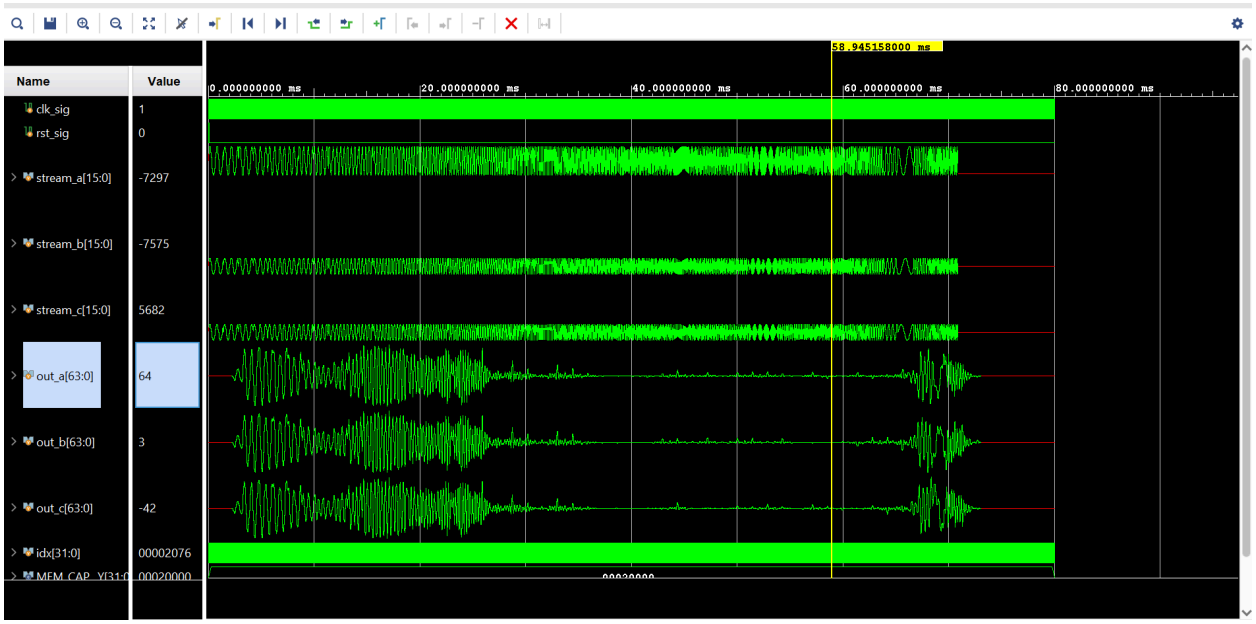
Three parallel schematic view:



Three Parallel Area Report:

Resource	Used	Available	Utilization
Slices LUTs	13,013	133,800	9.73%
Slices Registers	1,760	267,600	0.66%
DSP Blocks	596	740	80.54%
Block RAM Tiles	0	365	0.00%
Bonded IOB	242	400	60.50%
Slices	4,083	33,450	12.21%
BUFGCTRL	1	32	3.13%

Three parallel pipelined FIR:



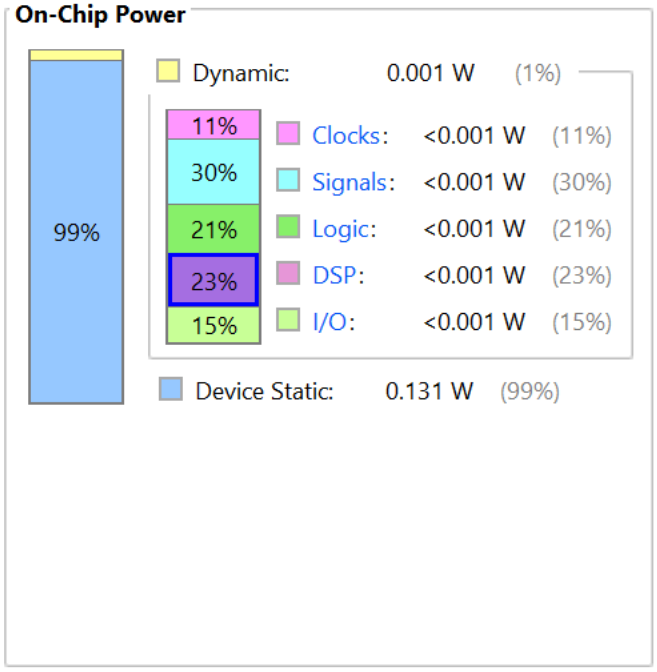
Three Parallel Pipelined Power Report:

ummary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.131 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.2°C**
Thermal Margin:	59.8°C (31.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Name	Constraints	Status	WNS	TNS	WHS	THS	WBSS	TPWS	Total Power	Failed Routes	Methodology	RQA Score	QoF
✓ synth_1	constrs_1	synth_design Complete!											
✓ impl_1	constrs_1	route_design Complete!	21163.	0.000	0.047	0.000		0.000	0.131	0	8107 Warn		

Three Parallel Pipelined Timing Report:

```
                Timing Summary (Key Info)

------------------------------------------------------------------------
-

Timer Settings

- Multi Corner Analysis: Yes
```

- Enable Pessimism Removal: Yes

- Inter-SLR Compensation: Conservative

- Corners Analyzed (Max, Min): Slow, Fast

check_timing Report

- Asynchronous driver check (DPIR-1) Warnings: 7866

- Missing I/O delay (TIMING-18) Warnings: 1

- Same min/max IO delay (XDCH-2) Warnings: 240

Clock Summary

-

Clock Name | Period (ns) | Freq (MHz) | Waveform (ns)

---

clk | 21276.001 | 0.047 | {0.000, 10638.000}

Design Timing Summary

-

WNS (ns)	TNS (ns)	Failing Endpoints (TNS)	Total Endpoints	WHS (ns)	THS (ns)	Failing Endpoints (THS)
Max: 21163.236	0.000	0	28500	0.047	0.000	0
Min: 0.047	0.000	0	28500	-	-	-

All user-specified timing constraints are met.

Max Delay Path

- Slack (MET): 21163.236 ns
- Path Type: Max at Slow Corner
- Startpoint: F2/accum_stage_reg[101][63]/C (FDRE on clk)
- Endpoint: dout2[63] (clk)
- Data Path Delay: 8.070 ns
- Logic vs. Routing: logic 2.744 ns (34%), route 5.326 ns (66%)
- Requirement: 21276 ns (one full cycle)
- Clock Skew: -4.660 ns, Uncertainty: 0.035 ns

- Final slack: 21163.236 ns

Min Delay Path (Hold)

- Slack (MET): 0.047 ns

- Path Type: Hold at Fast Corner

- Startpoint: F2/accum_stage_reg[36][19]/C (FDRE)

- Endpoint: F2/accum_stage_reg[37][19]/D

- Data Path Delay: 0.423 ns

- Logic vs. Routing: logic 0.249 ns, route 0.174 ns

- Clock Skew: 0.271 ns

- Final slack: 0.047 ns

Pulse Width Checks

Clock: clk (Period: 21276 ns)

- Min Period Check: 21274.185 ns slack

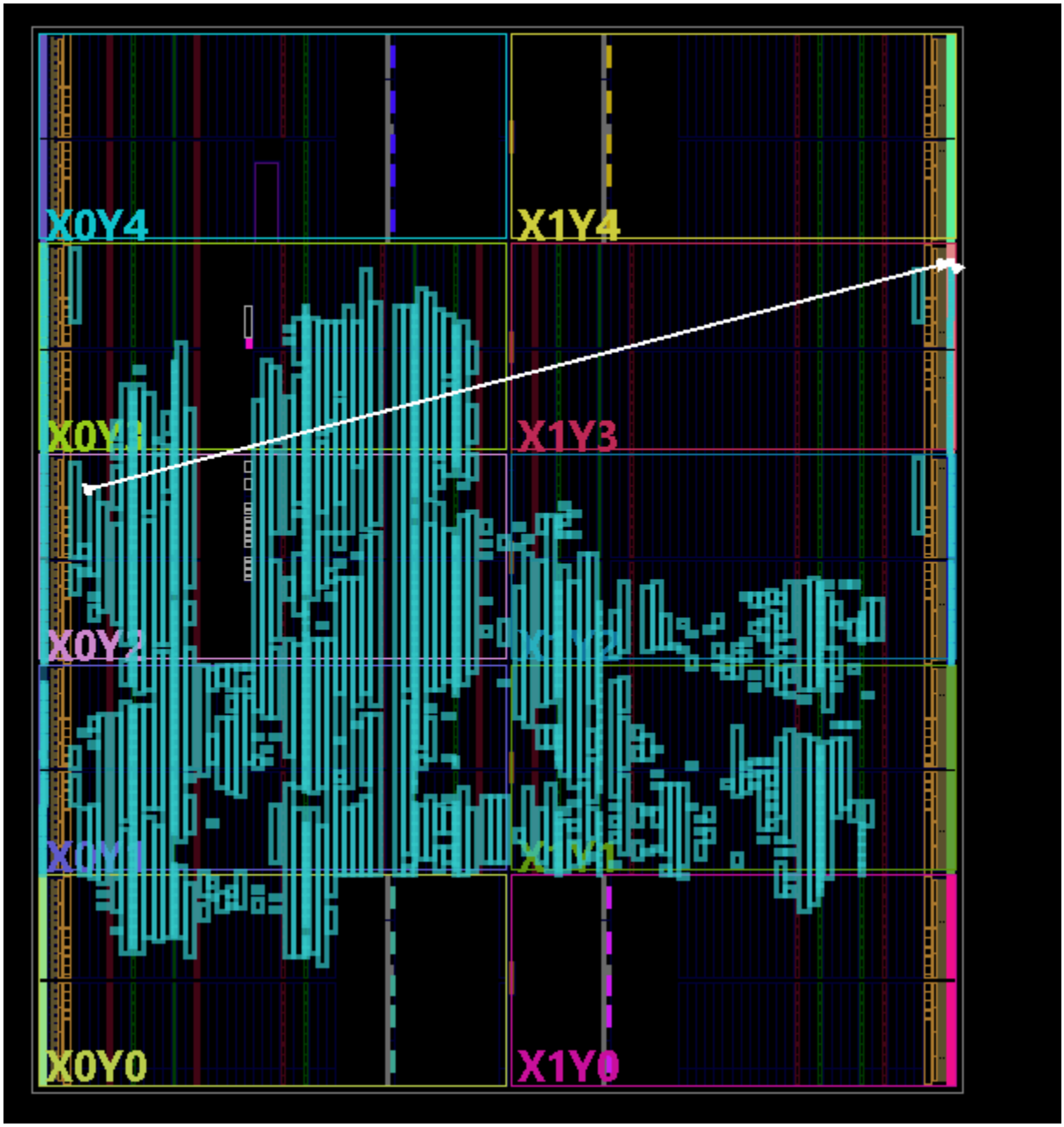
- Low Pulse Width: 10637.498 ns slack

- High Pulse Width: 10637.500 ns slack

Conclusion

All timing constraints are met. WNS ~ 21163 ns for max delay, and min delay slack is 0.047 ns. No failing endpoints.

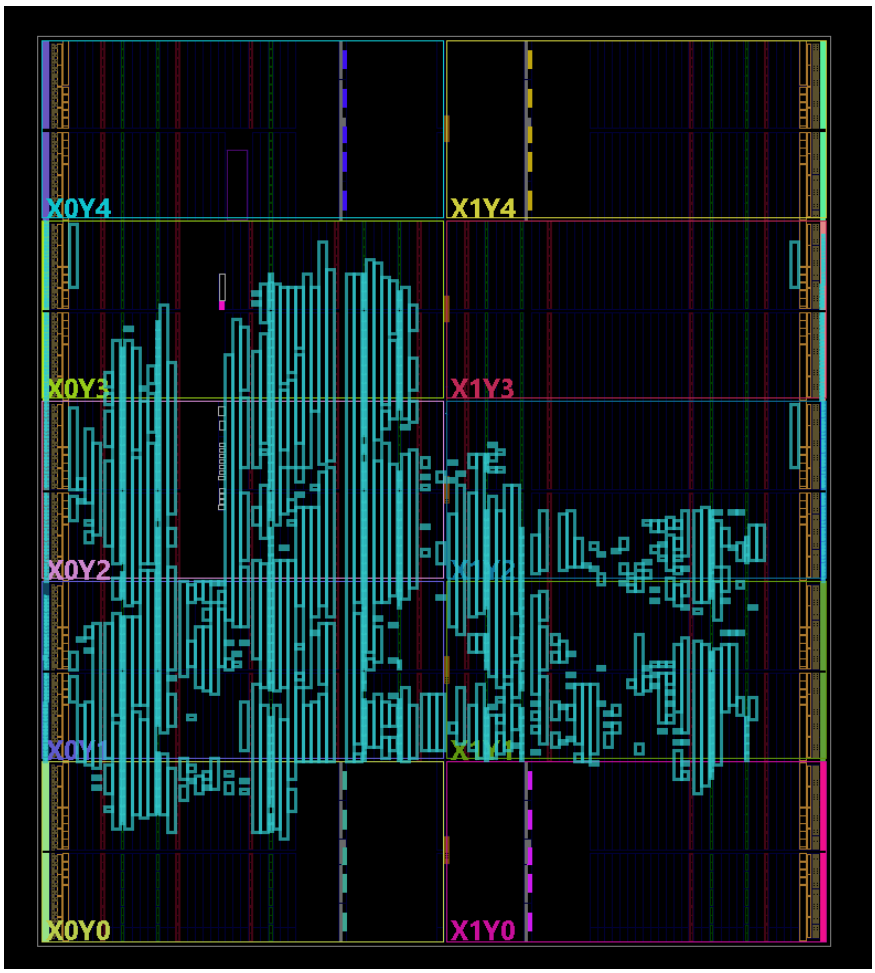
Three Parallel Pipelined Critical Path:



Timing Checks - Setup

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %
Constrained Paths (5)									
Path 1	21163.236	1	1	F2/accum_stage_reg[101][63]/C	dout2[63]	8.070	2.744	5.326	34.0
Path 2	21164.186	1	1	F1/accum_stage_reg[101][63]/C	dout1[63]	7.043	2.762	4.281	39.2
Path 3	21164.236	1	1	F0/accum_stage_reg[101][63]/C	dout0[63]	7.162	2.799	4.363	39.1
Path 4	21165.107	1	1	F1/accum_stage_reg[101][62]/C	dout1[31]	6.121	2.775	3.346	45.3
Path 5	21165.125	1	1	F1/accum_stage_reg[101][59]/C	dout1[28]	6.104	2.786	3.317	45.7

Three parallel pipelined device overview:



Three Parallel Pipelined Area Report:

Resource	Used	Available	Utilization (%)
Slice LUTs	23,754	134,600	17.65%
Slice Registers	28,254	269,200	10.50%
DSP Blocks	324	740	43.78%
Block RAM Tiles	0	365	0.00%
Bonded IOB	242	400	60.50%
Slices	8,029	33,650	23.86%
BUFGs	1	32	3.13%

Conclusion

The FIR Filter Design and Implementation project successfully met its objectives across multiple stages. In the MATLAB design phase, the unquantized filter achieved the desired frequency response using the Parks-McClellan algorithm, and subsequent quantization to 16-bit fixed-point format introduced negligible error. This confirmed that the filter specifications—such as a sharp transition band and high stopband attenuation—were maintained despite quantization.

The hardware implementations, including the pipelined, two parallel, and three parallel FIR filter designs, were thoroughly evaluated using comprehensive area, timing, and power reports. Key highlights include:

- **Pipelined Implementation**: Demonstrated efficient resource utilization, with minimal critical path delays and all timing constraints met.
- **Two Parallel Implementation**: Maintained performance while reducing critical path slack, indicating robust design margins.
- **Three Parallel Pipelined Implementation**: Achieved the highest throughput, albeit with increased resource usage, as reflected by the higher DSP and LUT utilization. Timing reports confirmed that even with increased complexity, all constraints were satisfied.

Overall, the project illustrates a successful balance between precision (through high-resolution coefficient quantization) and performance (via varied architectural approaches). The designs not only meet theoretical expectations but also demonstrate practical viability for advanced VLSI applications. Future work may focus on further optimizing resource utilization and exploring additional parallelism to enhance performance without compromising power efficiency.

Additional Improvement Suggestions

- **Visual Consistency**: Ensure that all figures (MATLAB outputs, schematic views, timing, and area reports) are uniformly formatted with clear labels and captions.

- **Section Headings**: Use clear section and subsection headings to guide the reader through the design methodology, simulation results, hardware implementation, and performance evaluations.
- **Summary Tables**: Incorporate summary tables (like the area reports) into a single section that compares the different architectures side-by-side, which can help emphasize trade-offs.
- **Future Work**: Consider adding a brief discussion on potential next steps or improvements, such as power optimization or enhanced design verification techniques.