VeriSilicon
SPDIF Specification

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REV	REVISION HISTORY	DATE
1.0	First initial	2009-09-04
1.1	Add non-linear PCM audio transmit	2009-09-18
1.2	Add non_linear PCM audio receive	2009-11-06
1.2.1	Add HDMI interface	2010-03-23

Contents

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1. GENERAL DESCRIPTION

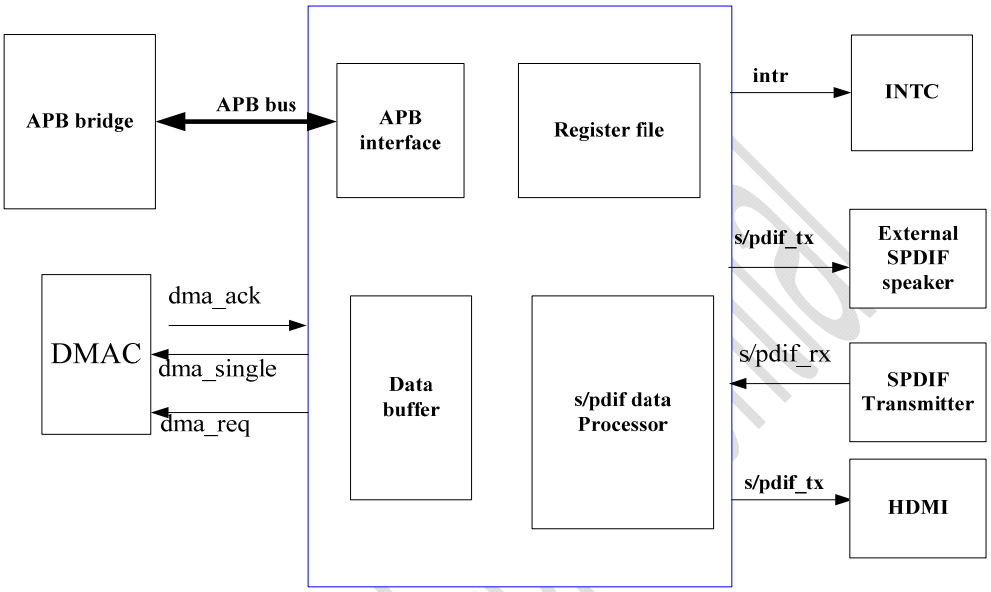
The Sony Philips Digital Interface Format (S/PDIF) is used in many (V)LSI ICs based systems, especially in many digital stereo audio systems. S/PDIF, a standardized communication interface, is vital to both equipment and IC manufacturers because of the increased system flexibility. S/PDIF interface provides a stable way to transmit stereo data with special sampling. S/PDIF interface transmits or receives non-linear PCM stream.

2. FEATURE LIST

- **AMBA 2.0-compliant APB bus interface**
- **Half duplex asynchronous operation**
- **Performs DMA handshake interfacing**
- **The size of embedded FIFO is 32x16 bit**
- **SPDIF clock comes from CODEC PLL_OUT (256*fs) or PCLK**
- **SPDIF clock up to 256*96k=24.576MHz, if it comes from CODEC**
- **Supports the IEC 60958 standards for PCM audio transmit**
- **Supports the IEC 61937 standards for non-linear PCM audio transmit**
- **Transmitter supports variable sample rate (8K~192K)**
- **Transmitter supports 16/24 bits per sample (PCM)**
- **Transmitter supports consecutive or non-consecutive linear PCM data transmit**
- **Transmitter supports support even parity generation**
- **Transmitter supports programmable channel status, user data, auxiliary bits and validity bit**
- **Supports the IEC 61937 standards for non-linear PCM audio receive**
- **Receiver supports variable sample rate (8K~48K), when it uses CODEC_pllout clock for decoding.**
- **Receiver supports sample rate high to N(KHz), when it uses APB clock for decoding and the frequency of APB clock is higher than 2*N*256(KHz). Eg, N=96, 2*N*256=49.152MHz**

3. APPLICATION SYSTEM CIRCUIT

In AMBA system, S/PDIF module can be configured as transmitter. It connects audio codec interface. The application circuit as following:

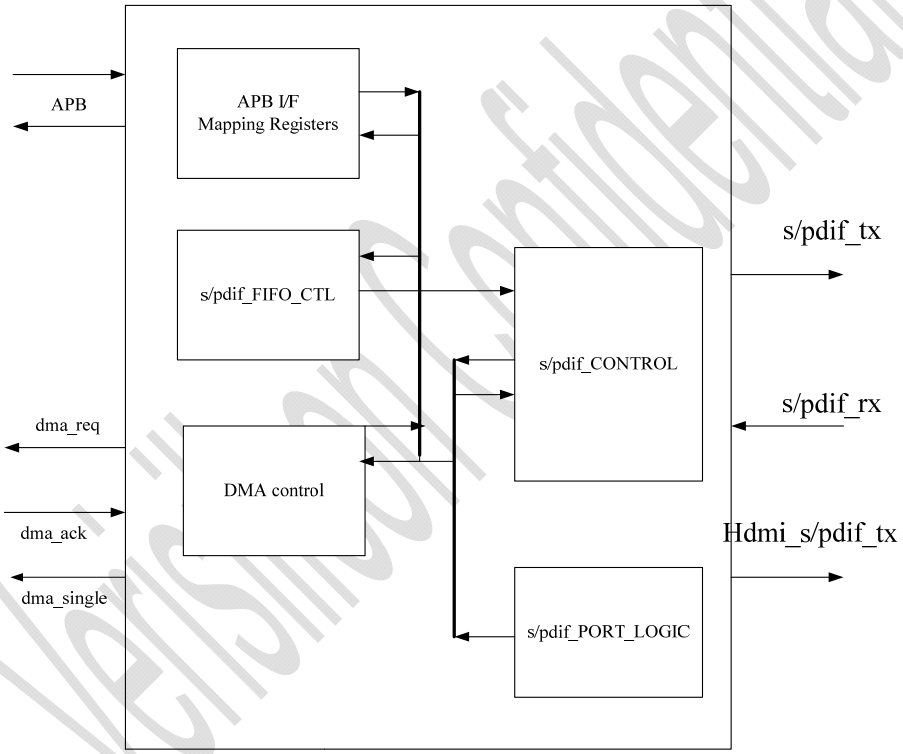


4. BLOCK DIAGRAM

S/PDIF can connect with external audio equipment, it includes the following basic sub-modules:

DMA Interface Logic
APB Interface Logic
Register Logic
FIFO controller
Transmitter Logic
Receiver Logic

The Block Diagram as the following:



4.1. APB BUS INTERFACE LOGIC

AMBA system can access control register, transmit data register through APB bus interface. The DMA can receive request and sends acknowledge in order to control the audio on APB bus.

4.2. REGISTER LOGIC

The register logic block contains all memory mapped register. The registers' definitions are shown in section 6.

4.3. FIFO

There is a FIFO in this design. It is 16 words level FIFO. It buffers data for transmitter or receiver.

APB writes data to **FIFO**, when SPDIF works as a transmitter.

A transmit operation begins when data is written to the temp data registers. Then, 16/24 bits will stuff in slot3~slot27 each time. Finally, the packed stream is encoded into BMC stream.

The "**dma_req"** signal is set when FIFO is no more than eight and need data to transmit, the signal sends to DMA and request APB bus transmits data to FIFO.

The "**dma_single"** signal is set when FIFO is not full and need data to transmit, the signal sends to DMA and request APB bus transmits data to TX FIFO.

APB reads data from **FIFO**, when SPDIF works as a receiver.

A receive operation begins when spdif_rx transmits stream to the temp register. Then, the register writes data to FIFO. Finally, APB reads data from FIFO.

The "**dma_req"** signal is set when FIFO is no less than eight and need data to receive, the signal sends to DMA and request APB bus receives data from FIFO.

The "**dma_single"** signal is set when FIFO is not empty and need data to receive, the signal sends to DMA and request APB bus receives data from FIFO.

4.4. NON-LINEAR RECEIVER

The receiver consumes 9 sub-frames for first stream locking. It updates the information automatically depend on the sample of input stream.

5. PIN LIST AND ASSIGNMENT

Pin assignment diagram.

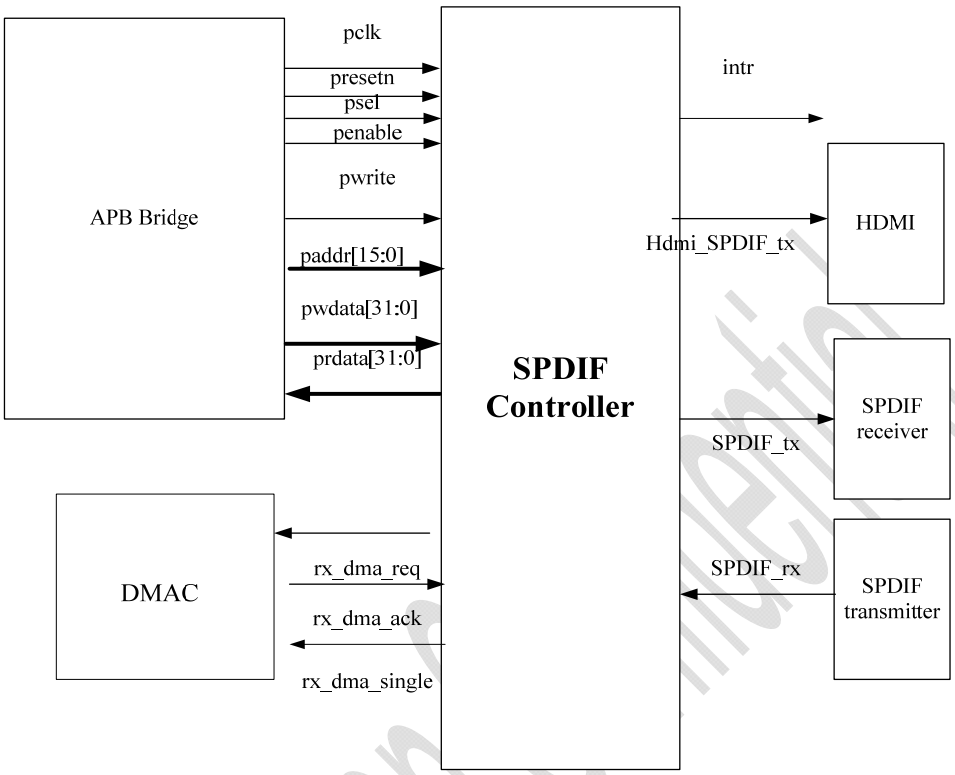


Figure 2: SPDIF Pin Assignment Diagram

Name	IO	Description
APB Interface Signal		
pclk	I	The APB clock and spdif_clk are asynchronous
presetn	I	Low active, APB reset signal
psel	I	Input from APB selection signal
penable	I	Input from APB enable signal
pwrite	I	Input from APB write signal, high is write signal, low is read signal
paddr[15:0]	I	Input from APB address bus
pwdata[31:0]	I	The APB data which are written into spdif
prdata[31:0]	O	The APB data which area read out from spdif
DMA Interface Signal		
dma_req	O	Transmit Burst Request signal to DMA, edge active Request a 8 burst, when it is valid.
Dma_single		Transmit single Burst Request signal to DMA, edge active,. It is sampled by the DMA only in the single

Name	IO	Description
		transaction. It must remain asserted until dma_ack is asserted, at which time the peripheral should de-assert dma_simgle.
Dma_ack	I	Transmit Burst Clear signal from DMA, edge active
Interface to peripheral bus or audio codec module		
Spdif_clk	I	A clock comes from CODEC PLL_OUT. It is used to generate SPDIF stream.
Spdif_tx	O	The SPDIF stream outputs to SPDIF receiver.(A speaker owns SPDIF interface).
HDMI_spdif_tx	O	The SPDIF stream outputs to HDMI receiver.
Spdif_rx	I	The input SPDIF stream from external SPDIF transmitter.
Global Signal		
intr	O	SPDIF transmitter interrupt signal to interrupt controller

6. REGISTER FILE AND MEMORY MAPPING DESCRIPTION

The following sections describe the registers used in configuring and operating the SPDIF transmitter or receiver

6.1. REGISTER AND MEMORY MAPPING SUMMARY TABLE

Table 1: SPDIF register file table

Name	Offset Address	Access	Width	Reset Value	Description
WR_DAT*	12'h000	W/R	[31:0]	32'h0	Write data register
RD_DAT**	12'h004	R	[31:0]	32'h0	Read data register
SYS_CTRL***	12'h008	W/R	[31:0]	32'h0	System control register
INT_STA***	12'h00c	R	[31:0]	32'h0	Interrupt status register
INT_EN***	12'h010	W/R	[31:0]	32'h0	Interrupt enable register
INT_CLR***	12'h014	W/R	[31:0]	32'h0	Interrupt clear register
IEC_CFG0*	12'h018	W/R	[31:0]	32'h0	Configuration according to IEC 60958
IEC_CFG1***	12'h01c	W/R	[31:0]	32'h0	Configuration according to IEC 61937
RP_BURST*	12'h020	W/R	[31:0]	32'h0	The number of IEC 60958 frames indicates Repetition period of burst.
RP_PAUSE*	12'h024	W/R	[31:0]	32'h0	The number of IEC 60958 frames indicates Repetition period of pause
RP_NULL*	12'h028	W/R	[31:0]	32'h0	The number of IEC 60958 frames indicates Repetition period of null
FIFO_CSTA***	12'h02c	W/R	[31:0]	32'h0	FIFO Current State
CHSTA_A0*	12'h030	W/R	[31:0]	32'h0	Information of Channel status for left channel
CHSTA_A1*	12'h034	W/R	[31:0]	32'h0	
CHSTA_A2*	12'h038	W/R	[31:0]	32'h0	
CHSTA_A3*	12'h03c	W/R	[31:0]	32'h0	
CHSTA_A4*	12'h040	W/R	[31:0]	32'h0	
CHSTA_A5*	12'h044	W/R	[31:0]	32'h0	
CHSTA_B0*	12'h048	W/R	[31:0]	32'h0	Information of Channel status for right channel
CHSTA_B1*	12'h04c	W/R	[31:0]	32'h0	
CHSTA_B2*	12'h050	W/R	[31:0]	32'h0	
CHSTA_B3*	12'h054	W/R	[31:0]	32'h0	
CHSTA_B4*	12'h058	W/R	[31:0]	32'h0	
CHSTA_B5*	12'h05c	W/R	[31:0]	32'h0	
UDAT_A0*	12'h060	W/R	[31:0]	32'h0	Information of User data for left channel
UDAT_A1*	12'h064	W/R	[31:0]	32'h0	
UDAT_A2*	12'h068	W/R	[31:0]	32'h0	
UDAT_A3*	12'h06c	W/R	[31:0]	32'h0	
UDAT_A4*	12'h070	W/R	[31:0]	32'h0	
UDAT_A5*	12'h074	W/R	[31:0]	32'h0	

UDAT_B0*	12'h078	W/R	[31:0]	32'h0	Information of User data for right channel
UDAT_B1*	12'h07c	W/R	[31:0]	32'h0	
UDAT_B2*	12'h080	W/R	[31:0]	32'h0	
UDAT_B3*	12'h084	W/R	[31:0]	32'h0	
UDAT_B4*	12'h088	W/R	[31:0]	32'h0	
UDAT_B5*	12'h08c	W/R	[31:0]	32'h0	
PD_PC***	12''h090	W/R	[31:0]	32'h0	The third and fourth burst preamble, PC is on low 16 bits, Pd is on high 16 bits APB writes and reads this register, when design works as a transmitter. APB reads this register only, when design works as a receiver.
PF_PE***	12'h094	W/R	[31:0]	32'h0	Extended preamble, PE is on low 16 bits, PF is on high 16 bits APB writes and reads this register, when design works as a transmitter. APB reads this register only, when design works as a receiver.

NOTE:

1. The register with a * postfix are valid, when design works as a transmitter.
2. The register with a ** postfix are valid, when design works as a receiver.
3. The register with a ***postfix are valid, when design works as a transmitter or receiver.

6.2. REGISTER DESCRIPTION

- **SPDIF Write data register (WR_DAT, offset address : 12'h000)**

Name	Bits	Access	Reset value	Description
WR_DAT	31:0	W/R	0x0000	Write 32bit audio data to transmitter FIFO

- **SPDIF Read data register (RD_DAT, offset address: 12'h004)**

Name	Bits	Access	Reset value	Description
RD_DAT	31:0	R	0x0000	Read 32bit audio data from receiver FIFO

- **System Control Register (SYS_CTRL, offset address: 12'h008)**

Name	Bits	Access	Reset value	Description
---	31:9	W/R	0x00	Reserved

RX_clk_sel	8	W/R	0x0	Select decode clock, when it works as non-linear receiver 0, codec_pllout 1, APB clock
If_sel	7	W/R	0x0	Select audio interface 0x0, external spdif receiver 0x1, HDMI spdif interface
Tx_sample_rate	6	W/R	0x0	Select sample rate 0, The sample rate of SPDIF transmit is same as fs, which is defined by internal CODEC 1, The sample rate of SPDIF transmit is double frequency of fs.
Tx_linear	5	W/R	0x0	Indicates the transmit stream contains linear PCM or non-linear PCM. 1, linear PCM; 0 non-linear PCM.
Tx_stop	4	W/R	0x00	A stop command. It is active high. It will stop transmission, when all sub-frames have been sent. It is automatically cleared, after the transmission stop.
Fifo_flush	3	W/R	0x0	1, Flush FIFO 0, FIFO works normally
Tx0_Rx1	2	W/R	0x0	Select transmitter or receiver 0, enable transmitter only 1, enable receiver only
Dma_en	1	W/R	0x0	Enable DMA
Spdif_en	0	W/R	0x0	Enable SPDIF

- **Interrupt Status Register (INT_STA, offset address: 12'h00c)**

Name	Bits	Access	Reset value	Description
---	31:15	R	0x0	Reserved
RxInfo_int	14	R	0x0	Information of Pc, Pd, Pe or Pf have updated
RxTotal_int	13	R	0x0	All data have been received
Rxburst_int	12	R	0x0	An audio burst have been received
---	11	R	0x0	Reserved
TxGap_int	10	R	0x0	Indicates non-linear transmission in stream gap status
Txburst_int	9	R	0x0	A non-linear audio burst finish
TxHalfBlk_int	8	R	0x0	96 frames (IEC 60958) have been sent
TxBlock_int	7	R	0x0	192 frames(IEC 60958) have been sent
TxFrame_int	6	R	0x0	A frame (IEC 60958) has been sent
TxSFrame_int	5	R	0x0	A sub-frame (IEC 60958) has been sent
TxTotal_int	4	R	0x0	All data transmit completely. TxTotal_int is

				high, when FIFO is empty and stop is high.
	[3:2]	R	0x0	Reserved
Full_int	1	R	0x0	FIFO is full
Empty_int	0	R	0x0	FIFO is empty expect initial empty

NOTE: All interrupts are triggered by rise-edge .

- **Interrupt Enable Register (INT_EN, offset address: 12'h010)**

Name	Bits	Access	Reset value	Description
---	31:15	W/R	0x0	Reserved
RxInfo_en	14	W/R	0x0	Enable Receive Information update interrupt
RxTotal_en	13	W/R	0x0	Enable Total data receive interrupt
Rxburst_en	12	W/R	0x0	Enable audio burst interrupt
---	11	R	0x0	Reserved
TxGapInt_en	10	W/R	0x0	Enable non-linear gap interrupt
Txburst_en	9	W/R	0x0	Enable non-linear audio burst interrupt
TxHalfBlk_en	8	W/R	0x0	Enable half block interrupt
TxBlock_en	7	W/R	0x0	Enable block interrupt
TxFrame_en	6	W/R	0x0	Enable frame interrupt
TxSFrame_en	5	W/R	0x0	Enable sub-frame interrupt
TxTotal_en	4	W/R	0x0	Enable Total data transmit interrupt
	[3:2]	R	0x0	Reserved
Full_en	1	W/R	0x0	Enable FIFO full interrupt
Empty_en	0	W/R	0x0	Enable FIFO empty interrupt

- **Interrupt Clear Register (INT_CLR, offset address: 12'h014)**

Name	Bits	Access	Reset value	Description
---	31:15	R	0x0	Reserved
RxInfo_clr	14	W/R	0x0	Clear Receive Information update interrupt
RxTotal_clr	13	W/R	0x0	Clear Total data receive interrupt
Rxburst_clr	12	W/R	0x0	Clear receiver audio burst interrupt
---	11	R	0x0	Reserved
TxGapInt_Clr	10	W/R	0x0	Clear Tx non-linear gap interrupt
TxBurstInt_Clr	9	W/R	0x0	Clear Tx non-linear audio burst interrupt
TxHalfBlk_Clr	8	W/R	0x0	Clear Tx half clock interrupt
TxBlock_Clr	7	W/R	0x0	Clear Tx clock interrupt
TxFrame_Clr	6	W/R	0x0	Clear Tx frame interrupt
TxSFrame_Clr	5	W/R	0x0	Clear Tx sub-frame interrupt
TxTotal_Clr	4	W/R	0x0	Clear Tx Total data transmit interrupt
	[3:2]	R	0x0	Reserved
Full_clr	1	W/R	0x0	Clear full interrupt
Empty_Clr	0	W/R	0x0	Clear empty interrupt

● **IEC (60958-1) Configuration Register 0(IEC_CFG0, offset address: 12'h018)**

Name	Bits	Access	Reset value	Description
---	[31:16]	R	0x0	Reserved
Lock_time	15:12	W/R	0x0	Indicates a time for receiver locking the sample rate. It is valid only, when design works a linear PCM transmitter There are N zeros frames before valid frame transmitting, when lock_time=N.
---	11:9	R	0x0	Reserved
Data_format	8	W/R	0x0	Indicates linear PCM data format 0, consecutive data format 1, non-consecutive data format
stereo	7	W/R	0x0	1: stereo; 0: mono.
Width	6	W/R	0x0	It indicates the sample depth. 0, 16 bits; 1, 24 bits
Auxi_bits	[5:2]	W/R	0x0	Auxiliary sample bit in the sub-frame. These bits are valid, when the sample is 16 bits. (width=0)
Valid_bitR	1	W/R	0x0	The validity bit in Right channel
Valid_bitL	0	W/R	0x0	The validity bit in Left channel

Note:

When you are dealing with such stereo or mono sounds (linear PCM), if data_format (register IEC_CFG0) is low, single sample points from each channel are interleaved.

For example, when the sample rate is 16, for 32bit FIFO, its data format as following:

1) Mono data

For one channel to transmit (stereo=1'b0 in IEC_CFG0)

31	16	15	0
Second 16-bit mono channel data		First 16-bit mono channel data	
Fourth 16-bit mono channel data		Third 16-bit mono channel data	

2) Stereo data

For two channel data to transmit
(stereo = 1'b1, in IEC_CFG0)

31	16	15	0
First 16-bit channel 2 data		First 16-bit channel 1 data	
Second 16-bit channel 2 data		Second 16-bit channel 1 data	

When you are dealing with such stereo sounds (linear PCM), if data_format (register IEC_CFG0) is high, single sample points from each channel store in low bits of a word (32 bits).

For example, when the sample rate is 16, for 32bit FIFO, its data format as following:

1) Mono data

For one channel data transmit (stereo =1'b0 in IEC_CFG0)

31 ... 16	15 ... 0
zreos	First 16-bit mono channel data
zeros	Secod 16-bit mono channel data

2) Stereo data

For two channel data to transmit
(stereo = 1'b1 in IEC_CFG0)

31 ... 16	15 ... 0
zeros	First 16-bit channel 1 data
zeros	First 16-bit channel 2 data
zeros	Second 16-bit channel 1 data
zeros	Second 16-bit channel 2 data

When the sample rate is 24, the data (linear PCM) in FIFO is similar to 16-bit data.

● **IEC (61937-1) Configuration Register 1(IEC_CFG1, offset address: 12'h01c)**

Name	Bits	Access	Reset value	Description
---	[31:7]	R	0x0	Reserved
Pl_en	6	W/R	0x0	Pause length enable. 1, pause burst payload contains the burst length; 0, pause burst length in payload is 0.
Bit_byte***	5	W/R	0x0	The unit of length code in Pd is bit or byte. 0, byte; 1 bit
reserved	4	W/R	0x0	Keep it low (0).
Null_On	3	W/R	0x0	1, null data-type is provided to be inserted occasionally in case the interface is idle; 0, disable (refer to 61937-1)
Pause_Middle	2	W/R	0x0	1, Send pause data-burst, when gap occurs 0, Send zeros or null data (idle), when gap occurs
Pause_End	1	W/R	0x0	1, A pause data burst follows the last data burst. 0, Non pause data burst follows the last data burst (refer to 61937-1)
Pause_front	0	W/R	0x0	1, A pause data_burst is sent immediately preceding the transmission of the first audio data_burst.

				0. non pause data-burst before the first audio data-burst .(refer to 61937-1)

The Bit_byte with a ***postfix are valid, when design works as a transmitter or receiver

- **Repetition Period of audio data-burst Register (RP_BURST, offset address: 12'h020)**

Name	Bits	Access	Reset value	Description
---	[31:16]		0x0	Reserved
Rp_burst	[15:0]	W/R	0x0	The number of IEC 60958 frames indicates the repetition period of audio data-burst

- **Repetition Period of PASUE Register (RP_PAUSE, offset address: 12'h024)**

Name	Bits	Access	Reset value	Description
---	[31:16]		0x0	Reserved
Rp_Pause	[15:0]	W/R	0x0	The number of IEC 60958 frames indicates the repetition period of pause

- **Repetition Period of NULL Register (RP_NULL, offset address: 12'h028)**

Name	Bits	Access	Reset value	Description
---	[31:16]		0x0	Reserved
Rp_null	[31:16]	W/R	0x0	The number of IEC 60958 frames indicates the repetition period of null

- **FIFO Current State (FIFO_CSta, offset address: 12'h02c)**

Name	Bits	Access	Reset value	Description
------	[31:4]	R	0x0	reserved
MHalf_Num	3	R	0x0	Indicates the number of data in FIFO is more than half depth of FIFO (eight).
LHalf_Num	2	R	0x1	Indicates the number of data in FIFO is less than half depth of FIFO (eight).
Fifo_full	1	R	0x0	Indicates FIFO full

Fifo_empty	0	R	0x1	Indicates FIFO empty

- **Channel Status Left(A) 0 Register (CHSTA_A0, offset address: 12'h030)**

Name	Bits	Access	Reset value	Description
ChSta_A0	[31:0]	R/W	0x0	First four bytes in channel status table for left(A) channel

- **Channel Status Left(A) 1 Register (CHSTA_A1, offset address: 12'h034)**

Name	Bits	Access	Reset value	Description
ChSta_A1	[31:0]	R/W	0x0	Second four bytes in channel status table for left(A) channel

- **Channel Status Left(A) 2 Register (CHSTA_A2, offset address: 12'h038)**

Name	Bits	Access	Reset value	Description
ChSta_A2	[31:0]	R/W	0x0	Third four bytes in channel status table for left(A) channel

- **Channel Status Left(A) 3 Register (CHSTA_A3, offset address: 12'h03c)**

Name	Bits	Access	Reset value	Description
ChSta_A3	[31:0]	R/W	0x0	Fourth four bytes in channel status table for left(A) channel

- **Channel Status Left(A) 4 Register (CHSTA_A4, offset address: 12'h040)**

Name	Bits	Access	Reset value	Description
ChSta_A4	[31:0]	R/W	0x0	Fifth four bytes in channel status table for left(A) channel

- **Channel Status Left(A) 5 Register (CHSTA_A5, offset address: 12'h044)**

Name	Bits	Access	Reset value	Description
ChSta_A5	[31:0]	R/W	0x0	Sixth four bytes in channel status table for left(A) channel

- **Channel Status Right(B) 0 Register (CHSTA_B0, offset address: 12'h048)**

Name	Bits	Access	Reset value	Description
ChSta_B0	[31:0]	R/W	0x0	First four bytes in channel status table for right (B) channel

- **Channel Status Right(B) 1 Register (CHSTA_B1, offset address: 12'h04c)**

Name	Bits	Access	Reset value	Description
ChSta_B1	[31:0]	R/W	0x0	Second four bytes in channel status table for Right(B) channel

- **Channel Status Right(B) 2 Register (CHSTA_B2, offset address: 12'h050)**

Name	Bits	Access	Reset value	Description
ChSta_A2	[31:0]	R/W	0x0	Third four bytes in channel status table for left(B) channel

- **Channel Status Right(B) 3 Register (CHSTA_B3, offset address: 12'h054)**

Name	Bits	Access	Reset value	Description
ChSta_B3	[31:0]	R/W	0x0	Fourth four bytes in channel status table for Right(B) channel

- **Channel Status Right(B) 4 Register (CHSTA_B4, offset address: 12'h058)**

Name	Bits	Access	Reset value	Description

ChSta_B4	[31:0]	R/W	0x0	Fifth four bytes in channel status table for Right(B) channel

- **Channel Status Right(B) 4 Register (CHSTA_B5, offset address: 12'h05c)**

Name	Bits	Access	Reset value	Description
ChSta_B5	[31:0]	R/W	0x0	Sixth four bytes in channel status table for Right(B) channel

- **User Data Left(A) 0 Register (UDAT_A0, offset address: 12'h060)**

Name	Bits	Access	Reset value	Description
UDat_A0	[31:0]	R/W	0x0	First four bytes in User Data table for Left(A) channel

- **User Data Left(A) 1 Register (UDAT_A1, offset address: 12'h064)**

Name	Bits	Access	Reset value	Description
UDat_A1	[31:0]	R/W	0x0	Second four bytes in User Data table for Left(A) channel

- **User Data Left(A) 2 Register (UDAT_A2, offset address: 12'h068)**

Name	Bits	Access	Reset value	Description
UDat_A2	[31:0]	R/W	0x0	Third four bytes in User Data table for Left(A) channel

- **User Data Left(A) 3 Register (UDAT_A3, offset address: 12'h06c)**

Name	Bits	Access	Reset value	Description
UDat_A3	[31:0]	R/W	0x0	Fourth four bytes in User Data table for Left(A) channel

- **User Data Left(A) 4 Register (UDAT_A4, offset address: 12'h070)**

Name	Bits	Access	Reset value	Description
UDat_A4	[31:0]	R/W	0x0	Fifth four bytes in User Data table for Left(A) channel

- **User Data Left(A) 5 Register (UDAT_A05 offset address: 12'h074)**

Name	Bits	Access	Reset value	Description
UDat_A5	[31:0]	R/W	0x0	Sixth four bytes in User Data table for Left(A) channel

- **User Data Right(B) 0 Register (UDAT_B0, offset address: 12'h078)**

Name	Bits	Access	Reset value	Description
UDat_B0	[31:0]	R/W	0x0	First four bytes in User Data table for Right(B) channel

- **User Data Right(B) 1 Register (UDAT_B1, offset address: 12'h07c)**

Name	Bits	Access	Reset value	Description
UDat_B1	[31:0]	R/W	0x0	Second four bytes in User Data table for Right(B) channel

- **User Data Right(B) 2 Register (UDAT_B2, offset address: 12'h080)**

Name	Bits	Access	Reset value	Description
UDat_B2	[31:0]	R/W	0x0	Third four bytes in User Data table for Right(B) channel

- **User Data Right(B) 3 Register (UDAT_B3, offset address: 12'h084)**

Name	Bits	Access	Reset value	Description

UDat_B3	[31:0]	R/W	0x0	Fourth four bytes in User Data table for Right(B) channel

- **User Data Right(B) 4 Register (UDAT_B4, offset address: 12'h088)**

Name	Bits	Access	Reset value	Description
UDat_B4	[31:0]	R/W	0x0	Fifth four bytes in User Data table for Right(B) channel

- **User Data Right(B) 5 Register (UDAT_B5 offset address: 12'h08c)**

Name	Bits	Access	Reset value	Description
UDat_B5	[31:0]	R/W	0x0	Sixth four bytes in User Data table for Right(B) channel

- **IEC 61937 PC and PD Register (PD_PC, offset address: 12'h090)**

Name	Bits	Access	Reset value	Description
PD_PC	[31:0]	R/W	0x0	The third and forth preamble in IEC 61937 PC is on low 16-bits; PD is on high 16-bits. Read value equal to write value, when design works as a transmitter. Read value is from decoding stream, when design works as a receiver.

- **IEC 61937 PF and PE Register (PF_PE offset address: 12'h094)**

Name	Bits	Access	Reset value	Description
PF_PE	[31:0]	R/W	0x0	The extended preamble in IEC 61937 PE is on low 16-bits, PF is on high 16-bits Read value equal to write value, when design works as a transmitter. Read value is from decoding stream, when design works as a receiver.

7. INTERFACE TIMING

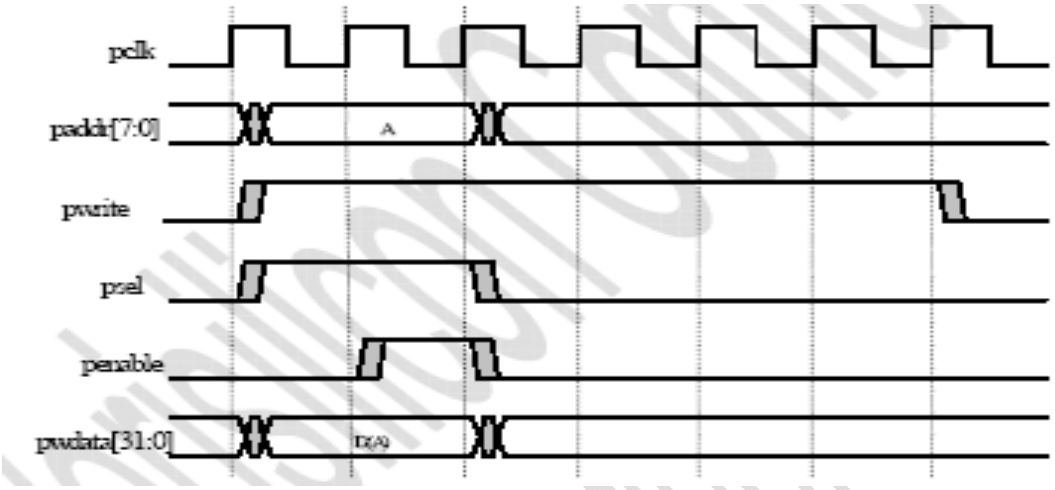


Figure 7-1 APB Write Transfer TIMING

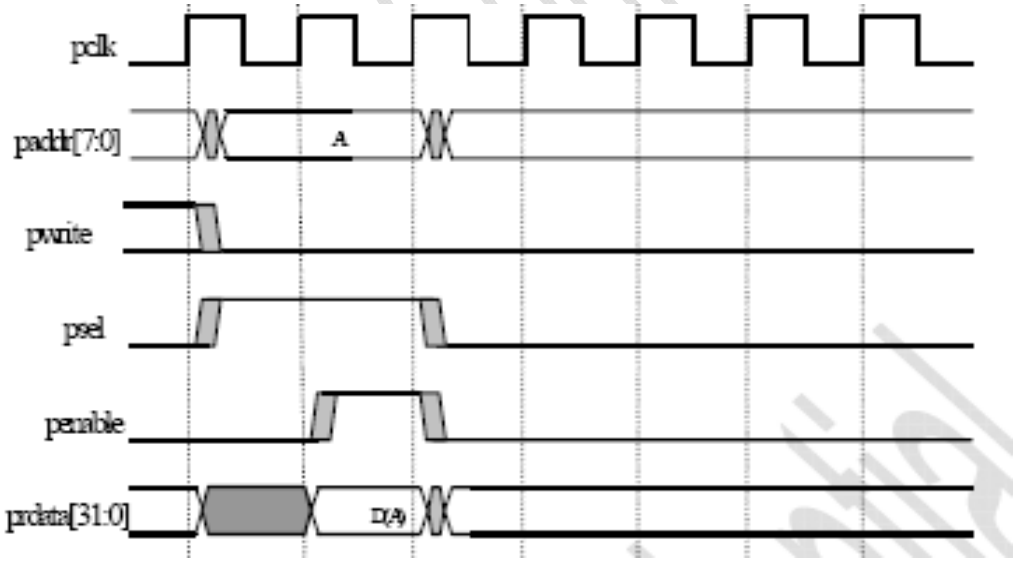


Figure 7-2 APB Read Transfer TIMING

8. SPDIF (IEC 60958) PROTOCOL (LINEAR PCM)

8.1. SUB-FRAME FORMAT

Each sub-frame is divided into 32 times slots, numbered from 0 to 31.(see Figure 8-1)

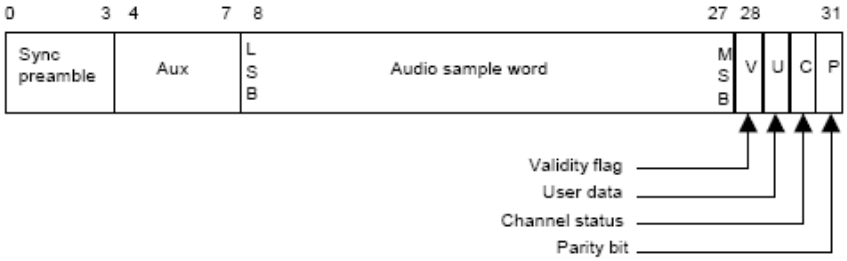


Figure 8-1 Sub-frame format (liner PCM application)

Time slots 0 to 3 carry one of the three permitted preambles.

Time slots 4 to 27 carry the audio sample word in linear 2's complement representation. The most significant bit (MSB) is carried by time slot 27. When source audio sample range is 20, the time slots 4 to 7 is programmable by APB bus. When source audio sample range is 16, the time slots 4 to 11 is stuffed 0s.

Time slot 28 carries the validity bit associated with the main data field.

Time slot 29 carries 1 bit of the user data channel associated with the main data field channel transmitted in the same sub-frame.

Time slot 30 carries 1 bit of channel status information associated with the main data field channel transmitted in the same sub-frame.

Time slot 31(parity bit) carries a parity bit such that time slots 4 to 31 inclusive carry an even number of ones and an even number of zeros (even parity).The parity bit is zero, when the number of one is even.

The parity bit is one, when the number of one is odd.

8.2. FRAME FORMAT

A frame is uniquely composed of two sub-frames. For linear coded audio applications, the rate of frames normally corresponds exactly to the source sampling frequency.

In 2-channel operation mode, the samples taken from both channels are transmitted by time multiplexing in consecutive sub-frames. The first sub-frame (left or "A" channel in stereophonic operation and primary channel in monophonic operation) normally starts with preamble "M". However, the preamble changes to preamble "B" once every 192 frames to identify the start of the block structure used to organize the channel status information. The second sub-frame (right or "B" channel in stereophonic operation and secondary channel in monophonic operation) always starts with preamble "W".

In single channel operation mode in a professional application, the frame format is the same as in the 2-channel mode. Data is carried in the first sub-frame and may be duplicated in the second sub-frame. If the second sub-frame is not carrying duplicate data, time slot 28 (validity flag) shall be set to logical "1".

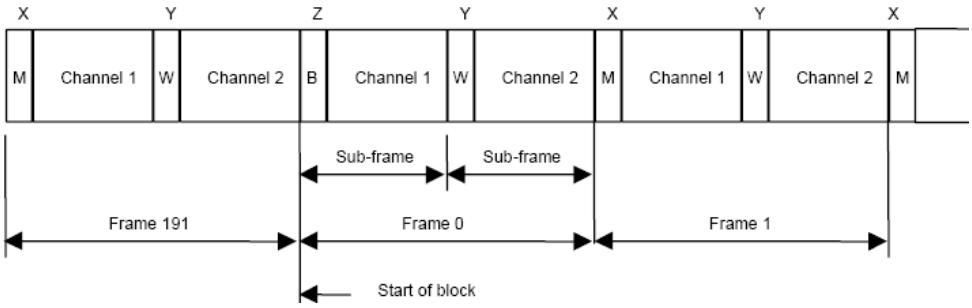


Figure 8-2 Frame format

8.3. CHANNEL CODING

To minimize the direct current (DC) component on the transmission line, to facilitate clock recovery from the data stream and to make the interface insensitive to the polarity of connections, time slots 4 to 31 are encoded in biphase-mark.

Each bit to be transmitted is represented by a symbol comprising two consecutive binary states. The first state of a symbol is always different from the second state of the previous symbol. The second state of the symbol is identical to the first if the bit to be transmitted is logical "0". However, it is different if the bit is logical "1" (see Figure 8-3).

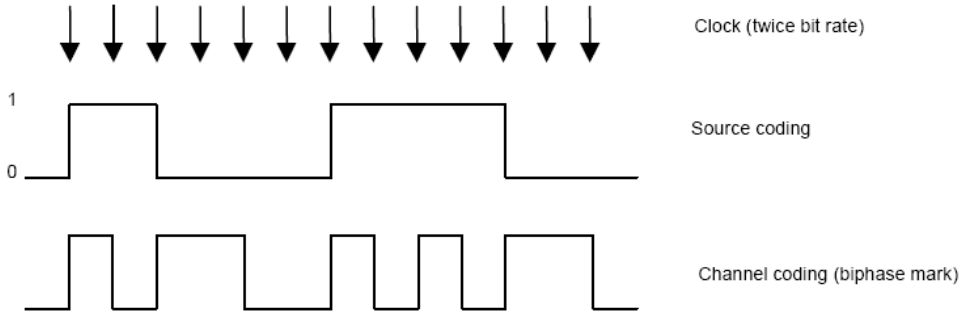


Figure 8-3 Channel coding

8.4. PREAMBLE

Preambles are specific patterns providing synchronization and identification of the sub-frames and blocks.

To achieve synchronization within one sampling period and to make this process completely reliable, these patterns violate the biphase-mark code rules, thereby avoiding the possibility of data imitating the preambles.

A set of three preambles is used. These preambles are transmitted in the time allocated to four time slots at the start of each sub-frame (time slots 0 to 3), and are represented by eight successive states. The first state of the preamble is always different from the second state of the previous symbol (representing the parity bit). Depending on this state, the preambles are as shown in Table 8-1.

Preceding state	0	1	
Preamble code	**Channel coding**		
"B" or "Z" (see note to 4.1.2)	11101000	00010111	Sub-frame 1 and the start of the block
"M" or "X"	11100010	00011101	Sub-frame 1
"W" or "Y"	11100100	00011011	Sub-frame 2

Table 8-1 Preamble coding

9. SPDIF (IEC 61937) PROTOCOL (NON-LINEAR PCM)

9.1.

The non-linear PCM encoded audio bit-stream is transferred using the basic 16-bit data area of the IEC 60958 sub-frames, i.e. in time-slots 12 to 27. (See, figure 9-1)

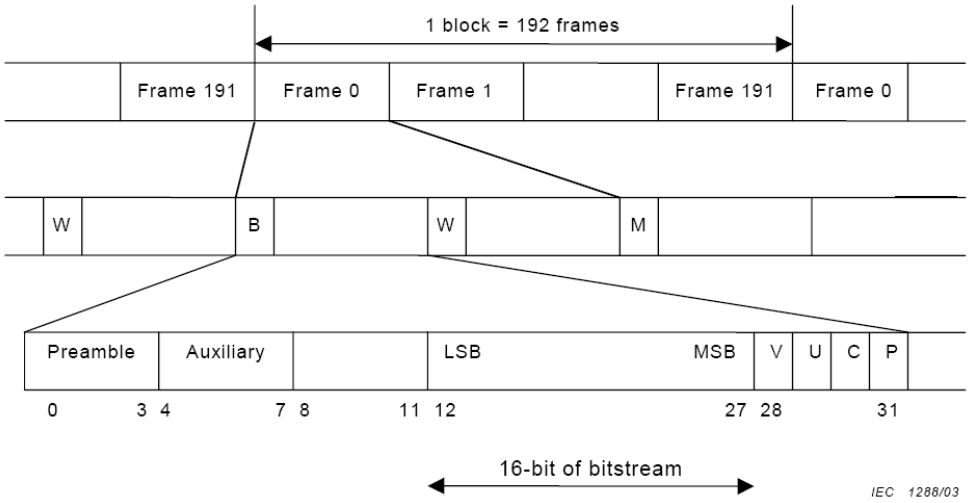


Figure 9-1 non-linear PCM format base on IEC60958

9.2. THE FORMAT OF THE DATA-BURST

Each data-burst contains a burst-preamble consisting of four 16-bit words (Pa, Pb, Pc and Pd) followed by the burst-payload which contains data of an encoded audio frame.(See figure 9-2) The repetition period of these bursts is defined as the length between the reference points R (measured in IEC 60958 frames) of one data-burst and the next data-burst (with the same bit-stream-number).

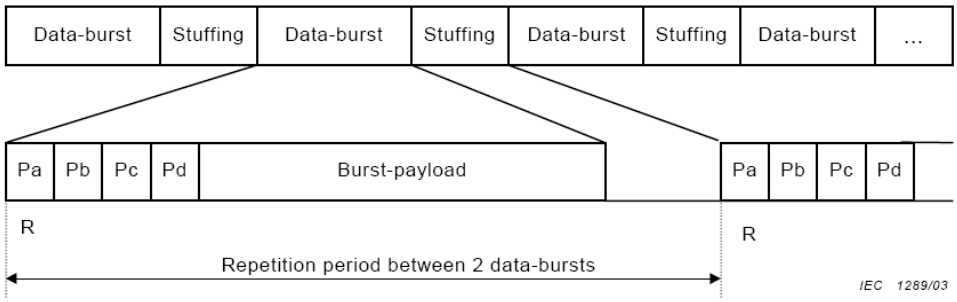
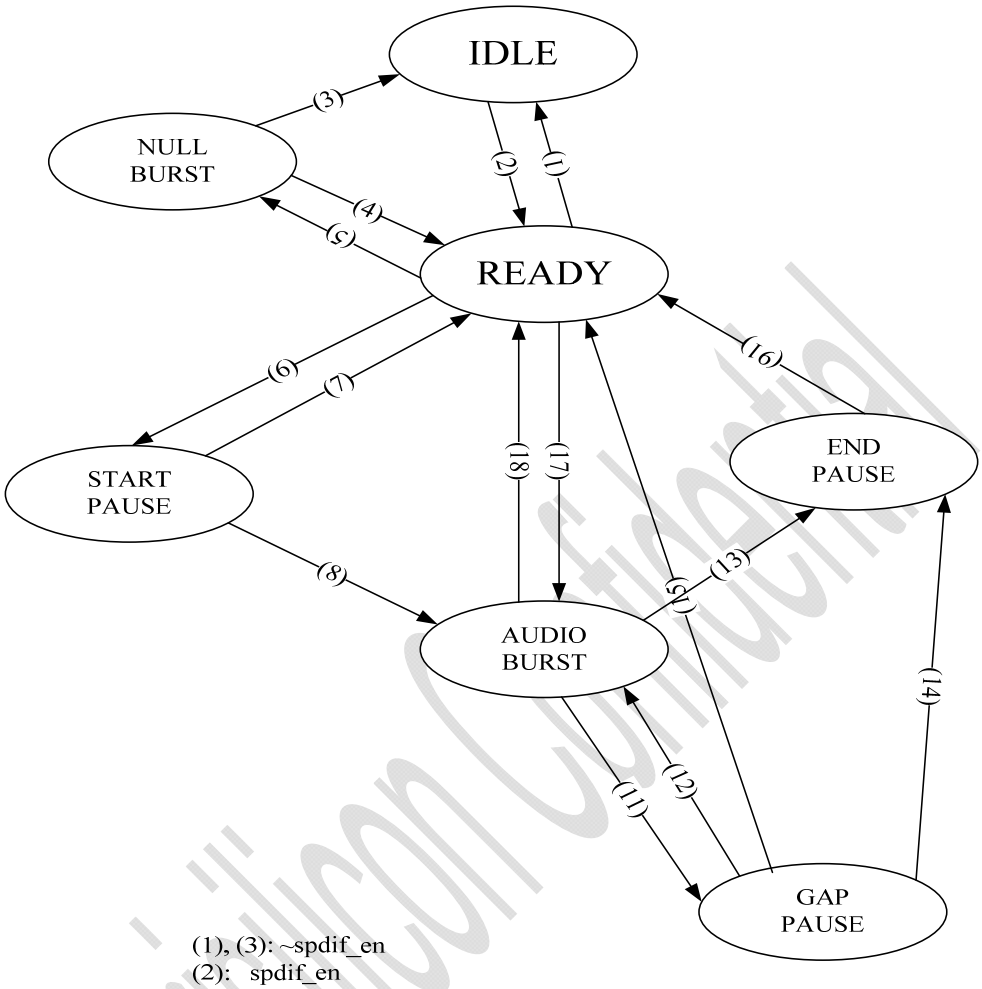


Figure 9-2 data-burst format

10. FSM FOR NON-LINEAR TRANSMISSION



(1), (3): ~spdif_en
(2): spdif_en
(4): null_stop
(5): null_start
(6): ~fifo_empty&pause_front&~gap_sta
(7): stop
(8): pause_stop
(9): remove burst-spcae
(10): remove burst-spcae
(11): burst_stop&~stop&fifo_empty&pause_middle
(12): pause_stop&~stop&~fifo_empty
(13): stop&burst_stop&pause_end
(14): pause_stop&pause_end&stop
(15): pause_stop&~pause_end&stop
(16): pause_stop
(17): ~fifo_empty&pause_front&gap_sta
(18): burst_stop&~stop&fifo_empty&~pause_middle

11. CONFIGURATION PROGRAM FLOW

- **SPDIF linear PCM Data Transmit Program Flow**

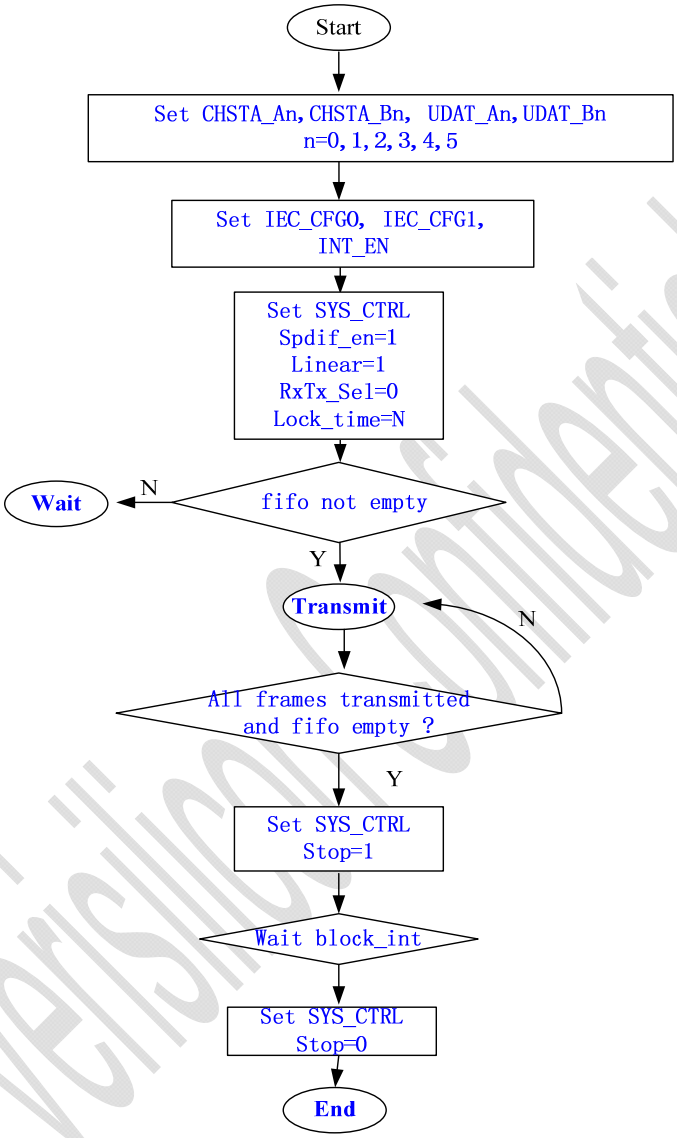


Figure 11-1 linear PCM transmit program flow

Note: The total number of data is decides by DMA controller.

● **SPDIF non-linear PCM Data Transmit Program Flow**

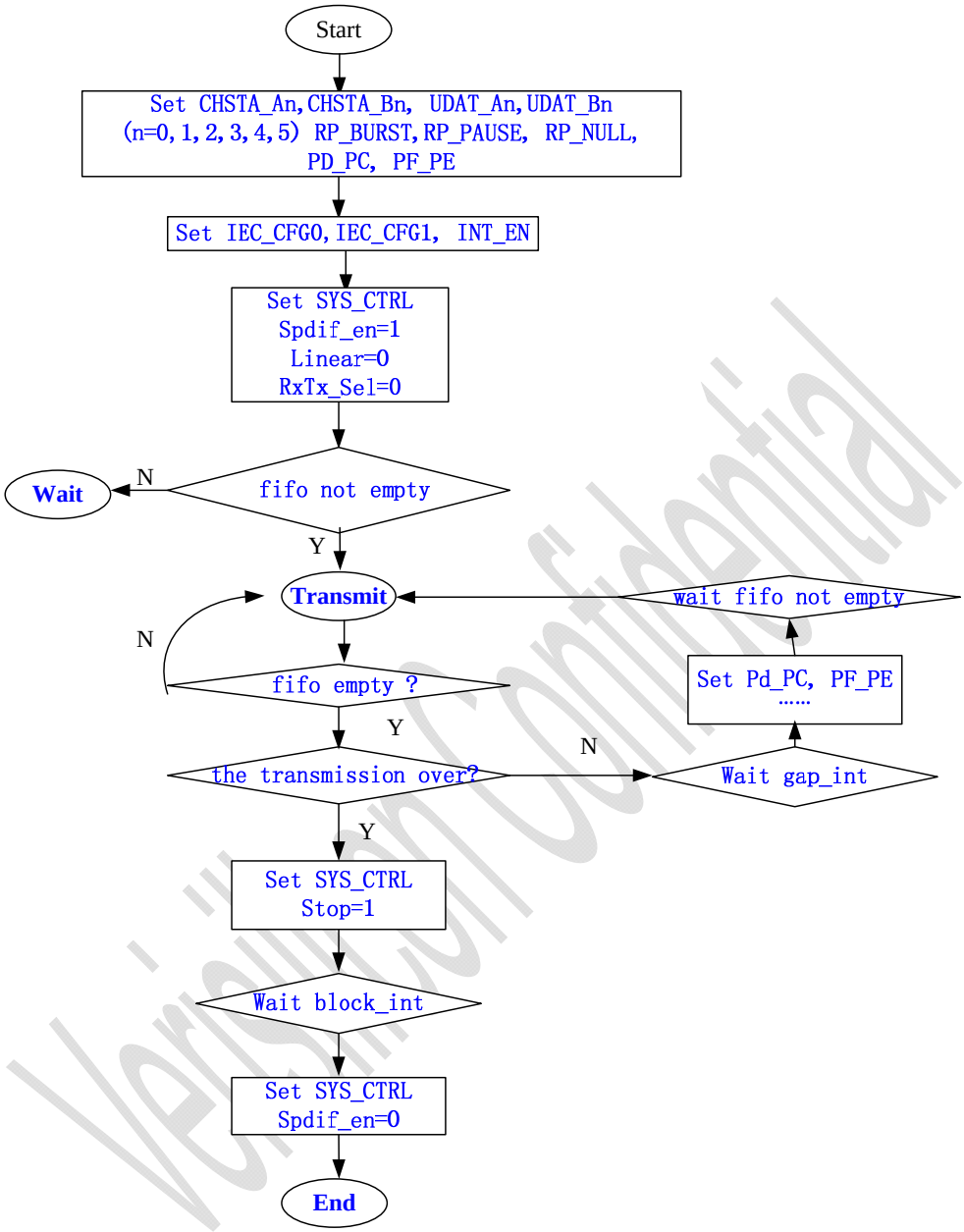
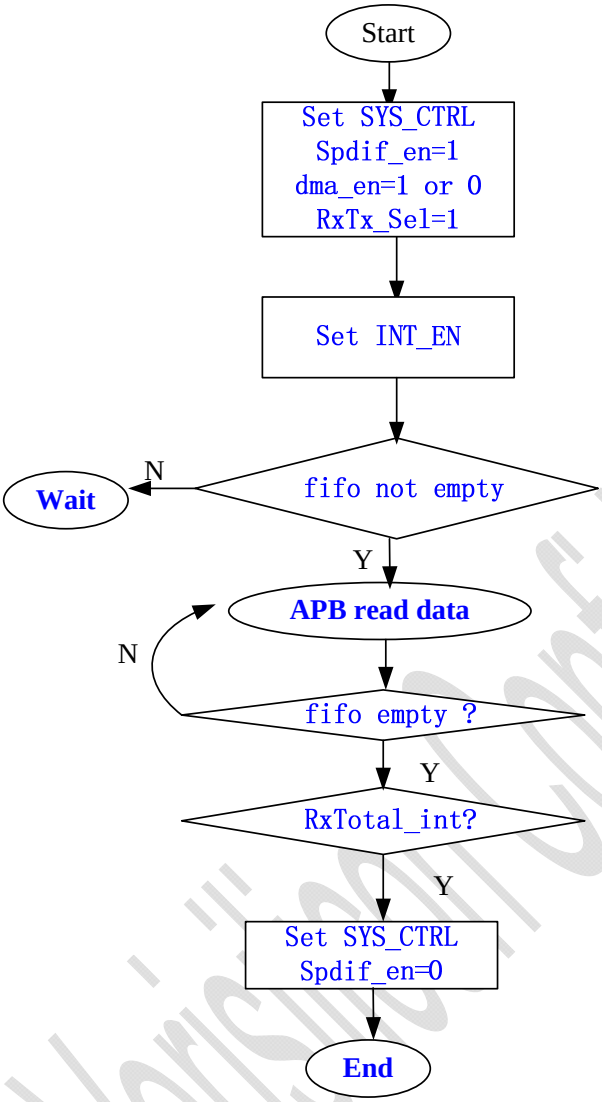


Figure Non-linear PCM transmit program flow

Note: The total number of data is decides by DMA controller.

- **SPDIF non-linear PCM Data receive Program Flow**



12. TEST PLAN

For simulation, we major in the following aspects:

1) **bus interface logic**
2) **data format (data path)**
3) **SPDIF interface**
4) **DMA operation**
5) **Register access**
6) **Corner case**

13. NEXT STEP

1. Add SPDIF linear PCM receiver