Project 3: Measuring Cache and TLB Performance

Due: 11:59PM Nov 18

Each student must turn in a separate set of homework solutions, but you may work together in study groups with other students from the class. Include the names of your study group members on the solution set you submit.

In this assignment, you are going to select a computer, use a program to measure the computer’s cache (built of SRAM) performance, and report the measured cache performance.

Any of the Linux computers in the lab will work. You can also measure your own computer if you like.

The benchmark memory.c can be downloaded on canvas. Follow the instructions at the beginning of the code for compilation and run. After launched, this program prints results of data size, stride size, access time. Use the results and plot with a software, e.g., Excel, python with matplotlib, or matlab, a figure similar as Figure 1.

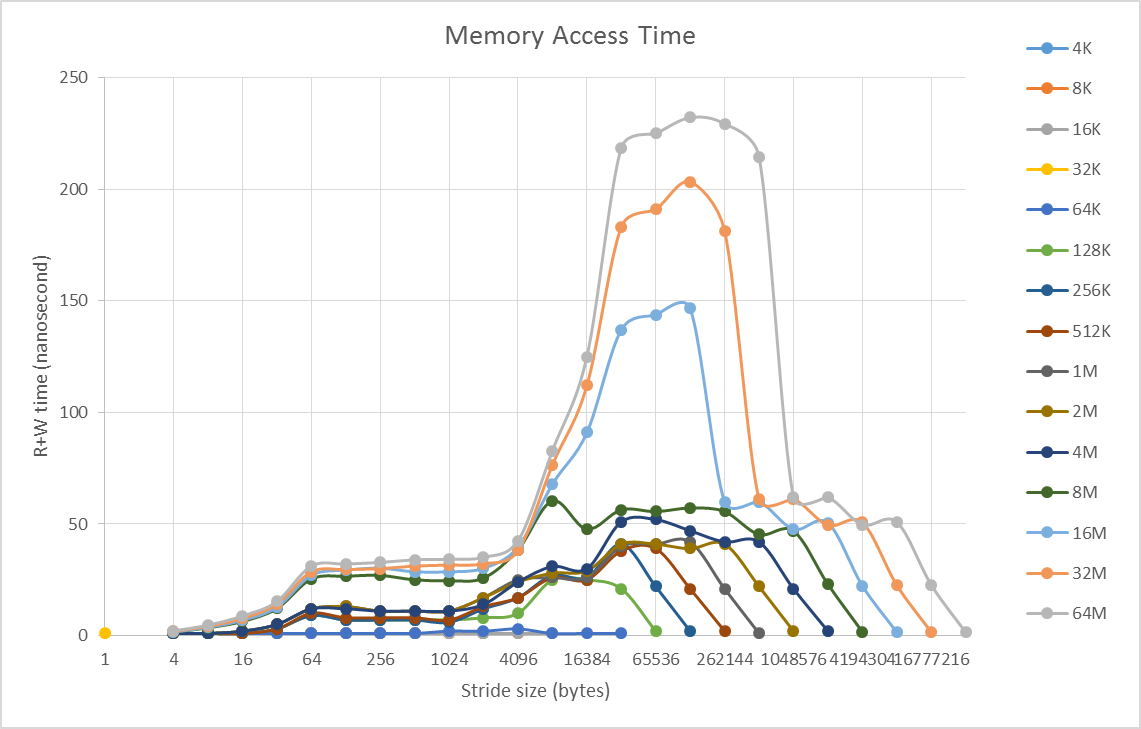
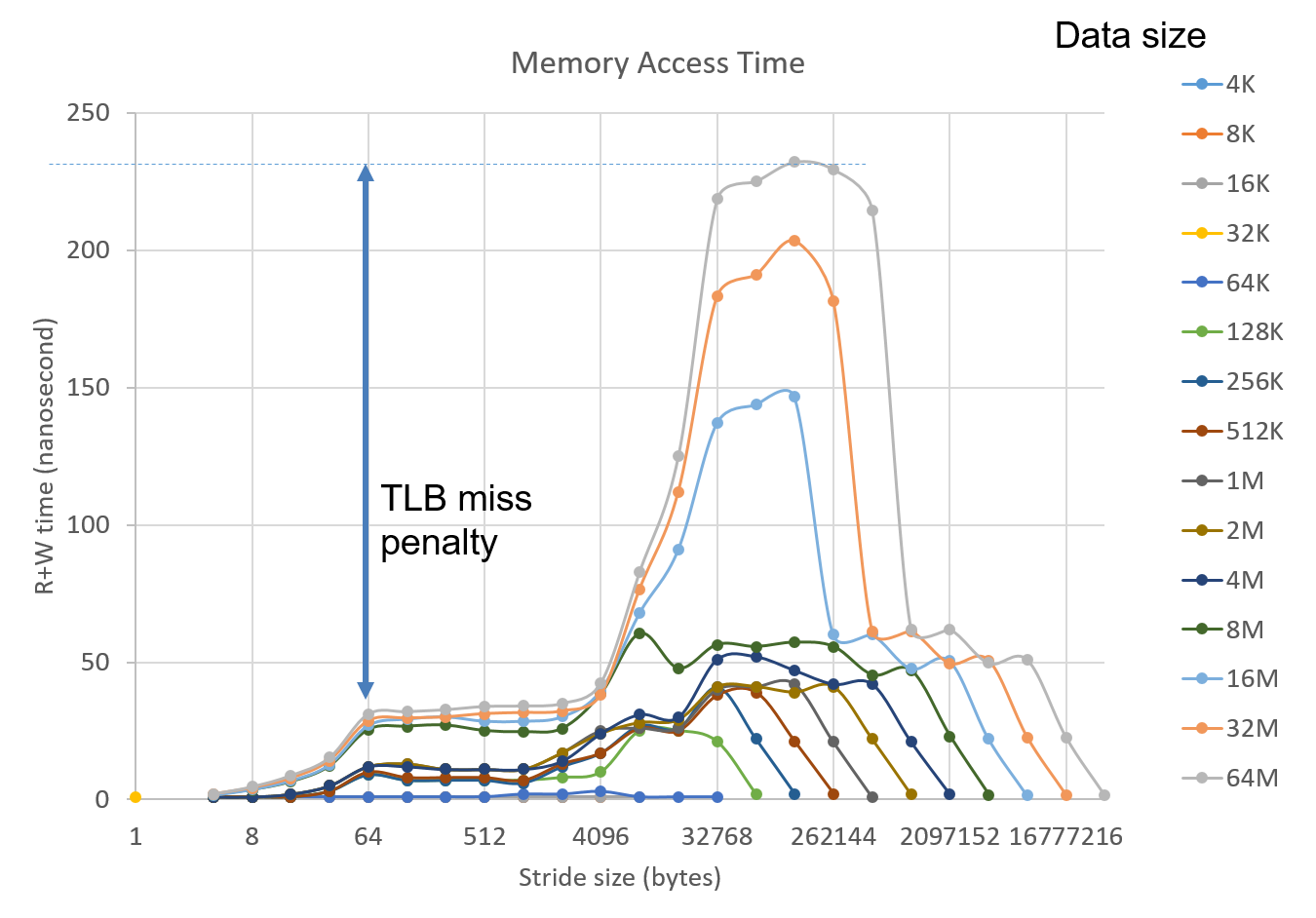


Fig 1. Cache Performance of Machine I.



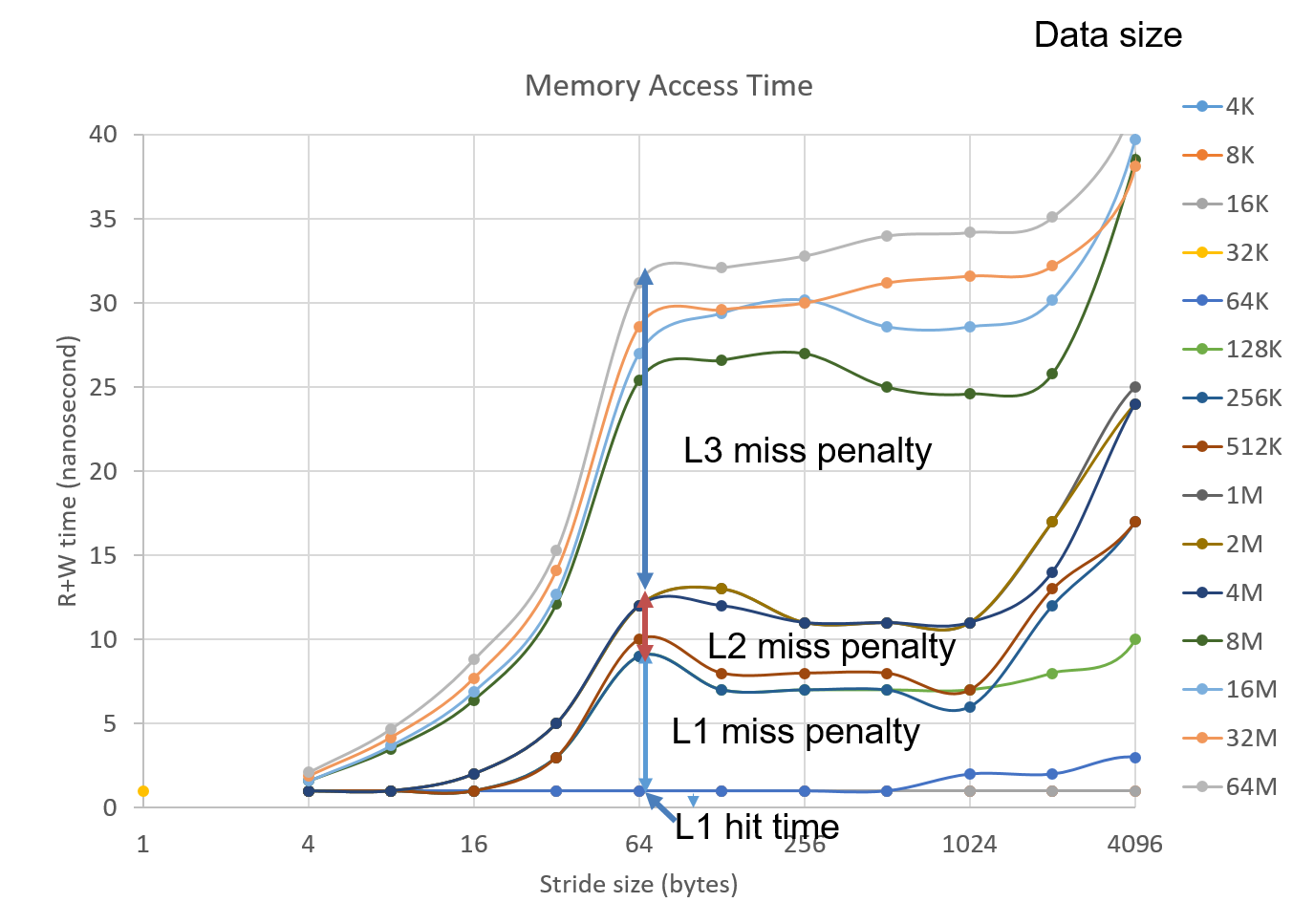


Fig2. Cache performance for Machine II

Include the following information in your report.

1. The manufacturer, model, CPU clock of the processor on the computer. For example, Machine I shown in figure 1 is AMD Opteron(tm) Processor 2380. Its clock is 2.5GHz. You can find this info with Linux command “cat /proc/cpuinfo”.
2. Available physical memory hierarchy on the computer. For example, Machine I has 8GB DRAM memory. You can find this info with Linux command “cat /proc/meminfo” to get memory size and other memory property information, and use command “getconf -a| grep CACHE” to get cache information.
3. Compile memory.c and run it on the computer, and use the results to draw a graph that is similar as Figure 1. Figure 2 illustrates how to get the cache performance. Note: read the program before your compile. According to the results and the graph, provide the following information as a table in your report.
   1. Levels of caches on the computer. A typical computer today should have 2 or 3 levels of caches, which are built of SRAM. If you are not sure, confirm them with specifications of the processor you can find online. If there is no L3 cache on the computer, fill in “NA” in the corresponding cells.
   2. The size of each memory level. Again, confirm your answer with specifications, and note how they are reflected in the plot.
   3. L1 cache access time, and the miss penalty time for L1, L2, L3, and TLB.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | L1 | L2 | L3 | Main Memory |
| Size (Bytes) |  |  |  |  |
| access time (ns) |  | X | X | X |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | L1 | L2 | L3 | TLB |
| Miss penalty (ns) |  |  |  |  |

Submit your report to canvas on time.