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Hardware Description Document

SKARAB MOTHERBOARD

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Approvals

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Contents

1. Introduction

1.1. Scope and Limitations

This document provides an intended detailed description of the SKARAB Motherboard. It provides a means of addressing the requirements as laid out in the Hardware Requirements Document.

1.2. Applicable Documents

- Hardware Detailed Design Spreadsheet (HDDS) for the SKARAB Motherboard.
- Hardware Requirements Document (HRD) for the SKARAB Motherboard.

1.3. Document Layout

Section 1 reflects the content of the document, and provides the reader with associated reference material.
Section 2 details the hardware description.

2. Hardware Description

The design considerations for each of the key interfaces and modules of the SKARAB Motherboard will now be discussed.

2.1. Clock Distribution

The following block diagram illustrates the major components of the clock distribution circuitry:

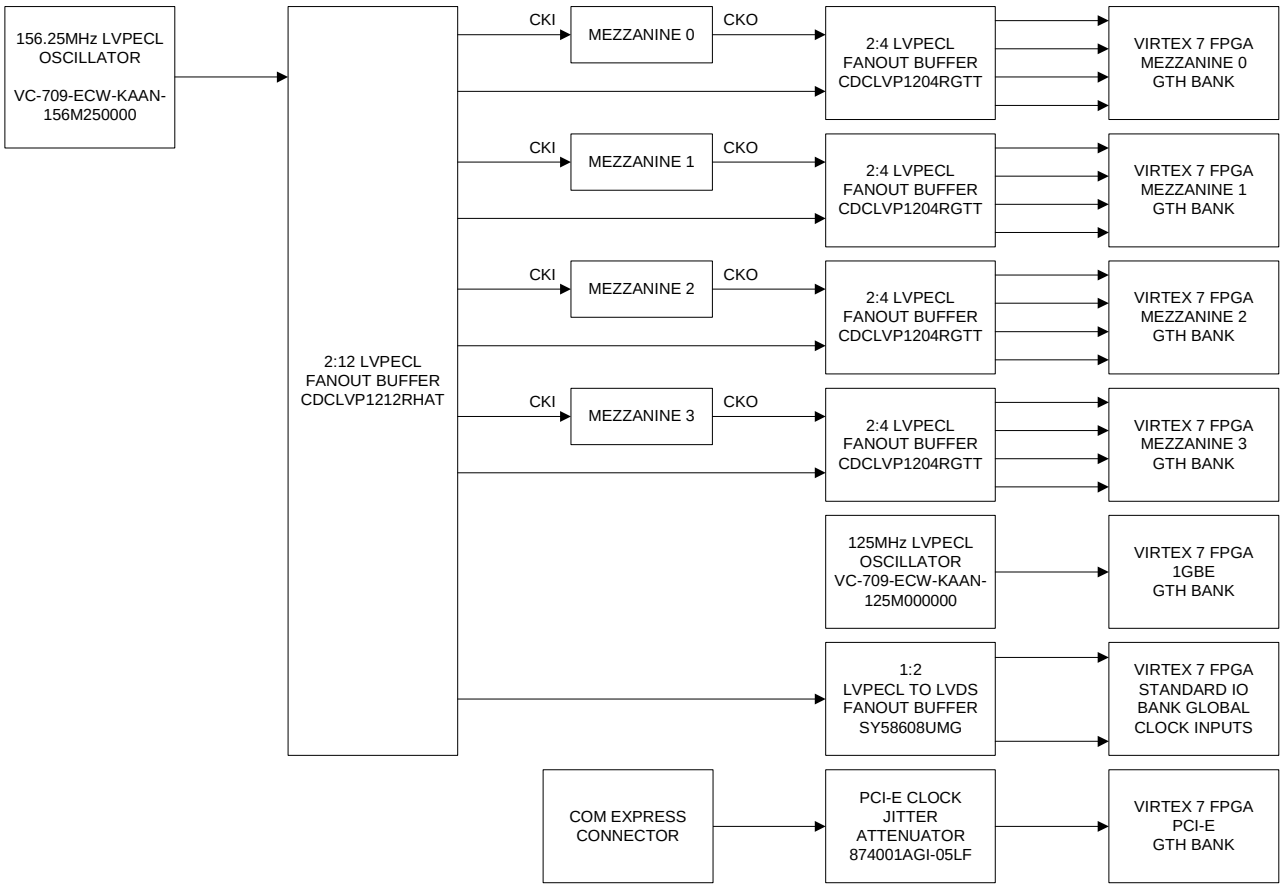

Figure 1: Clock Distribution Block Diagram

40GBE poses strict requirements on the reference clock source. These requirements come from both the FPGA GTH transceivers used and the 40GBE 'PHY' situated on the mezzanine module. These requirements include:

- Large clock signal swing with fast rise and fall time
- 156.25MHz clock source
- +/-100ppm clock tolerance
- 45% to 55% duty cycle
- Low jitter (less than 1ps RMS from 12kHz to 20MHz)

LVPECL was chosen as the clock signaling standard as it offers large signal swing with typically low jitter. Xilinx recommend using LVPECL as the clock signaling standard when providing clocks to the dedicated GTH reference clock inputs.

A very low phase noise 156.25MHz oscillator generates the reference clock on the SKARAB Motherboard. A 2:12 LVPECL fanout buffer distributes this clock to the four mezzanine sites. This 2:12 fanout buffer has a very low additive jitter specification. The 156.25MHz clock is also optionally

distributed to the Virtex 7 GTH banks as follows: a 2:4 LVPECL fanout buffer provides the option of either connecting the reference clock from each mezzanine site to the corresponding Virtex 7 GTH bank or the SKARAB Motherboard reference clock. This 2:4 fanout buffer has a very low additive jitter specification. This 2:4 fanout buffer also fulfills the requirement that each Virtex 7 GTH quad (of which there are four in each bank) requires it own copy of the reference clock. The FPGA controls the selection between whether the SKARAB Motherboard 156.25MHz clock is fed to a GTH bank or whether the clock provided from the mezzanine is fed to a GTH bank. So for example, the QSP+ mezzanine requires a 156.25MHz reference clock.

A 125MHz LVPECL oscillator also connects to the Virtex 7 GTH bank which contains the SGMII connection to the 1GBE PHY. Although it is possible to use a 156.25MHz reference clock with SGMII, this does complicate the firmware requirements and imposes limitations on the FPGA firmware which can be difficult to meet depending on the complexity of the design.

A PCI-E clock jitter attenuator cleans up the PCI-E reference clock from the COM Express connector and connects it to the Virtex 7 GTH bank which contains the PCI-E connection to the COM Express.

Lastly, the Virtex 7 FPGA does not support LVPECL on it's FPGA banks. An LVPECL to LVDS translator is used to convert the 156.25MHz reference clock to LVDS so that it can connect to the global clock pins of the FPGA. These will be the 'system clocks' within the FPGA firmware. If other frequencies are required for specific firmware components within the FPGA then an MMCM within the FPGA can be used to generate these frequencies from the 156.25MHz.

2.2. I2C Monitoring and Fan Control

The following block diagram illustrates the major components of the I2C monitoring and fan control circuitry:

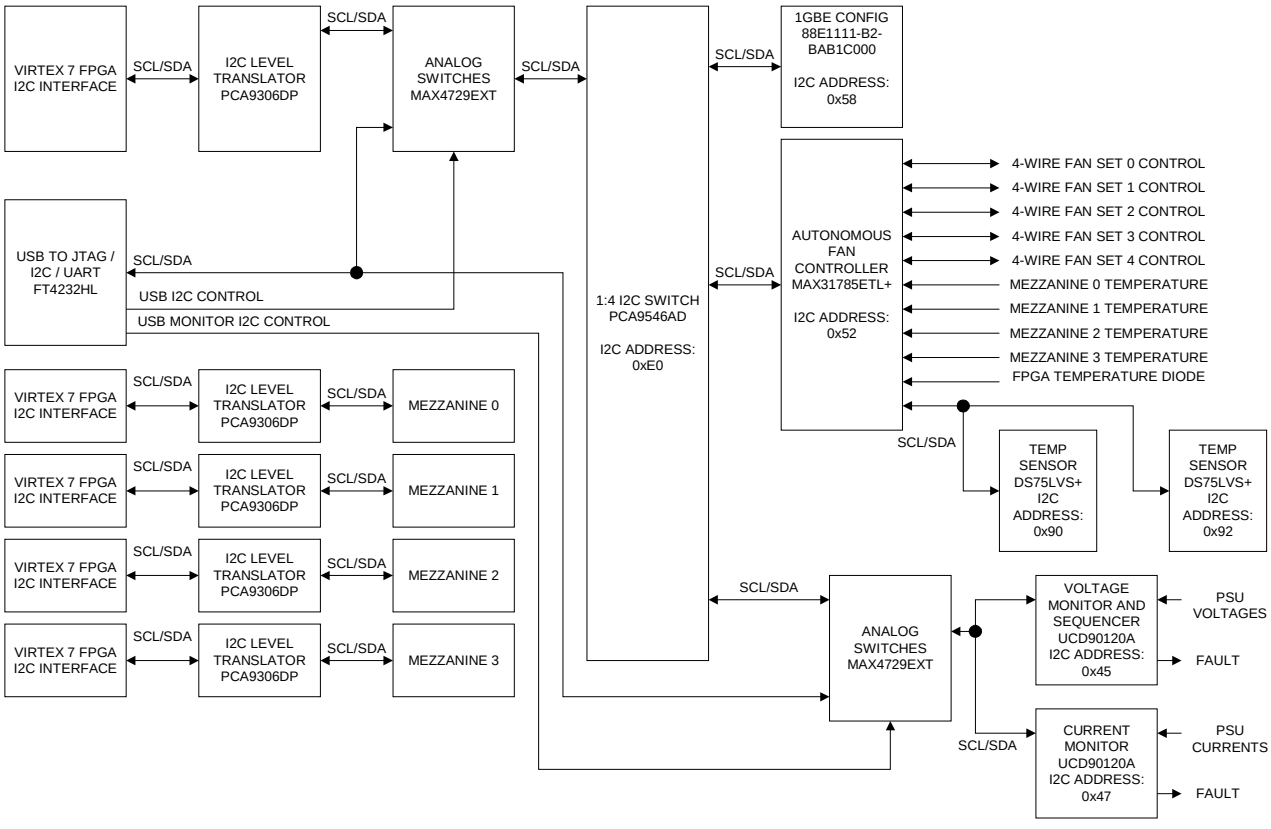

Figure 2: I2C Monitoring and Fan Control Block Diagram

The Virtex 7 FPGA has five I2C interfaces implemented in firmware. These I2C interfaces are at +1V8. I2C level translators step this interface up to +3V3.

There is a USB PHY on the ROACH3 Motherboard. This USB PHY provides three separate interfaces:

- JTAG
- I2C
- UART

This USB PHY can be used to control the SKARAB Motherboard I2C bus from the host. Analog switches connect either the FPGA or the USB PHY as the I2C master. By default, the FPGA is the master of the I2C bus. When the host requires control of the I2C bus, a signal from the USB PHY toggles the analog switches. This control signal is also fed to the FPGA so that it knows not to attempt any further I2C accesses while the USB PHY is the I2C master. The USB PHY also has the option of a direct I2C connection to the voltage and current monitor. This is used when the board is in standby to read the fault logs off the voltage and current monitor.

A 4-way I2C switch isolates the different sections of the I2C bus. This helps to minimize bus capacitance and also limit the chance of an I2C address collision.

All four mezzanine sites have I2C interfaces. The mezzanine I2C interface is at +3V3.

The 1GBE ETH PHY can be accessed via the I2C bus. This interface is unlikely to be used, as the default configuration of the 1GBE is set via bootstrapping pins at start up. The default configuration of the 1GBE ETH PHY is as follows:

- Auto negotiation enabled, advertise all abilities, preferably slave
- Support for automatic crossover
- SGMII to MAC with copper external interface

The voltage monitoring device monitors the voltages of the different on-board PSUs. The voltages from the PSUs are scaled to within the input range of the voltage monitoring device analog input pins. The load current of the on-board PSUs are sensed using current sense resistors. The voltage drop across the current sense resistors is amplified before being connected to the current monitoring device analog input pins. Both the voltage monitoring device and current monitoring device have programmed thresholds. If these thresholds are exceeded then a shutdown of the SKARAB LRU is initiated.

The autonomous fan controller is connected to the I2C bus. This will be used to configure the device during production. It will also allow the host to read back temperatures and fan speeds. Once configured, the fan controller does not require input from the host to control the different fan speeds within the SKARAB LRU. It takes as inputs the following temperature readings:

- Two remote temperature sensor devices connected to a dedicated I2C bus. The fan controller is the master of this I2C bus. One of these temperature sensors will be situated on the motherboard near the inlet. The second will be situated on the motherboard near the outlet.
- Virtex 7 FPGA diode temperature.
- Four mezzanine site temperatures represented at voltages in the range of 0 to +2V.

Using these temperatures as inputs, it is possible to set up ratios between the input temperatures and the desired fan speeds. Also, support for different regions within the SKARAB LRU is provided. This fan controller is designed to work with 4-wire fans. The default configuration for the fan controller is to set the three inlet fan pairs to 20%, the outlet fan pair to 30% and the FPGA fan to 100%.

2.3. AUX, GPIO and 1-wire Interfaces

The following block diagram illustrates the major components of AUX, GPIO and 1-wire interface circuitry:

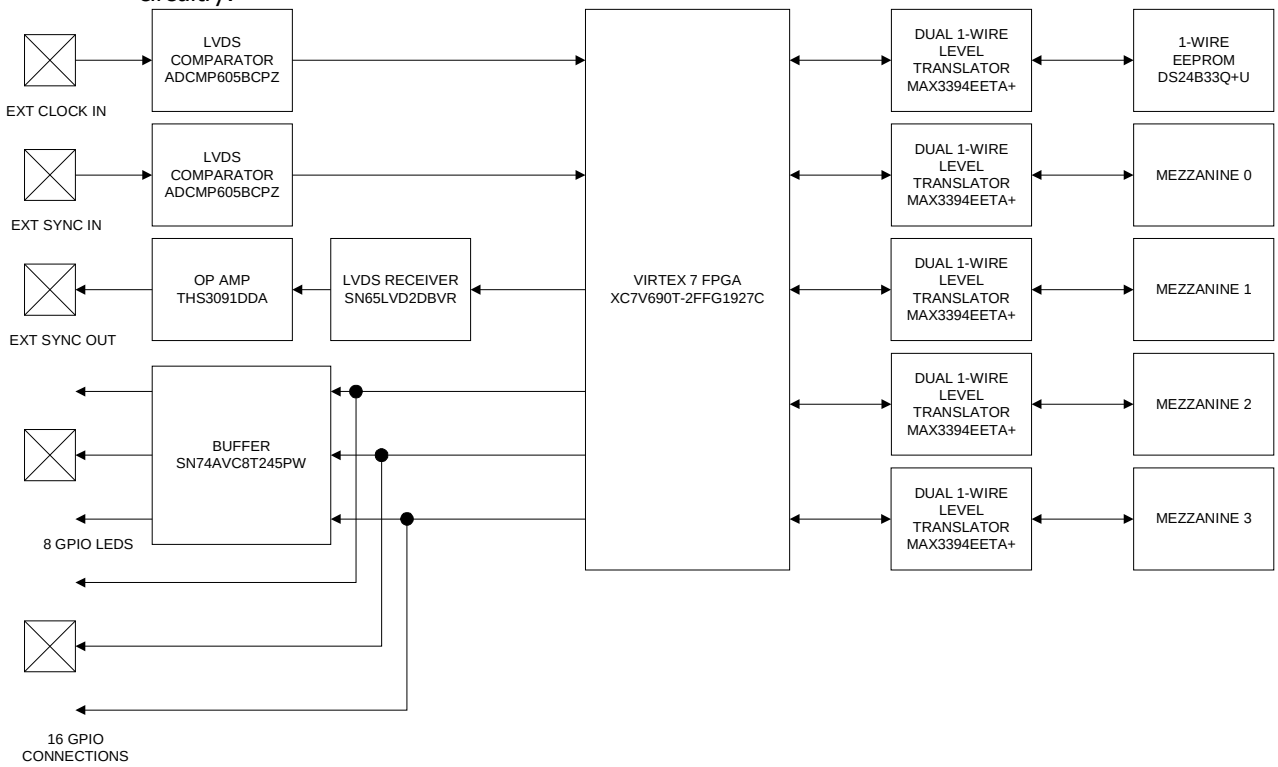

Figure 3: AUX, GPIO and 1-wire Interface Block Diagram

A 1-wire EEPROM will be used on the SKARAB Motherboard and each mezzanine to store a unique 64-bit serial number. This number will be programmed during production. The Virtex 7 FPGA will have five 1-wire interfaces implemented in firmware. The FPGA 1-wire interfaces will be at +1V8. A dual 1-wire level translator will be used to step this voltage up to +3V3 because most 1-wire devices operate at +3V3. Provision will also be made for enabling a strong pull-up. The strong pull-up is required to provide the necessary current to the EEPROM during programming.

Provision is made on the SKARAB Motherboard to connect an external clock input via an SMA connector. This clock is converted to LVDS before being connected to the Virtex 7 FPGA. Provision is made on the SKARAB Motherboard to connect an external synchronization input via an SMA connector. This signal is converted to LVDS before being connected to the Virtex 7 FPGA. Provision is made to output a synchronization signal from the SKARAB Motherboard via an SMA connector. An LVDS signal from the Virtex 7 FPGA is converted into a single ended signal and then amplified before being output.

Status information is provided via eight front panel status LEDs. These are sourced from the Virtex 7 FPGA and are buffered before driving the LEDs. 16 Virtex 7 GPIO signals are also available via two IDC headers.

2.4. Virtex 7 FPGA GTH Connections

The following block diagram illustrates the major Virtex 7 FPGA GTH connections:

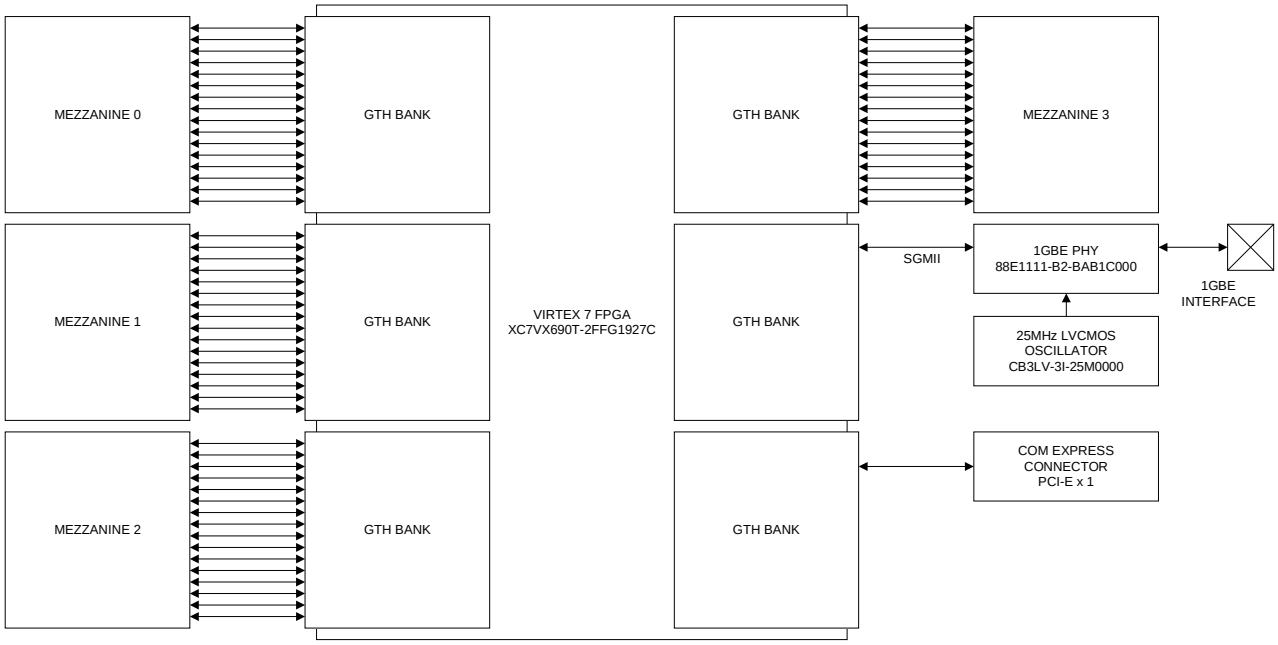

Figure 4: Virtex 7 FPGA GTH Connection Block Diagram

Each GTH bank on the Virtex 7 FPGA supports four GTH quads with each quad having four high speed serial interfaces. All 16 of the high speed serial interfaces from each GTH bank are routed to the connected mezzanine site. A single high speed serial interface is used as an SGMII interface to the 1GBE PHY. A single high speed serial interface is used as a 1x PCI-E interface to the COM Express.

2.5. Virtex 7 FPGA Configuration

The following block diagram illustrates the major Virtex 7 FPGA configuration components:

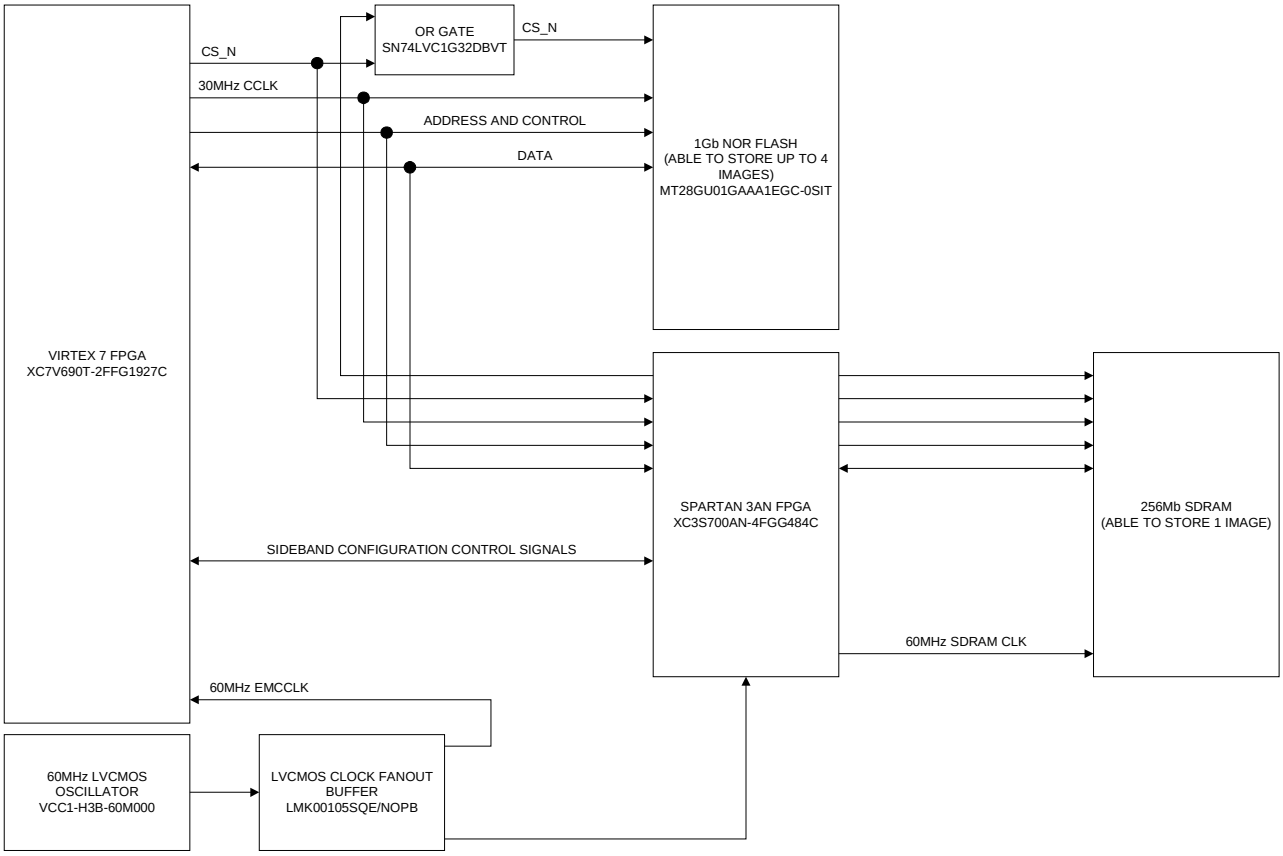

Figure 5: Virtex 7 FPGA Configuration Block Diagram

The Virtex 7 FPGA on the SKARAB Motherboard is initially configured from a 1Gb NOR flash device using BPI fast configuration. This device is able to store up to four images although only two of these images will be used. The first image will only be programmable via JTAG. This will be the golden image. The second image will be programmable via JTAG and in-system via the 1GBE interface. This flash is used to store the 'static' FPGA images – the FPGA configuration images that do not change very often.

The SKARAB LRU also has a requirement to load a new FPGA image every 20 minutes. This image must be programmable via the 1GBE interface. This imposes the following requirements:

- The memory used to store the image should not experience wear
- The memory used must be programmed and the FPGA booted within approximately 1 second

These requirements cannot be achieved through non-volatile memory. Consequently, a 256Mb SDRAM is used on the SKARAB Motherboard to store these 'dynamic' images. Because the Virtex 7 FPGA does not support booting from an SDRAM device, a Spartan 3AN FPGA will be used to convert the SDRAM interface into a standard parallel NOR flash interface.

The Spartan 3AN FPGA has an embedded SPI flash device to store it's configuration data. As a result, it configures automatically at start up. It is envisioned that this flash device will only be programmed once during production. Provision will be made to support in-system programming.

The boot procedure is as follows:

- The SKARAB Motherboard PSUs are ramped up sequentially. Once the final PSU in the sequence is running, the Spartan 3AN FPGA is allowed to boot from it's internal SPI flash device.
- Once the Spartan 3AN FPGA has booted, the Virtex 7 FPGA is allowed to boot.
- The Spartan will initial set the boot selection control to '0'. This will select the parallel NOR

flash rather than the Spartan 3AN FPGA.

- The RS lines of the Virtex 7 FPGA are connected to the two most significant address bits of the parallel NOR flash. There are pull-up resistors on these address lines so by default, the fourth image address space is selected in the parallel NOR flash.
- The Virtex 7 FPGA will start in asynchronous read mode to load the configuration data from the parallel NOR flash. Embedded in the configuration bit stream will be the option to switch to using the synchronous read mode.
- The Virtex 7 FPGA will write to the parallel NOR flash configuration register to put the NOR flash in synchronous read mode. It will then switch to the synchronous read mode and reload it's configuration image from the parallel NOR flash.
- The multiboot image is now loaded on the Virtex 7 FPGA. If there was a problem booting from the multiboot image (for example, the image was corrupted during in-system reprogramming), then the Virtex 7 FPGA will drive the RS lines low and will start the configuration cycle again. Now the golden image will be selected (first image address space in the parallel NOR flash). This guarantees that the Virtex 7 FPGA will always be able to boot an image.
- The Virtex 7 FPGA will now be running.
- At some point, the host will start loading a 'dynamic' FPGA configuration image into the SKARAB LRU.
- The parallel flash bus can be controlled through FPGA firmware after configuration completes. The FPGA firmware will now ensure that the Spartan 3AN FPGA is selected and will start sending the configuration data to the Spartan 3AN FPGA over the parallel flash bus. Dedicated sideband signals between the Virtex 7 FPGA and the Spartan 3AN FPGA will indicate to the Spartan 3AN FPGA that it is in a programming phase and that the data provided must be written to the SDRAM device.
- Once the FPGA configuration image has been downloaded to the SDRAM, a reconfiguration of the Virtex 7 FPGA can be initiated using the ICAPE2 firmware component.
- Now the Spartan will have latched the Spartan select high so that the Spartan 3AN will be selected and the configuration cycle will start again.
- As before, the Virtex 7 FPGA will start in asynchronous read mode. The Spartan 3AN FPGA will emulate an asynchronous read response. Embedded in the configuration bit stream will be the option to switch to using the synchronous read mode.
- The Virtex 7 FPGA will write to the configuration register to select the synchronous read mode. The Spartan 3AN FPGA will identify this write and will switch to synchronous read mode itself. Now when the Virtex 7 FPGA loads it's configuration image the Spartan 3AN FPGA will emulate a synchronous read response.
- If there is any problem loading the 'dynamic' FPGA image, the Virtex 7 FPGA will drive the RS lines low and the golden image will be loaded from the parallel NOR flash.

Using a SDRAM device imposes a couple of limitations:

- The SDRAM device must be refreshed at a regular rate.
- Data must be read from and written to the SDRAM device in bursts.
- Rows within the SDRAM must be activated before they can be read or written and must be pre-charged once reading or writing is complete.

To account for these limitations, the parallel flash bus will operate at a lower frequency than the SDRAM bus. A 60MHz LVCMOS oscillator will provide a 60MHz clock to the EMCCLK pin of the Virtex 7 FPGA. The 60MHz clock will also be connected to the Spartan 3AN FPGA. The 60MHz EMCCLK will be divided by two in the Virtex 7 FPGA and so the synchronous parallel flash bus will operate at 30MHz. In contrast, the SDRAM bus will operate at 80MHz (generated from the 60MHz by a DCM in the Spartan FPGA).

In addition to the difference in clock frequencies, the Spartan 3AN FPGA will cache a portion of the configuration image in it's own embedded BRAM components. This will ensure that even if a refresh of the SDRAM is required during configuration, sufficient data will be cached to ensure that there are no breaks.

The Virtex 7 FPGA supports compressed FPGA images. Compressed FPGA images will be used to reduce the amount of time required to program and boot.

2.6. JTAG

The following block diagram illustrates the major JTAG components:

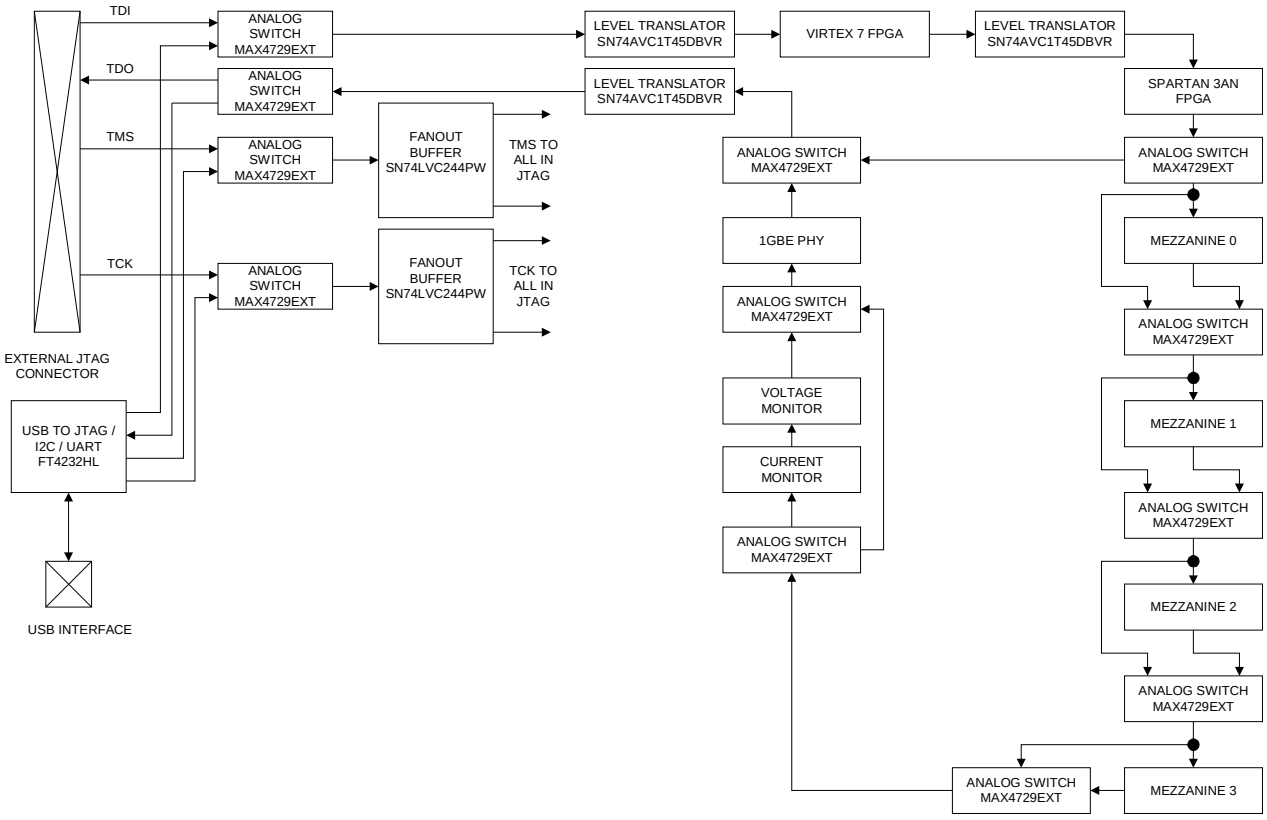

Figure 6: JTAG Block Diagram

The SKARAB Motherboard has a JTAG chain. This JTAG chain provides the following functionality:

- Program the golden image in the parallel NOR flash. The Xilinx iMPACT tool does this by loading a JTAG to flash bridge image in the Virtex 7 FPGA.
- Program the SPI flash in the Spartan 3AN FPGA.
- Provide as much test coverage of PCB connections as possible through boundary scan testing.

The JTAG bus is accessible through two methods:

- A dedicated JTAG header is provided on the SKARAB Motherboard. The connections on this header are compatible with the Xilinx Platform Cable USB programmer. The connections on this header are also compatible with other JTAG controllers (such as XJLink from XJTAG and the JTAG controllers from JTAG Technologies). This JTAG interface is at +3V3.
- A USB PHY on the SKARAB Motherboard can be used to control the JTAG chain.

Analog switches on theSKARAB Motherboard select between the external JTAG master and the USB PHY device. By default, the external JTAG header is connected. The USB PHY device controls which of the two masters is connected to the JTAG chain.

The Virtex 7 FPGA JTAG interface pins are at +1V8 so a level translator is used to step the voltage down to +1V8. After the Virtex 7 FPGA, a level translator is used to step the JTAG chain voltage back up to +3V3. The 1GBE PHY device JTAG output is at +2V5 (the JTAG input is +3V3 compatible). A level translator is used to step the JTAG chain voltage back up to +3V3.

The TMS and TCK signals are buffered by fanout buffers so that each component in the JTAG chain receives it's own copy of TMS and TCK. This is to optimize signal integrity so that the JTAG can operate at the highest clock frequency supported by the devices connected.

The mezzanine sites are included in the JTAG chain. An analog switch automatically bypasses the mezzanine site when a mezzanine module is not plugged in. Zero ohm jumper resistors are included throughout the JTAG chain to optionally bypass individual components in the JTAG chain. Analog switches also provide the option of shortening the JTAG chain.

2.7. Power Button, Reset Button and Automatic Fault Handling

The following block diagram illustrates the major power button, reset button and fault handling components:

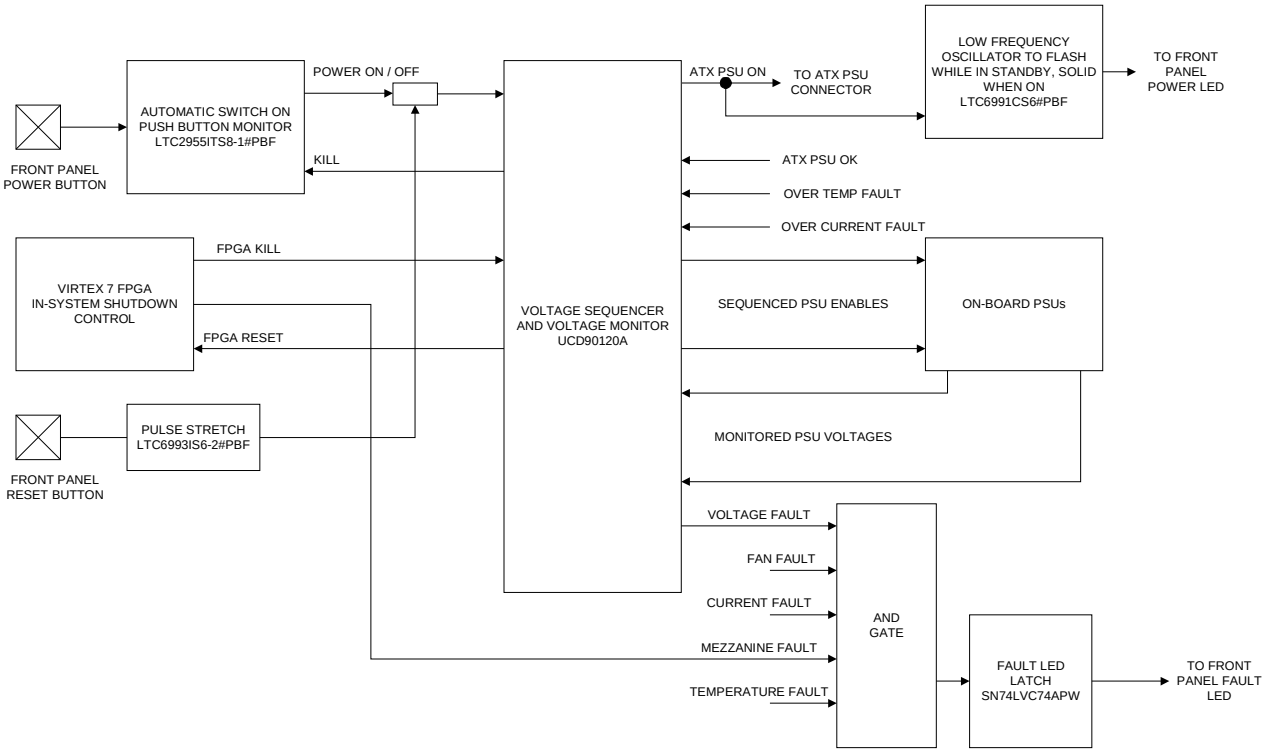

Figure 7: Power Button, Reset Button and Automatic Fault Handling Block Diagram

The SKARAB LRU has an ATX power supply. This provides a +5V standby voltage. When the AC input is connected this voltage goes comes up. A push button monitor is used on the SKARAB Motherboard which switches on under the following conditions:

- A power button is pressed
- Voltage is first applied

An intelligent voltage monitoring and sequencing device handles all the power up and power down sequencing of the SKARAB LRU. It sequences the switching on of the ATX power supply as well as all the on board power supplies. It provides basic logic that constructs a kill signal to the push button monitor. This kill signal is asserted in the following situations:

- ATX PSU OK signal not asserted
- Over temperature fault
- Over current fault
- Out of range voltage (measured by the voltage monitor itself)
- Kill request from the FPGA

These faults are only monitored after a certain power-on time has elapsed to allow voltages to stabilize. A latch ensures that the fault event is captured and the fault LED stays on after the ATX power supply switches off. This latch is only reset when the user triggers a start up of the SKARAB LRU by pushing the power button or power cycling the AC.

The power status of the SKARAB LRU is given through two front panel LEDs. The power LED flashes slowly when only the +5V standby voltage is present. Once the SKARAB LRU is switched on, the power LED is solid on. There is also a front panel reset button. The reset button triggers a sequenced shutdown and then starts up all the power supplies again (including the ATX power supply). A pulse stretcher ensures that the power supplies are off long enough for all the voltages to decay to roughly 0V before sequencing the power supplies back on again.

3. Test Procedure

The SKARAB motherboard ATP document (ATP-123702) details the full procedure for programming and testing a SKARAB motherboard.