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Hardware Description Document

ROACH3 QSFP+ MEZZANINE

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1. Introduction

1.1. Scope and Limitations

This document provides an intended detailed description of the ROACH3 QSFP+ Mezzanine Card. It provides a means of addressing the requirements as laid out in the Hardware Requirements Document.

1.2. Applicable Documents

- Hardware Detailed Design Spreadsheet (HDDS) for the ROACH3 QSFP+ Mezzanine (PX123801).
- Hardware Requirements Document (HRD) for the ROACH3 QSFP+ Mezzanine (PX123801).

1.3. Related Documents

- Hardware Description Document (HDD) for the ROACH3 QSFP+ PHY Mezzanine (PX123901).
- Hardware Description Document (HDD) for the ROACH3 Motherboard (PX123701).
- Hardware Requirements Document (HRD) for the ROACH3 Motherboard (PX123701).

1.4. Document Layout

Section 1 reflects the content of the document, and provides the reader with associated reference material.
Section 2 details the hardware description.

2. Hardware Description

The requirements for the QSFP+ Mezzanine are described in the Roach3 Tender Requirements document and the Hardware Requirements Document (HRD) for this board.

The design is deemed complex due to the very strict signal integrity requirements laid out by the IEE802.3-2012 standard. This is described in depth in section 2.3 below.

A block diagram of the board will be presented, after which the critical design considerations will be discussed.

2.1. Block Diagram

Figure 2-1 below shows the block diagram of the ROACH3 QSFP+ Mezzanine.

The board directly connects four XLPPI interfaces provided by the motherboard (implemented on GTH quads on the Virtex 7) on the FCI 84740-202LF connector to each of the four ports of a four-port ganged QSFP connector.

An STM32F205RGT6 microprocessor is used to perform management of the four QSFP+ transceivers (using the low speed control pins: ModSelL, ResetL, LPMode, ModPrsL, IntL, SCL and SDA) and drive the QSFP+ link status LEDs. The mezzanine I2C interface is able to interrogate the microprocessor to fetch status from the processor.

A DS24B33 EEPROM is provided on the mezzanine 1-wire interface to store mezzanine identification information.

A voltage regulator is used to provide 3.3V power to the QSFP+ transceivers and the microprocessor

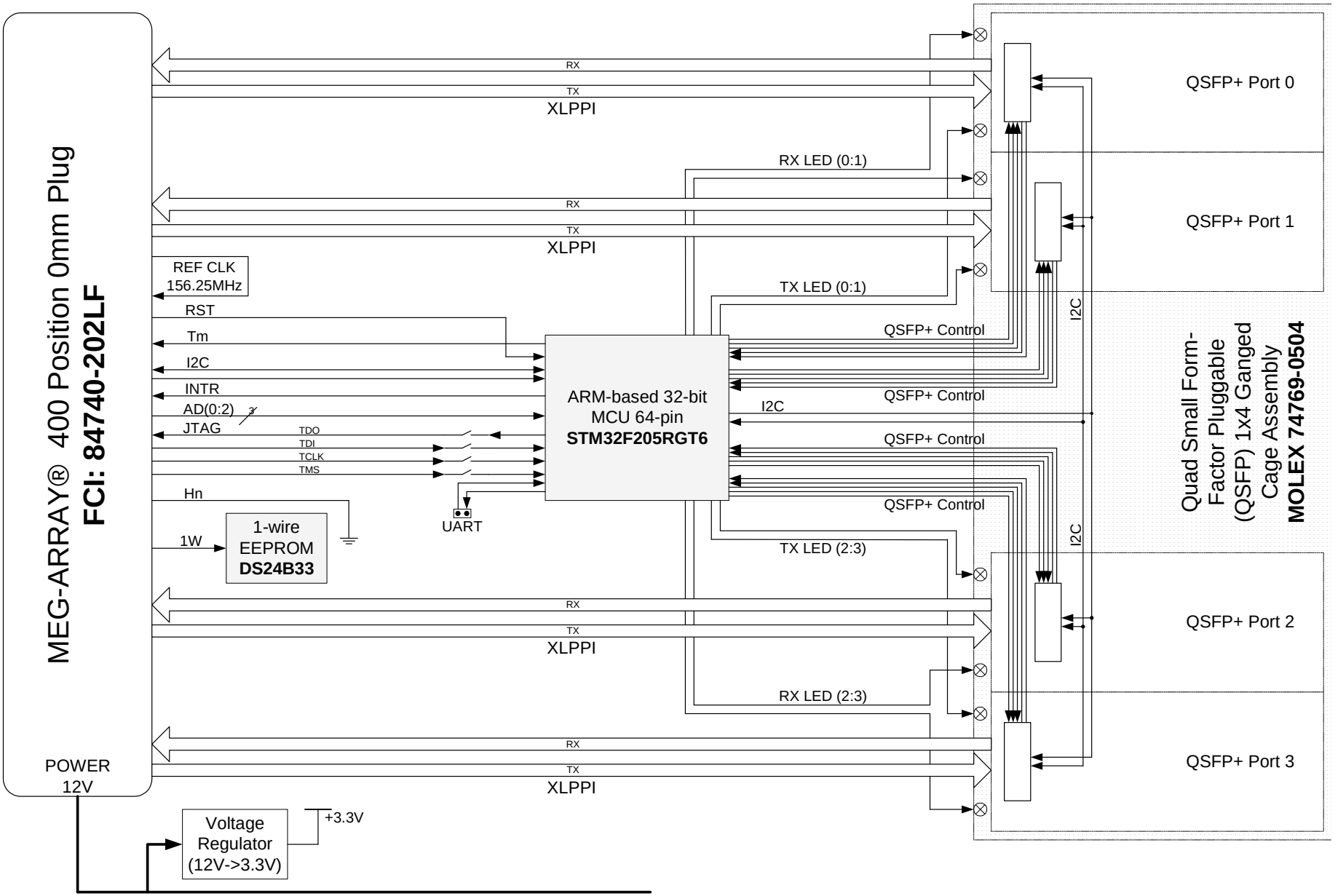

Figure 2-1: Block Diagram of ROACH3 QSFP+ Mezzanine

2.2. Reference Clock

There are no components on the QSFP+ Mezzanine that require a reference clock.

2.3. High-speed data signals

There are two common interfaces used to talk to 40GbE Ethernet transceivers.

1. The 40Gbps Attachment Unit Interface (XLAUI) is a 4 lane serial interface designed to talk across PCB traces between 2 different Physical Medium Attachment (PMA) Units.
2. The 40Gbps Parallel Physical Interface (XLPPI) is a 4 lane serial interface designed as a service interface to a Physical Medium Dependant (PMD) Unit. It interfaces a PMA to a PMD.

The difference between XLAUI and XLPPI are the signal integrity requirements. The requirements of XLAUI are similar to those of XFI which are both host side interfaces. The requirements of XLPPI are far stricter, and are similar to those of SFI since they are both line side interfaces. These differences are illustrated by Figure 2-2 below and Table 2-1 below.

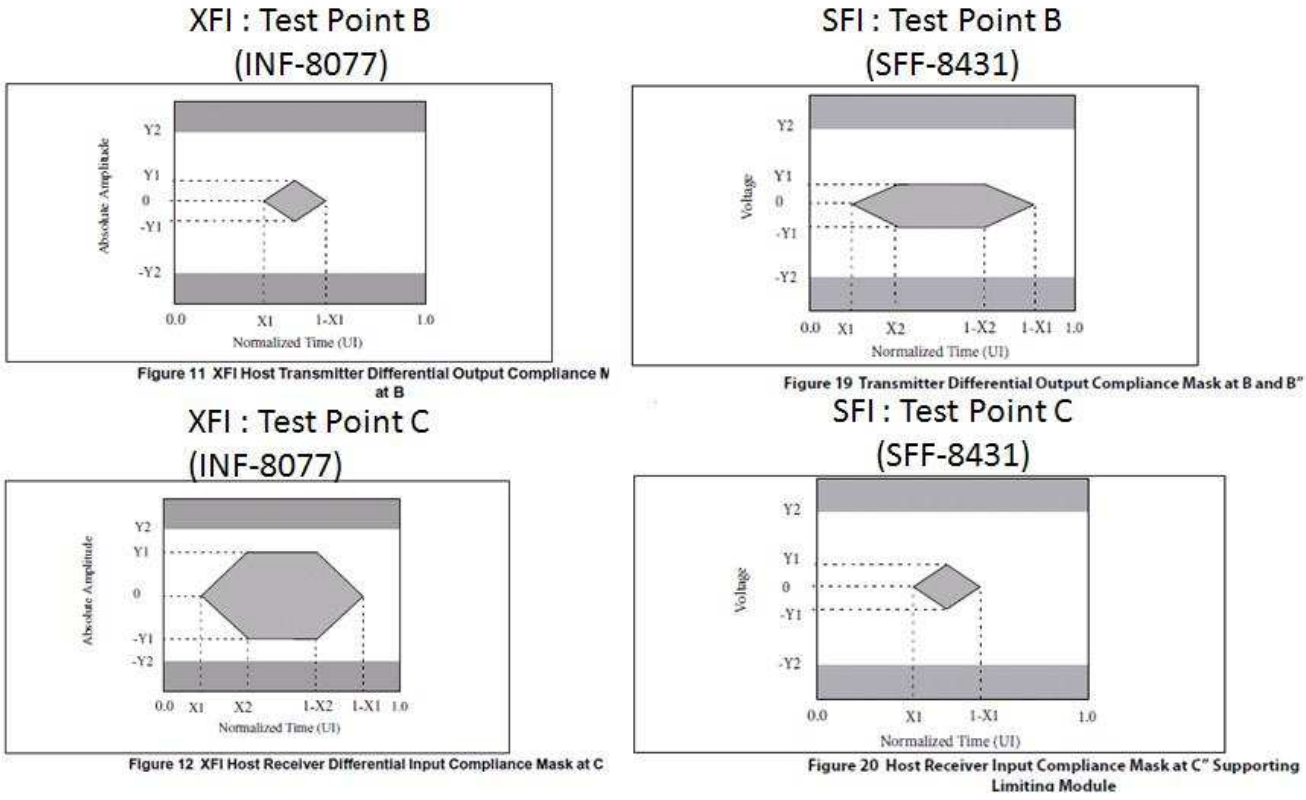

Figure 11 XFI Host Transmitter Differential Output Compliance N at B

Figure 19 Transmitter Differential Output Compliance Mask at B and B"

Figure 12 XFI Host Receiver Differential Input Compliance Mask at C

Figure 20 Host Receiver Input Compliance Mask at C" Supporting Limiting Module

Figure 2-2: Eye diagram of SFI vs XFI

	Interface comparison TX (MAC to Module)								
	MAC Interface (Output)					Module Interface (Input)			
	Interface	XFI	SFI	XLAUI	XLPPI	XFI	SFI	XLAUI	XLPPI
	Spec.	INF-8077	SFF-8431	802.3ba	802.3ba	INF-8077	SFF-8431	802.3ba	802.3ba
Parameters	X1	0.15UI	-	0.16UI	-	0.305UI	0.12UI	0.31UI	0.11UI
	X2	0.4UI	-	0.38UI	-	0.5UI	0.33UI	0.5UI	0.31UI
	Y1	180mV	-	200mV	-	60mV	95mV	42.5mV	95mV
	Y2	385mV	-	385mV	-	410mV	350mV	425mV	350mV
	Jitter	0.3UI	-	0.32UI	-	0.61UI	0.28UI	0.62UI	0.29UI
	Interface comparison RX (Module to MAC)								
	MAC Interface (Input)					Module Interface (Output)			
	Interface	XFI	SFI	XLAUI	XLPPI	XFI	SFI	XLAUI	XLPPI
	Parameter	INF-8077	SFF-8431	802.3ba	802.3ba	INF-8077	SFF-8431	802.3ba	802.3ba
Parameters	X1	0.325UI	-	0.31UI	-	0.17UI	0.35UI	0.2UI	0.29UI
	X2	0.5UI	-	0.5UI	-	0.42UI	0.5UI	0.5UI	0.5UI
	Y1	55mV	-	42.5mV	-	170mV	150mV	136mV	150mV
	Y2	525mV	-	425mV	-	425mV	425mV	380mV	425mV
	Jitter	0.65UI	-	0.62UI	-	0.34UI	0.7UI	0.4UI	0.65UI
	DDPWS	-	-	-	-	-	0.34UI	-	0.34UI

Table 2-1: Comparison of Parameters for XLAUI vs XLPPI

The Motherboard coupled with the Mezzanine (including all trace routing on both boards and signal distortion related to the mezzanine connector) must provide an XLPPI interface at the QSFP+ connectors. The Xilinx 7 series Transceiver wizard is able to generate an XLAUI interface, but does not specifically support XLPPI.

It is common practice to use a dedicated PHY that is located in close proximity to the QSFP+ cage to implement XLAUI to XLPPI conversion (a number of devices are available from Marvell, Broadcom, Vitesse and Cortina Systems for this purpose).

In the interests of hardware simplicity, this board omits a dedicated PHY. It is currently unclear whether this is viable from a signal integrity perspective, given the surrounding design constraints. First order checks of FPGA transceiver datasheet performance against the XLPPI requirement indicate that signal integrity is marginal. Simulation and hardware verification are urgently required to mitigate risk before this approach can be considered robust.

2.4. QSFP+ Control

The Microcontroller is also responsible for the control and monitoring of the QSFP+ Modules. The amount of control and monitoring is dependant on the Transceiver module in use; however since the QSFP+ modules are expected to abide by the QSFP+ Standard (SFF-8846) the memory map for all transceivers is the same. This means that the same code will be used for all transceivers, but not all functions will be called for all transceivers. A shared I2C bus with separate Module Select lines is used to access all Transceiver Modules on the Mezzanine.

The low speed lines are common to all transceiver modules.

All this is illustrated in Figure 2-3 below.

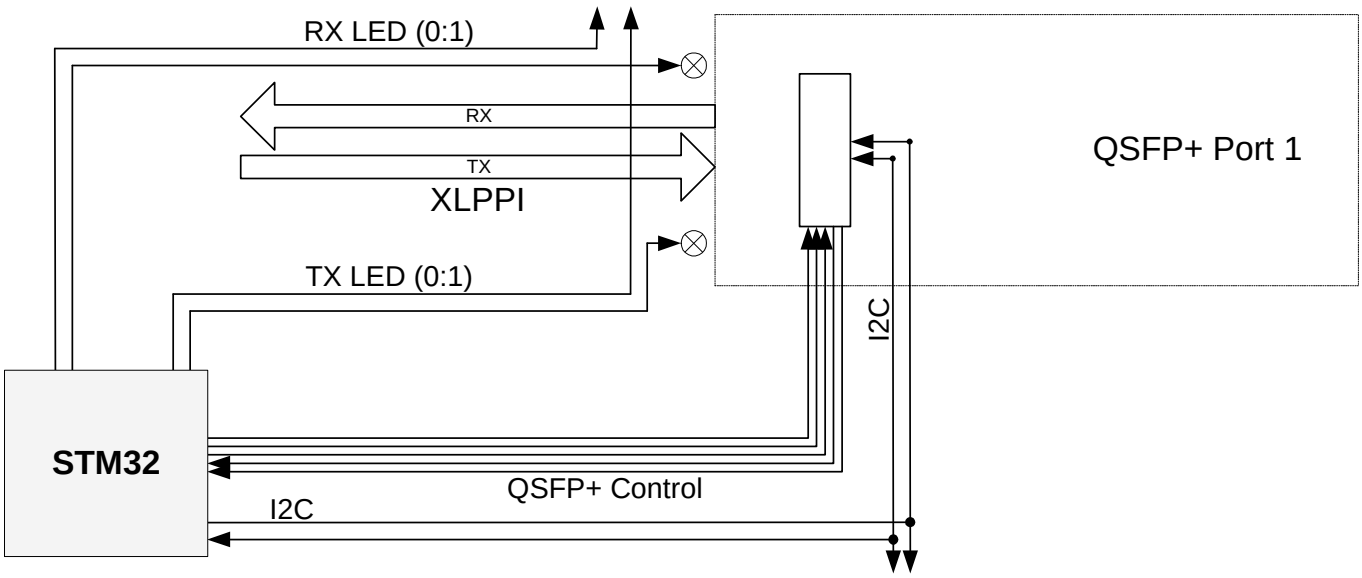

Figure 2-3: Mezzanine QSFP+ Port Control

2.5. STATUS LEDs

The Microcontroller will route 1 GPIO as an output to each of the QSFP+ Transmitter LEDs. This will be used to show the status of the transmit path and will be determined from both the QSFP+ Module and the FPGA.

The Microcontroller will route 1 GPIO as an output to each of the QSFP+ Receiver LEDs. This be used to show the status of the receive path and will be determined from both the QSFP+ transceiver and the FPGA.

The LEDs are illustrated in Figure 2-3 above.

2.6. JTAG Chain

The requirements specify that all components on the Mezzanine card should be connected to the Motherboards JTAG chain which in turn is to be connected to an FTDI USB to JTAG chain. This will be followed, however, this will result in a long JTAG chain that may cause problems when trying to debug and program the Microcontroller. Furthermore, debug access to the microcontroller will be required early on in the design. A set of jumpers will be added between the JTAG chain and the Microcontroller so that an external debugger can be connected directly to the Microcontroller. This is shown in Figure 2-4 below.

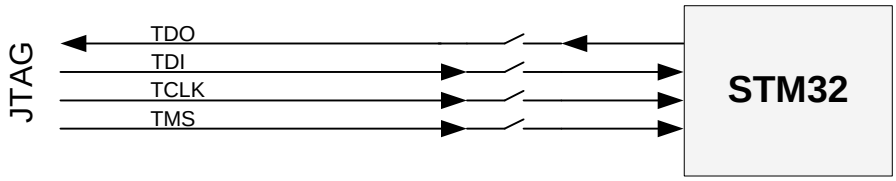

Figure 2-4 : Mezzanine JTAG Chain

2.7. Temperature Monitoring

The microcontroller has an internal temperature monitor which it will monitor itself.
There is a provision in the QSFP+ standard for transceiver modules to measure their own temperature.

The microcontroller will monitor temperatures of all the onboard chips and connected transceivers. This can be read by the motherboard through the Mezzanine I2C.

In addition to this one of the onboard DACs of the microcontroller will be used to provide the Tm pin with a valid output. This is to support standard motherboard temperature monitoring.

2.8. 1-wire EEPROM

The requirements specify that the Mezzanine card must include 1-wire interface which connects to an EEPROM. This will be identical to the motherboard and is illustrated in Figure 2-5 below.

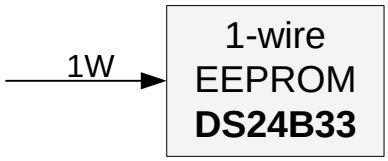

Figure 2-5: Mezzanine 1-wire EEPRO

3. Preliminary Test Procedure

In this section, we will discuss the preliminary test-strategies for the ROACH3 QSFP+ Mezzanine prototypes. The test-setup has been shown in Figure 3-6.

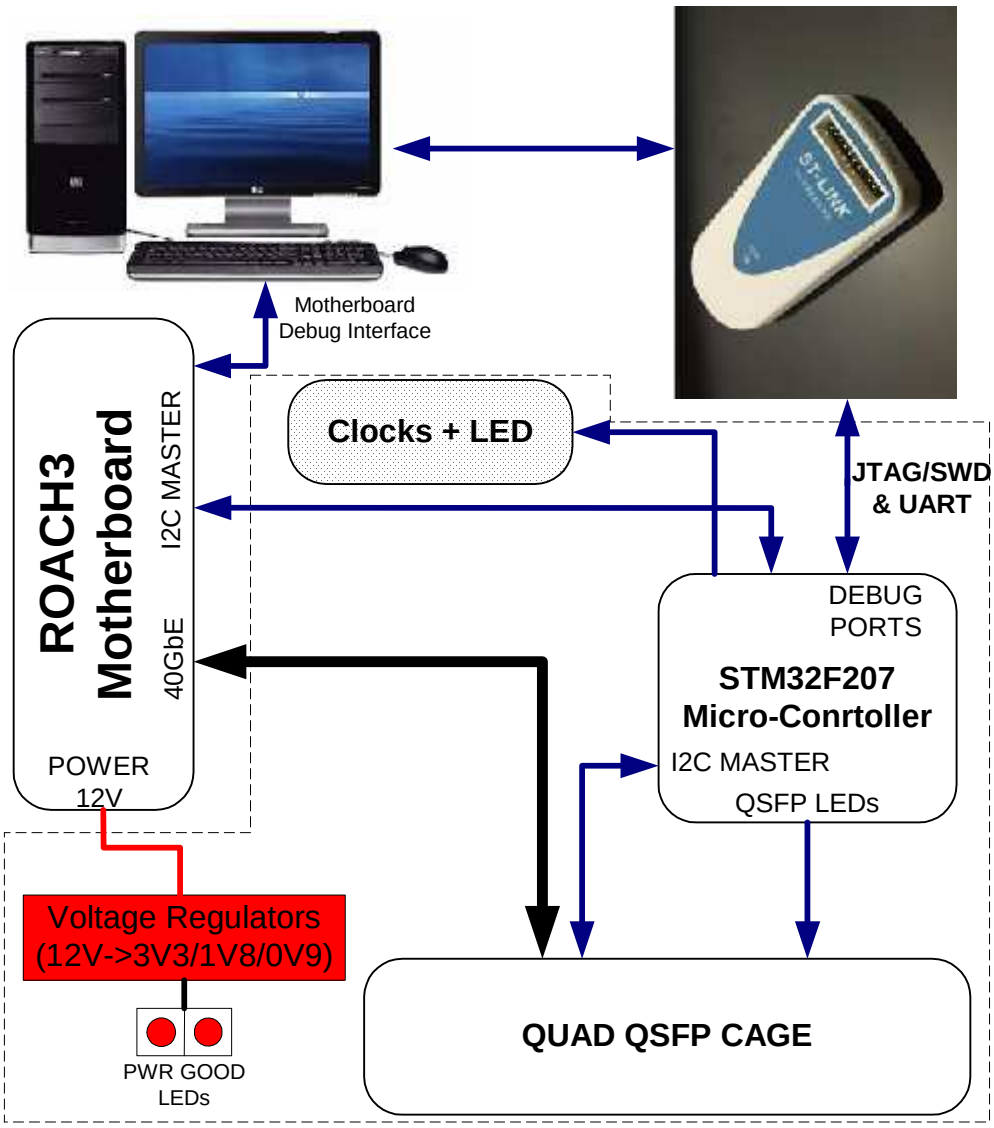

Figure 3-6: Preliminary Test-Setup for the ROACH3 QSFP+ Mezzanine board.

3.1. Board Bring-Up

The process of bringing up the board includes the following steps:

- Check if there is any short on the input power rail, 12V.
- Check if there are any shorts on the output supply rail, 3.3V.
- Isolate the output power supply rail and power-up the board and hence, confirm the output voltage using a digital multi-meter (Power GOOD LED should turn on as well).
- Check the Micro-Controller clock.

3.2. Basic Micro-Controller Testing

After the powering up of the board, the next step is to test the micro-controller and in interfaces by setting up the debug interface.

- Remove the jumpers over the JTAG/SWD connector, thereby isolating the micro-controller from the ROACH3 JTAG chain.
- Connect the JTAG/SWD to the ST-LINK programmer which in turn should be connected to the test PC.

- Connect the STM32 UART to the test PC through an appropriate serial cable.
- Setup the open-OCD or the STM utility to program the micro-controller.
- Perform basic operational tests confirming the correct functioning and configuration of the micr-controller, using serial prints and the debug LED.
- Perform Mezzanine reset.
- Test all the slave peripherals (i.e, the QSFP+ cables) for basic IO read/write operations.

3.3. Standalone Mezzanine functional tests

Once, the peripherals have been tested, the next step is to test the functionality of the complete Mezzanine board as standalone system. These tests include:

- Testing the QSFP+ management firmware. This includes initialization and monitoring of all the QSFP cables through the I2C interface..
- System management firmware. This includes all the system monitoring tasks as well as updating the Mezzanine status registers in order to facilitate the ROACH3 motherboard to access Mezzanine status reports.

3.4. Integration with Motherboard

Finally, after all the standalone tests of the Mezzanine board have been performed, the next task is to integrate the Mezzanine board with the Motherboard and perform complete functional test.

- Reset the Mezzanine using the Motherboard's Mezzanine Reset signal.
- Test the 1-wire interface using basic read and writes from and to the 1-Wire device respectively.
- Test the Motherboard-Mezzanine I2C interface. Perform reads and writes and confirm the desired functioning of the interface.
- Run the 40GbE high-speed interface, perform loopbacks' and monitor Mezzanine status.