HMC Register Addendum

MT43A4G40200, MT43A4G80200

Introduction

This document provides an overview of the configuration and status registers supported by the Hybrid Memory Cube (HMC) Gen2. Refer to the full HMC Gen2 data sheet for the complete specification.

Note: HMC engineering samples will support varying levels of functionality specified in this document. Contact Micron for more details about the functionality supported with each firmware revision.

Register Types

All registers are accessible through mode write and mode read requests or via sideband (JTAG/I^2C). Two of the distinct register types described throughout this document are direct registers, accessed directly through mode reads and writes, and indirect registers, which are accessed through the External Request Interface and are referred to as ERIs. There are two time periods for accessing these registers: during configuration and during runtime. Configuration registers correlate to Step 5 of the initialization routine as defined in the HMC data sheet, configuring the device prior to and during the INIT Continue ERI command. Runtime registers may be accessed following the clearing of the start bit after INIT Continue has completed execution. Register types include the four combinations of these two categories (direct/indirect and configuration/runtime), as well as two other types, device information status and debug. These combinations are detailed in Table 1.

Table 1: Register Types and Access Methods

Register Type	Accessible Time	Description
Device information status	Any (before or after initialization)	Used to determine device information and status.
Direct configuration	Initialization	Configuration registers used to set up the device prior to INIT Continue ERI command initiation.
Indirect configuration	Initialization	ERI commands used to set up the device prior to INIT Continue ERI command initiation.
Direct runtime	Runtime	Status and control registers that are valid following INIT Continue ERI command completion.
Indirect runtime	Runtime	Status and control ERI commands that are valid following INIT Continue ERI command completion.
Debug	Runtime	Registers or register fields that are only to be used for debug purposes and may have an impact on normal operation. These are valid following INIT Continue ERI command completion.

Sideband Direct Register Addressing Methods

HMC registers can be accessed in-band using the link interface with MODE WRITE and MODE READ commands or using sideband (I^2C or JTAG) accesses, which are explained in more detail here. The details of in-band addressing methods are contained in the Hybrid Memory Cube data sheet. With respect to sideband accesses, there are two methods that can be used to address each direct register in the HMC. The simplest method for addressing direct registers is to read or write the entire 32-bit register data field using the register addresses shown in the tables in this document. This method can potentially require a read-modify-write in order to properly set some data fields or it may require masking by the host or sideband processor when reading a register in order to isolate the desired register data fields. The start/size addressing method is a more advanced and precise method for accessing HMC status and control register fields. Using this method, a single register field can be read or written and all other fields can be masked.

Start/Size Addressing Method

This addressing method allows specific fields within a register to be accessed directly without having to read or write other fields in that register. Such a method is useful when modifying or reading a single field per access is desired.

The following is the format for the address to be used with the start/size addressing method through sideband accesses to configuration and status registers in the HMC.

Table 2: Start/Size Addressing Bit Fields

Field	Bits	Number of Bits	Description
Start	31:27	5	**Start field:** Encoded to provide a value from 0 to 31 that points to the starting bit position within the 32 bits of data, 0 being the LSB position and 31 being the most significant bit (MSB) position.
Size	26:22	5	**Size field:** Indicates the number of contiguous bits to read or write (from 1 to 32), and is encoded as follows: 0x0 = 32 bits, 0x1–0x1F = 1–31 bits.
Register address	21:0	22	**Register address field:** References a specific register as defined in this document.

Figure 1 illustrates an example of using the full register write method to set the link response open loop mode for link 0 to a value of 1. Figure 2 illustrates the same command using the start/size addressing method. The full register write method requires that the register be read, modified by masking values which are not being changed, followed by a write back to the link configuration register. The start/size addressing method only requires a single write to perform the same operation by automatically masking out values which are not being changed.

Figure 1: Full Register Write Method Example

```
openloop = 1 # Assign variable openloop value '1'
temp = (i2crd(0x20,0x00240000)) # Read 32 bit Link 0 Configuration Register
# Mask temp to assign openloop ('1') to only bit 2 of temp, and store in variable temp2
temp2 = ((temp&&0xFFFFFFFB||(openloop<<2))
# Write value stored in temp2 back to Link 0 Link Configuration Register
i2cwr(0x20,0x00240000,temp2))
```

Figure 2: Start/Size Register Write Method Example

```
openloop = 1 # Assign variable openloop value '1'
# Assign openloop ('1')as follows: start bit 2, size 1 address 0x240000
i2cwr(0x20,0x10640000,openloop)
```

Device Information Status Registers

Status registers in this section may be accessed with the I²C or JTAG buses at any point in time after tINIT. Access with in-band mode read requests must occur after the transaction layer has been initialized.

Table 3: Features

Register address: 0x2C0003

Name	Start Bit	Size	Description
Cube size	0	4	0x0: 2GB 0x1: 4GB 0x2-0xF: Reserved
Number of vaults	4	4	0x0: 16 vaults 0x1-0xF: Reserved
Number of banks per vault	8	4	0x0: 8 banks 0x1: 16 banks 0x2-0xF: Reserved
PHY	12	4	0x0: HMC-15G-SR 0x1-0xF: Reserved
Firmware feature set	16	16	Indicates revision of firmware programmed into the device. [23:16]: Indicates minor revision [27:24]: Indicates major revision [31:28]: Indicates patch revision

Table 4: Revisions and Vendor ID

Register address: 0x2C0004

Name	Start Bit	Size	Description
Vendor ID	0	8	Vendor ID Micron = 0x2C
Product revision	8	8	Product revision
Protocol revision	16	8	Protocol revision 0x01: HMCC Procotol revision 1.0 0x11: HMCC Protocol revision 1.1
PHY revision	24	8	PHY revision 0x01

Table 5: Cube Serial Number 1

Register address: 0x2C0001

Name	Start Bit	Size	Description
Serial number 1	0	32	Unique cube serial number (1 of 2)

Table 6: Cube Serial Number 2

Register address: 0x2C0002

Name	Start Bit	Size	Description
Serial number 2	0	32	Unique cube serial number (2 of 2)

Configuration Registers and ERIs

All of the register tables in this document include a column that specifies "type":
RW = Register can be read from and written to.
RO = Register can only be read from.
RWS = Register self clears after being written to.

Direct Configuration Registers

There are four types of direct configuration register fields:

1. **Init:** Must only be set during the configuration register load period of the initialization routine. Recommended values are included where appropriate.
2. **Debug:** Must match reset value for normal operation. Contact your Micron representative for information on how to use these registers for debug purposes.
3. **Runtime:** These register fields can be changed during the configuration register load period of the initialization routine or during normal operation (after transaction layer initialization).
4. **Reserved:** Must be set to 0.

Table 7: Global Configuration Registers

Register address: 0x280000

Name	Start Bit	Size	Type	Reset Value	Description	Register Type	Recommended/ Required Settings	Notes
Reserved	0	4	–	–	Reserved	Reserved	0x0	
Stop on fatal error	4	1	RW	0	When set to 1, a fatal error will cause the device to stop returning response packets back to the host (except for error response packets, when possible) and will stop transaction execution at the vault controller	Debug/Init	0	
Reserved	5	1	–	0	Reserved	Reserved	0	
Warm reset	6	1	RWS	0	Writing a 1 initiates a warm reset sequence; this bit auto clears	Runtime	0 unless warm reset required	1
Reserved	7	25	–	–	Reserved	Reserved	0x000000	

Note: 1. If a warm reset is required during normal operation, only the warm reset bit should be modified. Therefore it is recommended to use the start/size addressing method by writing 0x1 to address 0x30680000.

Table 8: Request Identification Register

Register address: Link 0 = 0x000000; Link 1 = 0x010000; Link 2 = 0x020000; Link 3 = 0x030000

Name	Start Bit	Size	Type	Reset Value	Description	Register Type	Recommended/ Required Settings
Source link ID (SLID)	0	3	RW	Actual cube link number	Sets the HMC link ID, which is used for internal routing of packets and will also be used in the SLID field in the response packet from the HMC, as shown in the specification. Legal values are 0, 1, 2, or 3 in current devices.	Debug	This field will be set automatically by the HMC upon boot and must not be modified.
Cube ID (CUB)	3	3	RW	Value of CUB pins	Cube number, which is used to match a cube with the CUB field in a request packet header that is directed to the appropriate cube.	Init	By default, this register field is set by the HMC with the value read from the CUB pins. It can be changed by the host in order to align with the desired cube identifier being sent by the host in the CUB field of the request packet header.
Reserved	6	26	–	–	Reserved	Reserved	0x0000000

Table 9: Link Configuration Register

Register address: Link 0 = 0x240000; Link 1 = 0x250000; Link 2 = 0x260000; Link 3 = 0x270000

Name	Start Bit	Size	Type	Reset Value	Description	Register Type	Recommended/ Required Settings	Notes
Link mode	0	2	RW	0x1	0x0: Link is not used 0x1: Link is a host link and a source link (typical use case) 0x2: RESERVED 0x3: Link is a pass-through link (used for chained configurations)	Init	System configuration dependent	
Link response open loop mode	2	1	RW	0	0x0: Response open loop mode is off 0x1: Response open loop mode is on	Init	Dependent upon how host consumes tokens	
Link packet sequence detection	3	1	RW	1	0x0: Packet sequence detection is off 0x1: Packet sequence detection is on	Debug	1	
Link CRC detection	4	1	RW	1	0x0: Link CRC error detection is off 0x1: Link CRC error detection is on	Debug	1	

Table 9: Link Configuration Register (Continued)

Register address: Link 0 = 0x240000; Link 1 = 0x250000; Link 2 = 0x260000; Link 3 = 0x270000

Name	Start Bit	Size	Type	Reset Value	Description	Register Type	Recommended/ Required Settings	Notes
Link duplicate length detection	5	1	RW	1	0x0: DLN detection is off 0x1: DLN detection is on	Debug	1	
Packet input enable	6	1	RW	1	0x0: Decode and parsing of incoming packets is disabled 0x1: Decode and parsing of incoming packets is enabled	Debug	1	
Packet output enable	7	1	RW	1	0x0: Transmission of outgoing packets is disabled 0x1: Transmission of outgoing packets is enabled	Debug	1	1
Inhibit link down mode	8	1	RW	0	When set to 1, the HSS PLLs will remain on regardless of the state of LxRXPS signals (applies only to links not reset in power-down mode)	Init	Host dependent, assess trade-off in low-power mode exit timing vs. power savings	
Link descramble enable	9	1	RW	1	0x0: Receiver descramblers are disabled 0x1: Receiver descramblers are enabled	Debug	1	
Link scramble enable	10	1	RW	1	0x0: Transmit scramblers are disabled 0x1: Transmit scramblers are enabled	Debug	1	
Error response packet	11	1	RW	1	When set to 1, the HMC will send error response packets on this link	Init	Host dependent; error responses may be sent on any combination of links	
Reserved	12	20	–	–	Reserved	Reserved	0x00000	

Note: 1. Unless set by the host, this field will reset to 0x0 upon cold reset and be set to 0x1 during execution of the init continue ERI.

Table 10: Link Run Length Limit Register

Register address: Link 0 = 0x240003; Link 1 = 0x250003; Link 2 = 0x260003; Link 3 = 0x270003

Name	Start Bit	Size	Type	Reset Value	Description	Register Type	Recommended/ Required Setting
Reserved	0	16	–	–	Reserved	Reserved	0x0000

Table 10: Link Run Length Limit Register (Continued)

Register address: Link 0 = 0x240003; Link 1 = 0x250003; Link 2 = 0x260003; Link 3 = 0x270003

Name	Start Bit	Size	Type	Reset Value	Description	Register Type	Recommended/ Required Setting
Transmit run length limit	16	8	RW	0x00	Sets the run length limit allowed on each lane (that is, the maximum number of zeros or ones that can be sent consecutively before a limiting circuit inserts a transition in the data stream to assure proper clock/data recovery at the far end receiver). A value of 50 (0x32) or more is required in this register to ensure proper run limiting operation. The default value is 0x00 (no limiting).	Init	Dependent on host Rx requirements; if host Rx is DC-coupled, set to 0x00
Reserved	24	8	–	–	Reserved	Reserved	0x00

Table 11: Link Retry Register

Register address: Link 0 = 0x0C0000; Link 1 = 0x0D0000; Link 2 = 0x0E0000; Link 3 = 0x0F0000

Name	Start Bit	Size	Type	Reset Value	Description	Register Type	Recommended/ Required Setting	Notes
Retry enable	0	1	RW	1	0x0: Retry is disabled 0x1: Retry is enabled	Debug	1	
Retry limit	1	3	RW	0x7	Controls the number of consecutive retry attempts for which there is no resulting progress (that is, local error abort never clears or received RRP does not advance despite unretired packets in the local retry buffer). Once this limit has been met, an error response packet is sent with link error in the ERRSTAT field to notify the host that the retry attempt limit has been met and FERR_N pin will assert. If retry limit = 0, there is no limit on the number of retries that can occur with no resulting progress.	Init	0x7	

Table 11: Link Retry Register (Continued)

Register address: Link 0 = 0x0C0000; Link 1 = 0x0D0000; Link 2 = 0x0E0000; Link 3 = 0x0F0000

Name	Start Bit	Size	Type	Reset Value	Description	Register Type	Recommended/ Required Setting	Notes
Retry time-out period	4	3	RW	0x5	0x0: 154ns 0x1: 205ns 0x2: 307ns 0x3: 410ns 0x4: 614ns 0x5: 820ns 0x6: 1229ns 0x7: 1637ns	Init	Dependent on host retry pointer return time	
Error abort mode	7	1	RO	0	Indicates that link has been in error abort mode. This bit is auto-cleared when the specified number of consecutive IRTRY packets have been received in order to clear error abort mode.	Debug	N/A	
Init retry packet transmit number	8	6	RW	0x06	0x2–0x3F: The number of IRTRY packets transmitted from link master during LinkRetry_Init is approximately four times the number specified in this field	Debug	0x06 (This will send 22–28 IRTRYs during LinkRetry_Init)	1
Reserved	14	2	–	–	Reserved	Reserved	0x0	
Init retry packet receive number	16	6	RW	0x10	The number of consecutive IRTRY packets that the link slave will detect before it clears the error abort mode.	Init	0x10 (16 IRTRY packets expected)	1
Reserved	22	2	–	–	Reserved	Reserved	0x0	
Link retry state	24	4	RO	0x1	Indicates status of the link retry state machine as follows: 0x1: Idle 0x2: Waiting for packet in progress to finish 0x4: Sending IRTRY 0x8: Sending retry buffer	Debug	N/A	
Reserved	28	4	–	–	Reserved	Reserved	0x0	

Note: 1. The number of IRTRYs transmitted and received by the host should be equivalent to those loaded into the Init Retry Packet Transmit Number and Init Retry Packet Receive Number fields, respectively. The host should transmit at least 22 IRTRYs during LinkRetry_Init and should expect 16 IRTRY packets before clearing error abort mode.

Table 12: Input Buffer Token Count Register

Register address: Link 0 = 0x040000; Link 1 = 0x050000; Link 2 = 0x060000; Link 3 = 0x070000

Name	Start Bit	Size	Type	Reset Value	Description	Register Type	Recommended/ Required Setting	Notes
Link input buffer max token count	0	8	RW	Recommended maximum token count for normal operation	Value represents the buffer space available, as measured in flits, in the link input buffer when it is empty	Init	System-dependent based on bandwidth and latency requirements	1
Reserved	8	24	–	–	Reserved	Reserved	0x000000	

Note: 1. The maximum token count allowed for normal operation is 219. The default value for this register will be the maximum value available for normal operation and can be checked by reading this value prior to writing it. The HMC data sheet Link Flow Control During Retry section contains discussion as to how the total sum of tokens are used for normal use as dictated by the protocol.

Table 13: Address Configuration Register

Register address: 0x2C0000

Name	Start Bit	Size	Type	Reset Value	Description	Register Type	Recommended/ Required Setting
Address mapping mode	0	4	RW	0x2	0x0: 32-byte block size (MAX). Low-interleave address mapping with the byte address set as the lowest five bits of the ADRS field in the request header, along with the default vault and bank mapping. 0x1: 64-byte block size (MAX). Low-interleave address mapping with the byte address set as the lowest six bits of the ADRS field in the request header, along with the default vault and bank mapping. 0x2: 128-byte block size (MAX). Low-interleave address mapping with the byte address set as the lowest seven bits of the ADRS field in the request header, along with the default vault and bank mapping. 0x3-0x7: Reserved. 0x8: User-defined 32-byte MAX block size. Byte address is defined as the lowest five bits of the ADRS field in the request header, along with user-defined vault and bank mapping. The user-defined vault and bank address start bits and size fields must be nonzero. 0x9: User-defined 64-byte MAX block size. Byte address is defined as the lowest six bits of the ADRS field in the request header, along with user-defined vault and bank mapping. The user-defined vault and bank address start bits and size fields must be nonzero. 0xA: User-defined 128-byte MAX block size. Byte address is defined as the lowest seven bits of the ADRS field in the request header, along with user-defined vault and bank mapping. The user-defined vault and bank address start bits and size fields must be nonzero. 0xB-0xF: Reserved.	Init	Host-dependent. Requests contained in completely random addresses do not benefit from any specific address mapping mode.

Table 13: Address Configuration Register (Continued)

Register address: 0x2C0000

Name	Start Bit	Size	Type	Reset Value	Description	Register Type	Recommended/ Required Setting
User-defined vault address	4	5	RW	0x00	Encoded field that specifies corresponding bit of ADRS to be LSB of vault address.	Init	Set to 0x00 if using low-interleave address mapping (0x0-0x2 in address mapping mode field). Must be nonzero if user-defined addressing mode is used.
User-defined bank address	9	5	RW	0x00	Encoded field that specifies corresponding bit of ADRS to be LSB of bank address.	Init	Set to 0x00 if user-defined addressing mode is NOT used. Must be nonzero if user-defined addressing is mode used.
Reserved	14	18	–	–	Reserved	Reserved	0

Table 14: Vault Control Register

Register address: 0x108000

Name	Start Bit	Size	Type	Reset Value	Description	Register Type	Recommended/ Required Setting	Notes
DRAM initialization mode	0	2	RW	0x0	0x0: DRAM is initialized to all 0s with correct ECC 0x1: Reserved 0x2: Initialize DRAM to user pattern 0x3: Reserved	Init	0x0, unless there is a need for a unique pattern.	2
Reserved	2	1	RO	0	Reserved	Reserved	0	2
Demand scrubbing	3	1	RW	1	Set to 0 to disable a scrub write to DRAM of corrected data when an SBE is detected on a transaction read request.	Init	0	

Table 14: Vault Control Register (Continued)

Register address: 0x108000

Name	Start Bit	Size	Type	Reset Value	Description	Register Type	Recommended/ Required Setting	Notes
Patrol scrubbing	4	1	RW	1	Set to 0 to disable a scrub write to DRAM of corrected data when an SBE is detected on a patrol read request.	Init	1: Writing the corrected data back into the memory array reduces the risk of the SBE turning into an uncorrectable MUE on subsequent accesses.	
Packet CRC detection	5	1	RW	1	Set to 0 to disable the CRC check performed on incoming packets to the vault controllers. This allows the vault controller to execute request packets that have CRC errors.	Debug	1	
Command/ Address retry count	6	3	RW	0x1	0x0: DRAM Command/Address retry disabled; 0x1: DRAM Command/ Address retry enabled	Debug	0x1	3
Data ECC correction disable	9	1	RW	0	Set to 1 to disable correction of an SBE if detected by the vault controller during read requests. Data from the DRAM will be returned unmodified in the response packet.	Debug	0	
MUE repair enable	10	1	RW	1	Enable to invoke a repair operation when an MUE is detected during either demand requests or patrol requests.	Init	1	4, 5
SBE dynamic repair enable	11	1	RW	1	Enable to invoke a dynamic repair operation when hard or frequent single bit errors are detected during either demand requests or patrol requests. Dynamic repair of hard SBE reduces the risk of the SBE turning into an uncorrectable MUE on subsequent accesses.	Init	1	4, 5
Enable SBE report	12	1	RW	0	Set to 0x1 (enable) to report any SBEs that occurred on a read request. These will be reported within the ERRSTAT field of the read response.	Init	0	4
Reserved	13	19	–	–	Reserved	Reserved	0x00000	

Notes: 1. Reserved bit values may be nonzero during runtime.

2. The DRAM Initialization Mode register field is set at initialization but will be used for DRAM initialization upon power up and cold reset as well as after DRAM BIST where applicable. See the DRAM BIST section for further details as to which modes will use this register field.
3. Only the values of 0x0 and 0x1 are supported.
4. Detection of MUE and SBE requires data ECC correction to be enabled. In order to detect MUE and SBE during patrol scrubbing, the patrol scrubbing feature must be enabled.
5. Detection of MUE and SBE are required in order for MUE and SBE repairs to take place.

Table 15: Disable NVM Write and Bootstrap Status

Register address: 0x280002

Name	Start Bit	Size	Type	Reset Value	Description	Register Type	Recommended/ Required Setting
Reserved	0	1	–	–	Reserved	Reserved	0
Cube ID	1	3	RO	N/A	These bits reflect the values of the CUB[2:0] pins captured when P_RST_N is de-asserted.	RO	N/A
Reference clock frequency	4	2	RO	N/A	These bits reflect the values of the REFCLK_BOOT[1:0] pins captured when P_RST_N is de-asserted. 00 = 125 MHz 01 = 156.25 MHz 10 = 166.67 MHz	RO	N/A
Reserved	6	2	–	–	Reserved	Reserved	0
Disable NVM write	8	1	RW	0x0	When bit is set to 1, all writing to NVM is disabled (includes logging and field repair).	Init	0x0 Host should set to 0x1 during device margin testing to avoid potentially using field repair resources due to voltages below specification.
Boot flag	9	23	RO	N/A	Contains boot information. HMC will populate with nonzero value.	Debug	N/A

External Request Interface (ERI) Commands

This type of access uses the external request data registers and the external request command register to access more complex commands and registers via the external request interface. The external data and request registers are accessible through mode write and mode read requests or sideband (JTAG/I^2C). The following section outlines how to run these commands by using the ERI register set.

Figure 3 illustrates the steps required to read or write ERI configuration registers.

Figure 3: ERI Command Access Flow

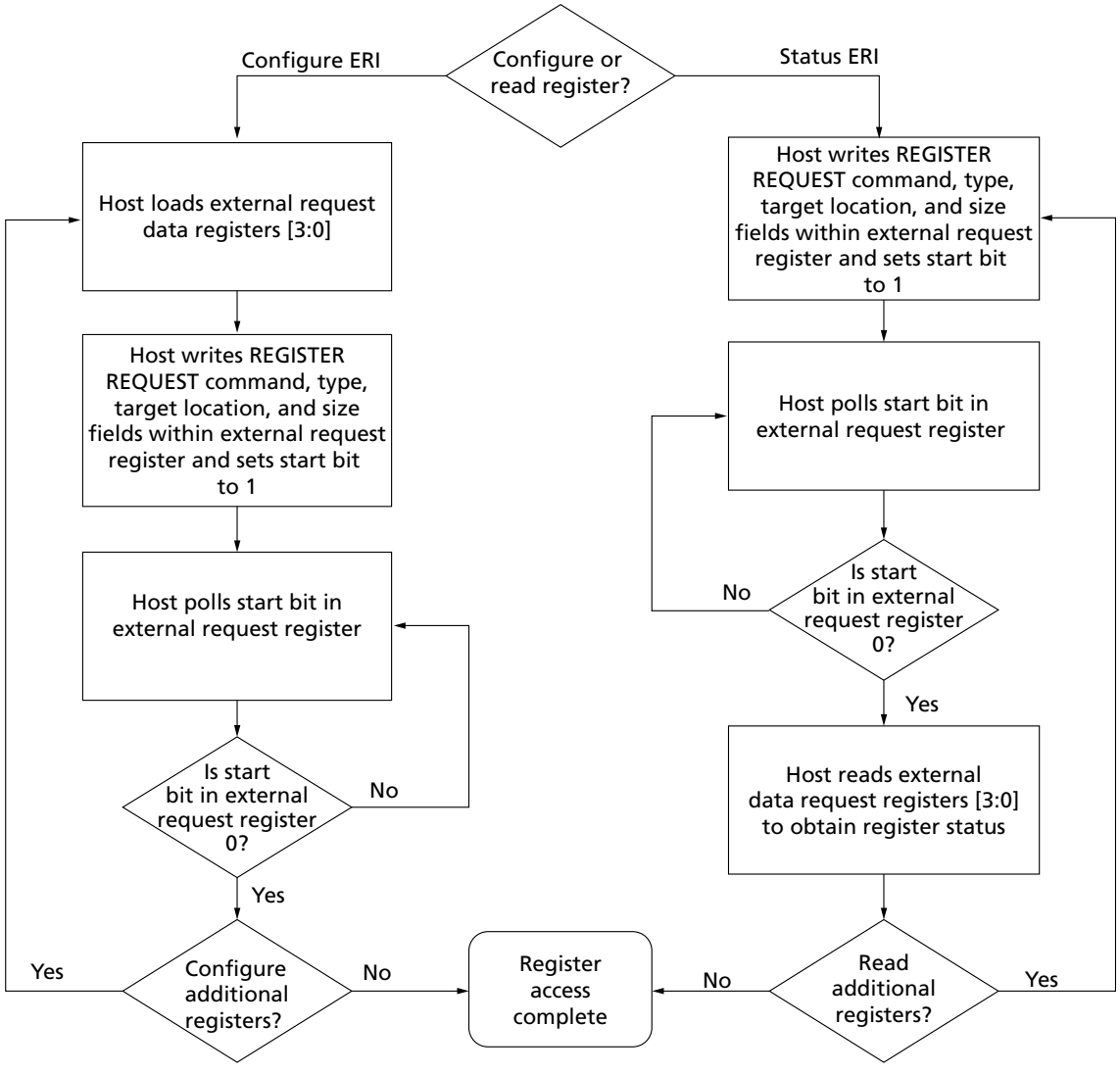


Table 16: External Request Data Register 0 (ERIDATA0)

Register address: 0x2B0000

Name	Start Bit	Size	Type	Reset Value	Description	Recommended Value
External data register 0	0	32	RW	N/A	Multipurpose register used to access configuration and status registers	ERI command dependent

Table 17: External Request Data Register 1 (ERIDATA1)

Register address: 0x2B0001

Name	Start Bit	Size	Type	Reset Value	Description	Recommended Value
External data register 1	0	32	RW	N/A	Multipurpose register used to access configuration and status registers	ERI command dependent

Table 18: External Request Data Register 2 (ERIDATA2)

Register address: 0x2B0002

Name	Start Bit	Size	Type	Reset Value	Description	Recommended Value
External data register 2	0	32	RW	N/A	Multipurpose register used to access configuration and status registers	ERI command dependent

Table 19: External Request Data Register 3 (ERIDATA3)

Register address: 0x2B0003

Name	Start Bit	Size	Type	Reset Value	Description	Recommended Value
External data register 3	0	32	RW	N/A	Multipurpose register used to access configuration and status registers	ERI command dependent

Table 20: External Request Register (ERIREQ)

Register address: 0x2B0004

Name	Start Bit	Size	Type	Reset Value	Description
Register request commands	0	8	RW	0x00	0x00: NO OPERATION 0x05: LINK CONFIGURATION 0x06: PHY CONFIGURATION 0x07: DRAM BIST WITH REPAIR 0x08: DRAM BIST WITHOUT REPAIR 0x09: MANUAL DRAM REPAIR 0x0A: TEMPERATURE MONITOR 0x0B: TEMPERATURE HISTORY 0x0C: REFRESH RATE ADJUSTMENT 0x0E: SIDEBAND DRAM ACCESS 0x0F: USER DRAM PATTERN DEFINITION 0x10: CHAINING TOPOLOGY CONFIGURATION 0x20: DRAM REPAIR HEALTH STATUS 0x21: NVM LOG READ START 0x22: NVM LOG READ NEXT 0x25: PRBS VERIFICATION 0x26: PATCH LOAD 0x27: PATCH EXECUTE 0xFF or 0x3F: INIT CONTINUE; command is executed by host after it has completed its register configuration, allowing internal HMC configuration to continue. All others: RESERVED
Type	8	8	RW	0x00	Reserved
Target location	16	6	RW	0x00	0x00–0x3E: Target location of command (including but not limited to links and vaults) 0x3F: Used to load global registers; also used to broadcast to all links
Size	22	4	RW	0x0	0x0: No data registers associated with request 0x1–0x4: Number of data registers associated with request 0x5–0x1F: Reserved
External request status	26	5	RO	0x00	0x00: Request was successful 0x01: Request caused an internal error 0x02: Request was invalid 0x03: Multi-cycle request complete The device sets this field when the last group of data registers for a status request is sent to the host; the field is also set after the last group of data registers expected from a configuration request 0x04–0x1F: ERI Specific

Table 20: External Request Register (ERIREQ) (Continued)

Register address: 0x2B0004

Name	Start Bit	Size	Type	Reset Value	Description
Start	31	1	RW	0	Host sets to 1 to inform the device there is a valid external request; HMC device sets to 0 after request is complete. Host polls bit and when it is 0, it can issue subsequent EXTERNAL REQUEST commands and read the external request status bits to determine the success of the pending EXTERNAL REQUEST command.

Early Configuration Time ERIs

Configuration ERI Sequences

The ERI registers in this section must only be issued during the configuration register load period of the initialization routine. Runtime reconfiguration is not supported. A cold reset must occur if configuration registers need to change after initialization. The only exception is the refresh rate adjustment ERI, which can be changed during initialization or runtime.

Table 21: Link Configuration ERI

Step	Command	Register Name	Register Address	Register Fields	Register Field Value	Notes
1	MODE WRITE REQUEST	ERIDATA0	0x2B0000	[1:0]: Link 0 speed	0x0: 10 Gb/s 0x1: 12.5 Gb/s 0x2: 15 Gb/s 0x3: Reserved	1, 2, 3, 4, 5
				[15:2]: Reserved	Must be 0x00	
				[17:16]: Link 0 link width	0x0: Full width Tx and Rx 0x1: Half-width Tx and Rx 0x2: Full-width Tx/half-width Rx 0x3: Half-width Tx/full-width Rx	
				[25:18]: Reserved	Must be 0x00	
				[26]: Link 0 Serial Loopback (TX-to-RX)	0: Disabled (required in normal operation) 1: Enabled	
				[29:27]: Link 0 PRBS patterns	0x0: PRBS7+ 0x1: PRBS7- 0x2: PRBS15+ 0x3: PRBS15- 0x4: PRBS23+ 0x5: PRBS23- 0x6: PRBS31+ 0x7: PRBS31-	
				[30]: Link 0 Tx pattern generation	0: Disabled (required in normal operation or when enabling parallel Rx-to-Tx loopback) 1: Enabled	
				[31]: Link 0 parallel loopback (Rx-to-Tx)	0: Disabled (required in normal operation) 1: Enabled	
2–4	MODE WRITE REQUEST	ERIDATA[3:1]	0x2B000[3:1]	Same as Step 1 for remaining links: Link 1 uses ERIDATA1 Link 2 uses ERIDATA2 Link 3 uses ERIDATA3	Same as Step 1 for remaining links	

Table 21: Link Configuration ERI (Continued)

Step	Command	Register Name	Register Address	Register Fields	Register Field Value	Notes
5	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: REGISTER REQUEST command	0x05: Link configuration	
				[30:8]: Reserved	0x000000: Reserved	
				[31]: Start	1: Inform HMC of valid request	
6	MODE READ REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x05: Link configuration	
				[25:8]: Reserved	0x00000: Reserved	
				[30:26]: External request status	Status will be valid after start bit is cleared: 0x0: Request was successful 0x02: Invalid request	
				[31]: Start	Start bit polling sequence If [31] = 1, pause for 10µs and issue subsequent MODE READ REQUEST to ERIREQ If [31] = 0, continue to next step	

Notes:
1. PRBS patterns are only valid when PRBS pattern generation is enabled.
2. Links are not trained when either TX pattern generation or parallel loopback (RX to TX) is enabled.
3. When using half-width link configurations, the lower half of the link is the half that is used.
4. Example PRBS algorithms are: PRBS7 = 1 + X^6 + X^7; PRBS15 = 1 + X^{14} + X^{15};PRBS23 = 1 + X^{18} + X^{23}; PRBS31 = 1 + X^{28} + X^{31}.
5. Link parallel loopback (RX to TX) functionality requires that Link Tx pattern generation be disabled.

Table 22: PHY Configuration ERI

Step	Command	Register Name	Register Address	Register Fields	Register Field Value	Notes
1	MODE WRITE REQUEST	ERIDATA0	0x2B0000	[4:0]: Link 0 Tx K2 coefficient	System dependent; Valid range: 0x0 to 0x15	1
				[15:5]: Reserved	Must be 0x000	
				[19:16]: Link 0 Tx K0 coefficient	System dependent; Valid range: 0x0 to 0x0D	1
				[29:20]: Reserved	Must be 0x000	
				30: AC-coupling capacitors used on board external to HMC Receivers	0: DC-coupled Rx; 1: AC-coupled Rx	
				31: Reserved	Must be 0	

Table 22: PHY Configuration ERI (Continued)

Step	Command	Register Name	Register Address	Register Fields	Register Field Value	Notes
2–4	MODE WRITE REQUEST	ERIDATA[3:1]	0x2B000[3:1]	Same as Step 1 for remaining links: Link 1 uses ERIDATA1 Link 2 uses ERIDATA2 Link 3 uses ERIDATA3	Same as Step 1 for remaining links	
5	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: REGISTER REQUEST command	0x06: PHY configuration	
				[30:8]: Reserved	0x000000: Reserved	
				[31]: Start	1: Inform HMC of valid request	
6	MODE READ REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x06: PHY configuration	
				[25:8]: Reserved	0x00000: Reserved	
				[30:26]: External request status	Status will be valid after start bit is cleared: 0x0: Request was successful 0x02: Invalid request	
				[31]: Start	Start bit polling sequence If [31] = 1, pause for 10µs and issue subsequent MODE READ REQUEST to ERIREQ If [31] = 0, continue to next step	

Note: 1. 0x0 is recommended unless simulation results indicate the need for a different value.

Table 23: Refresh Rate Adjustment ERI[1]

HMC automatically adjusts refresh rates and therefore the refresh rate adjustment ERI is for debug use only

Step	Command	Register Name	Register Address	Register Fields	Register Field Value
1	MODE WRITE REQUEST	ERIDATA0	0x2B0000	[0]: Refresh rate adjustment	0: Default refresh rates 1: Double the default refresh rates
2	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: REGISTER REQUEST command	0x0C: Refresh rate adjustment
				[30:8]: Reserved	0x000000: Reserved
				[31]: Start	1: Inform HMC of valid request

Table 23: Refresh Rate Adjustment ERI[1] (Continued)

HMC automatically adjusts refresh rates and therefore the refresh rate adjustment ERI is for debug use only

Step	Command	Register Name	Register Address	Register Fields	Register Field Value
3	MODE READ REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x0C: Refresh rate adjustment
				[25:8]: Reserved	0x00000: Reserved
				[30:26]: External request status	Status will be valid after start bit is cleared: 0x0: Request was successful 0x02: Invalid request
				[31]: Start	Start bit polling sequence If [31] = 1, pause for 10µs and issue subsequent MODE READ REQUEST to ERIREQ If [31] = 0, continue to next step

Note: 1. The refresh rate adjustment ERI may be issued during the configuration register load time or runtime.

Configuring Chained HMC Devices

In a chained system, each cube must be configured to route requests and responses through the cube network and to release tokens upstream in an ordered manner. The routing for each link in each device is configured by using the chaining configuration ERI. This section describes the Chaining Configuration ERI commands and register fields which are required to set up the routing tables.

Prior to executing the chaining configuration ERI, the link configuration register for every link of each cube must have already been properly programmed.

Table 24: Chaining Configuration ERI

Step	Command	Register Name	Register Address	Register Fields	Register Field Value	Notes
1	MODE WRITE REQUEST	ERIDATA0	0x2B0000	**Request Map Link 0** [15:0]: Link 0 accesses which cube(s)		1
				Request Map Link 1 [31:16]: Link 1 accesses which cube(s)		
2	MODE WRITE REQUEST	ERIDATA1	0x2B0001	**Request Map Link 2** [15:0]: Link 2 accesses which cube		1
				Request Map Link 3 [31:16]: Link 3 accesses which cube(s)		

Table 24: Chaining Configuration ERI (Continued)

Step	Command	Register Name	Register Address	Register Fields	Register Field Value	Notes
3	MODE WRITE REQUEST	ERIDATA2	0x2B0002	**Solicited Response Map** [15:0]: Which link will send solicited responses		1
				Unsolicited Response Map [31:16]: Which link will send unsolicited responses		1
4	MODE WRITE REQUEST	ERIDATA3	0x2B0003	**Source Link ID (SLID) Map** [15:0]: Which Link is attached to a SLID		1
				Token Dependency Map [31:16] Which link(s) are dependant upon another link(s) for token release		
5	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: REGISTER REQUEST command	0x10: Chaining topology config	
				[30:8]: Reserved	0x000000: Reserved	
				[31]: Start	1: Inform HMC of valid request	
6	MODE READ REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x10: Chaining topology config	
				[25:8]: Reserved	0x00000: Reserved	
				[30:26]: External request status	Status will be valid after start bit is cleared: 0x0: Request was successful 0x01: Internal error 0x02: Invalid request	
				[31]: Start	Start bit polling sequence If [31] = 1, pause for 10µs and issue subsequent MODE READ REQUEST to ERIREQ If [31] = 0, continue to next step	

Note: 1. Contact Micron for register configuration values.

Completing Initialization

When the INIT continue ERI is executed, the device will perform internal initialization tasks and initiate the training sequence on each of the active links. The start bit in the ERIREQ register will be 1 until the internal initialization is complete, at which time the device releases tokens during the transaction layer initialization. For normal operation, the INIT Continue ERI must be executed after writing all other INIT time registers and executing all configuration ERIs.

Link training must be executed during the time period specified as ^{t}INITCONTINUE, as outlined in the HMC Gen2 data sheet. The default timeout delay can be extended by setting the Timeout Delay field when executing the INIT Continue ERI as shown in the following table. Each bit set in the timeout delay field adds approximately 104µs for a total possible delay of approximately 55 seconds added to the ^{t}INITCONTINUE timeout period. When the internal INIT Continue process completes (link training is achieved or the maximum allowed timeout delay is reached), the start bit will be set to 0 to signify the completion of INIT Continue. If link training is not achieved within the specified time (including any added timeout delay), the INIT Continue read status will indicate a link initialization error.

Table 25: INIT Continue ERI

Step	Command	Register Name	Register Address	Register Fields	Register Field Value
1	MODE WRITE REQUEST	ERIDATA0	0x2B0000	[18:0]: Timeout delay	Timeout delay [18:0] multiplied by 104µs = actual timeout delay
				[31:19]: Reserved	0x0000: Reserved
2	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: REGISTER REQUEST command	0xFF or 0x3F: Init continue
				[30:8]: Reserved	0x000000: Reserved
				[31]: Start	1: Inform HMC of valid request

Table 25: INIT Continue ERI (Continued)

Step	Command	Register Name	Register Address	Register Fields	Register Field Value
3	MODE READ REQUEST	ERIREQ	0x2B0004	[7:0]: REGISTER REQUEST	0xFF or 0x3F (as written by host)
				[15:8]: Type	0x00
				[21:16]: Target location	0x00
				[25:22]: Size	0x00
				[30:26]: External request status	Status will be valid after start bit is cleared: 0x00: Request was successful 0x01: Request caused an internal error 0x02: Invalid request 0x11: Vault initialization error 0x12: Link initialization error 0x13: Vault initialization and link initialization error 0x14: Critical log warning 0x17: Critical log, vault, and link initialization error
				[31]: Start	Start bit polling sequence: If [31] = 1, pause 10µs and issue subsequent mode read request to ERIREQ If [31] = 0, continue to next step

Table 26: INIT Continue Error Status Handling

INIT Continue Status	Suggested Action
Request successful (status = 0x00)	Expected status, no errors and device is ready for normal use at this point.
Request caused an internal error (status = 0x01)	Indicates that an internal and possibly fatal error has occurred during INIT continue ERI execution. Device may be damaged or running at voltage conditions outside of specified range.
Invalid Request (status = 0x02)	Indicates that this ERI hasn't been implemented in this firmware revision. Newer device revisions accept 0xFF or 0x3F as valid INIT Continue commands, but early revisions only accepted 0x3F. Verify that the command aligns with the target FW revision.

Table 26: INIT Continue Error Status Handling (Continued)

INIT Continue Status	Suggested Action
Vault initialization error (status = 0x11)	A serious error has occurred while attempting to train the memory interface or initialize DRAM from the vault controller logic. NVM Write Disable will be automatically asserted by the firmware to prevent unintended dynamic or static repairs from being executed permanently. Verify that the voltages, temperatures and clocks are within specification. If so, running the BIST function can repair certain issues which may lead to this error, such as a TSV failure. To accomplish this, disable the patrol and demand scrubbing features, enable NVM Write, and run the DRAM BIST With Repair ERI to attempt to recover and permanently repair the issue. Note that the DRAM portion of BIST will not be executed and will indicate a failing status if INIT Continue has vault initialization error status. Make note of the TSV status output of BIST to determine if TSVs have been repaired through this process.
Link initialization error (status = 0x12)	The link training with the host did not complete during the time that INIT continue was being executed. Verify that the host is enabled and sending NULL flits prior to initiating the INIT continue ERI. Verify that the host is able to train the HMC link in the time required by INIT continue to complete. If unable to meet this requirement, utilize the appropriate timeout delay as shown in the INIT Continue ERI detailed description.
Vault initialization error and link initialization error (status = 0x13)	Combination of status values 0x11 and 0x12. See suggested actions for each of those two status return values.
Critical log warning (status = 0x14)	The non-volatile memory (NVM) log space is nearly or completely full. The device can function, but advanced functionality such as BIST repairs, static and dynamic repairs, and error logging will be limited or impossible. Read the NVM log in order to determine what has filled it by using the NVM Log Read ERIs and address the underlying issue that led to this condition.
Critical log warning, vault initialization error and link initialization error (status = 0x17)	Combination of critical log warning, vault initialization error and link initialization error status values. See suggested actions for each of those status return values.

I²C Configuration Register Load Example

The following example code is used to initialize the HMC with the I²C bus during the configuration register load period of the initialization routine. The I²C functions used in the example are represented by "i2cwr" and "i2crd" and represent properly formatted configuration register WRITE and READ commands, as outlined in the HMC data sheet. In this example, all four links are full width and operating at 15 Gb/s with the options noted in the comments in the script. Not all configuration registers are required to be written for normal operation.

```
#===== Global Configuration Direct Register ================================================
# No changes from default desired, register not written


#===== Request Identification Register ======================================================
# No changes from default desired, register not written.
# This will rely upon the CUB pins for the Cube ID for a positive match to the CUB field in
# packet headers from the host.


#===== Link Run Length Limit Register ======================================================
# Setting run length limit to 200 decimal (0xC8) to meet requirements of host receiver if
# AC Coupled.  Can leave as default (0x00000000 for infinite run lenght) if DC Coupled
i2cwr(0x10,0x00240003,0x00C80000) # Link 0 run length 0xC8 (200 dec)
i2cwr(0x10,0x00250003,0x00C80000) # Link 1 run length 0xC8 (200 dec)
i2cwr(0x10,0x00260003,0x00C80000) # Link 2 run length 0xC8 (200 dec)
i2cwr(0x10,0x00270003,0x00C80000) # Link 3 run length 0xC8 (200 dec)


#===== Link Retry Register =================================================================
# No changes from default desired.  Verify based upon host requirements.


#===== Link Configuration Direct Register ==================================================
#Setting link configuration as follows:
# bits 1:0 = 0x1 for host/source link
# bit 2 = '0' for response open loop mode off
# bit 3 = '1' for normal packet sequence detection (on)
# bit 4 = '1' to enable link CRC
# bit 5 = '1' to enable duplicate length detection
# bit 6 = '1' to decode/parse incoming packets (normal operation)
# bit 7 = '1' to enable transmission of packets
# bit 8 = '0' to allow links to enter down mode if RXPS set accordingly
# bit 9 = '1' to enable RX descramblers
# bit 10 = '1' to enable TX scramblers
# bit 11 = '1' to enable error response packets
i2cwr(0x10,0x00240000,0x00000EF9) # Link 0 Configuration
i2cwr(0x10,0x00250000,0x00000EF9) # Link 1 Configuration
i2cwr(0x10,0x00260000,0x00000EF9) # Link 2 Configuration
i2cwr(0x10,0x00270000,0x00000EF9) # Link 3 Configuration
```

```
#===== Input Buffer Token Count Register ============================================================
# Setting all links to have 219 (decimal) input buffer tokens
i2cwr(0x10,0x040000,0x000000DB) # Link0 Input Buffer Token Count = 219
i2cwr(0x10,0x050000,0x000000DB) # Link1 Input Buffer Token Count = 219
i2cwr(0x10,0x060000,0x000000DB) # Link2 Input Buffer Token Count = 219
i2cwr(0x10,0x070000,0x000000DB) # Link3 Input Buffer Token Count = 219


#===== Address Configuration Register ===============================================================
# No changes from default desired, so register not modified.


#===== Vault Control Register ========================================================================
# Sets all vaults as follows:
# bits 1:0 = 0x0 DRAM initalized to all 0's
# bit 2 = '1' to enable Hard SBE detect
# bit 3 = '1' to enable Demand scrubbing
# bit 4 = '1' to enable Patrol scrubbing
# bit 5 = '1' to enable CRC detection in packets
# bits 8:6 = 0x1 to enable CA Retry
# bit 9 = '0' to allow SBE correction
# bit 11 = '1' to enable Dynamic Repair
# bit 12 = '0' to disable SBE reporting
# All others Reserved (0x0)
i2cwr(0x10,0x00108000, 0x0000087C)


#===== Link Configuration ERI ========================================================================
#Set link confiuration ERI as follows (Same across all four links):
#Bits 1:0 = 0x2 for 15G
#Bits 17:16 = 0x0 for full width
#Bits 31:27 = 0x0 for normal operation (no loopback or PRBS generation/check)
# All others Reserved
i2cwr(0x10,0x002B0000, 0x00000002) #Link 0 ERIDATA0
i2cwr(0x10,0x002B0001, 0x00000002) #Link 1 ERIDATA1
i2cwr(0x10,0x002B0002, 0x00000002) #Link 2 ERIDATA2
i2cwr(0x10,0x002B0003, 0x00000002) #Link 3 ERIDATA3
#ERIREQ command for configuring all links based upon ERIDATA registers previously loaded
i2cwr(0x10,0x002B0004, 0x813F0005)
#Bits 7:0 = 0x05 ; Link Config Register Request Command
#Bits 15:8 = 0x00 ; Reserved
#Bits 21:16 = 0x3F ; Global Target
#Bits 25:22 = 0x4 ; Size = 4 for all ERIDATA registers
#Bits 30:26 = 0x00 ; Reserved
#Bit 31 = Start
# i2crd 0xF86B0004 simply reads bit 31 (start bit) of ERIREQ
# Alternatively, host can read 0x2B0004 and detect  bit 31 clear
while (i2crd(0x20,0xF86B0004)): wait(10usec)  # once start bit (bit 31) is cleared ('0') move to next commands/ERI
# Read ERI Request Status value (would be returned with 32b read of 0x2B0004
# 11010 (start bit = 26), 00101 (size = 5), address 10101100000000000000100 (2b0004)
i2crd(0x20,0xD16B0004)
```

```
#===== PHY Configuration ERI ========================================================================
#Set PHY confiuration ERI as follows (Same across all four links):
#Bits 4:0 = 0x0 K2 coefficient
#Bits 19:16 = 0x0 DC Coupled RX on board
# All others Reserved (0x0)
i2cwr(0x10,0x002B0000, 0x00000000) #Link 0 ERIDATA0
i2cwr(0x10,0x002B0001, 0x00000000) #Link 1 ERIDATA1
i2cwr(0x10,0x002B0002, 0x00000000) #Link 2 ERIDATA2
i2cwr(0x10,0x002B0003, 0x00000000) #Link 3 ERIDATA3
#ERIREQ command for configuring all links based upon ERIDATA registers previously loaded
i2cwr(0x10,0x002B0004, 0x80000006)
#Bits 7:0 = 0x06 ; PHY Config Register Request Command
#Bit 31 = Start
# i2crd 0xF86B0004 simply reads bit 31 (start bit) of ERIREQ
# Alternatively, host can read 0x2B0004 and detect  bit 31 clear
while (i2crd(0x20,0xF86B0004)): wait(10usec)  # once start bit (bit 31) is cleared ('0') move to next commands/ERI
# Read ERI Request Status value (would be returned with 32b read of 0x2B0004
# 11010 (start bit = 26), 00101 (size = 5), address 10101100000000000000100 (2b0004)
i2crd(0x20,0xD16B0004)



#===== INIT Continue ERI ============================================================================
# INIT Continue must be executed in order for the HMC to execute initialization and begin link training.
# Please see "Power on and Initialization section of HMC Datasheet for details.
i2cwr(0x10,0x002B0004, 0x800000FF) #INIT Continue ERIREQ
# Read from 0xF86B0004 simply reads bit 31 (start bit) of ERIREQ
# Alternatively, host can read 0x2B0004 and mask for bit 31 clear
while (i2crd(0x20,0xF86B0004)): wait(10usec) # wait for clear of start bit (bit 31)
# Read ERI Request Status value (would be returned with 32b read of 0x2B0004
# 11010 (start bit = 26), 00101 (size = 5), address 10101100000000000000100 (2b0004)
i2crd(0x20,0xD16B0004)
```

Runtime Registers and ERIs

Registers in this section may be accessed with the I²C or JTAG buses at any point during runtime. Runtime is defined as the period of time after initialization registers and ERIs have been executed, and the start bit in the INIT Continue ERI has been cleared (equals 0). Access with in-band mode register requests must occur after the transaction layer has been initialized.

Runtime Status Registers

Table 27: Global Status

Register address: 0x280001

Name	Start Bit	Size	Description
L0RXPS	0	1	Link 0 Rx power state level 1: Active state 0: Sleep or down
L1RXPS	1	1	Link 1 Rx power state level 1: Active state 0: Sleep or down
L2RXPS	2	1	Link 2 Rx power state level 1: Active state 0: Sleep or down
L3RXPS	3	1	Link 3 Rx power state level 1: Active state 0: Sleep or down
Reserved	4	2	Reserved
Self refresh	6	1	When 1, HMC is in self refresh state; occurs after all links exit active mode
Reserved	7	25	Reserved

Table 28: Link Training Synchronization Status

Register address: Link 0 = 0x240005; Link 1 = 0x250005; Link 2 = 0x260005; Link 3 = 0x270005

Name	Start Bit	Size	Description
Descrambler sync status	0	16	[0] = Lane 0,... [15] = Lane 15. Bit values of 1 indicate per lane recent descrambled Rx bits were zeros, required for descrambler sync. During link training, if the Link State (see Link Interface Status) does not progress past Descrambler Sync (0x04), bit values of 0 can identify lanes unable to achieve de-scrambler sync. After successful link training, all bits will have random values.

Table 28: Link Training Synchronization Status (Continued)

Register address: Link 0 = 0x240005; Link 1 = 0x250005; Link 2 = 0x260005; Link 3 = 0x270005

Name	Start Bit	Size	Description
TS1 sync status	16	16	[0] = Lane 0,... [15] = Lane 15. Bit values of 1 indicate per lane if TS1 is received while in link state TS1 Sync (0x10) or Lane Deskew (0x20). These values are frozen when exiting Lane Deskew (0x20), so these bytes should remain 0xFFFF when the link is trained.

Table 29: Lane Deskew Status

Register address: Link 0 = 0x240006; Link 1 = 0x250006; Link 2 = 0x260006; Link 3 = 0x270006

Name	Start Bit	Size	Description
Lane deskew status	0	32	Value of 0x0 indicates minimal deskew, value of 0x3 indicates maximal deskew. [0:1] = Lane 0,... [31:32] = Lane15.

Table 30: Link Token Status

Register address: Link 0 = 0x0C0001; Link 1 = 0x0D0001; Link 2 = 0x0E0001; Link 3 = 0x0F0001

Name	Start Bit	Size	Description
Response (transmit) token count	0	10	Indicates current number of tokens available for transmitting FLITs
RESERVED	10	6	Reserved
Last RRP	16	8	Indicates Last RRP value received on the link
Next FRP	24	8	Indicates FRP value that will be used next

Table 31: Link Interface Status[1]

Register address: Link 0 = 0x240002; Link 1 = 0x250002; Link 2 = 0x260002; Link 3 = 0x270002

Name	Start Bit	Size	Description
Link state	0	8	Link training state 0x01: Reset state 0x02: Rx CLK align 0x04: Descrambler sync 0x08: Nonzero wait 0x10: TS1 sync 0x20: Lane deskew 0x40: Zeroes wait 0x80: Link active

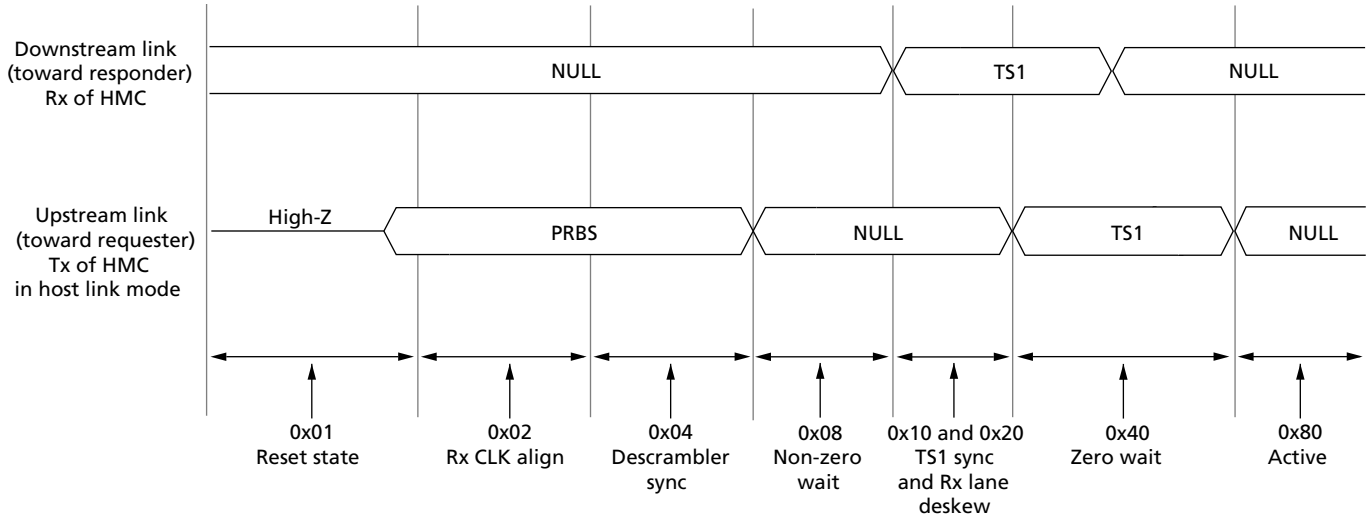
Table 31: Link Interface Status[1] (Continued)

Register address: Link 0 = 0x240002; Link 1 = 0x250002; Link 2 = 0x260002; Link 3 = 0x270002

Name	Start Bit	Size	Description
PLLB lock (required for 15G operation)	8	2	0x0: Neither of the PLLBs associated with the link is locked 0x1: PLLB associated with the half-link configuration is locked 0x3: PLLB PLLs associated with the full-link configuration are locked
PLLA lock (required for 10G and 12.5G operation)	10	2	0x0: Neither of the PLLAs associated with the link is locked 0x1: PLLA associated with half-link configuration is locked 0x3: PLLA PLLs associated with the full-link configuration are locked
Reserved	12	2	Reserved
Link down power state	14	1	0x1: Link is in down mode
Link sleep power state	15	1	0x1: Link is in sleep mode
Link active power state	16	1	0x1: Link is in active mode
Reserved	17	1	Reserved
Lane reversal	18	1	Status of auto-detected lane reversal 0x0: Lanes not reversed 0x1: Lanes reversed
Reserved	19	13	Reserved

Note: 1. Interface status registers are not valid until after INIT Continue.

Figure 4: Link Training State



Note: 1. The link training state begins at Step 6 of the power-on and initialization sequence.

Table 32: Lane Inversion Status

Register address: Link 0 = 0x240004; Link 1 = 0x250004; Link 2 = 0x260004; Link 3 = 0x270004

Name	Start Bit	Size	Description
Lane inversion	0	16	Status of auto-detected lane polarity inversion and correction found during descrambler synchronization; lane numbers map to decimal value 0x0: Lane polarity not inverted 0x1: Lane polarity inverted
Reserved	16	16	Reserved

Table 33: Temperature Monitor ERI Sequence

Step	Command	Register Name	Register Address	Register Fields	Register Field Value	Notes
1	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x0A: Temperature monitor	
				[30:8]: Reserved	0x000000: Reserved	
				[31]: Start	0x1: Inform HMC of valid request	
2	MODE READ REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x0A: Temperature monitor	
				[25:8]: Reserved	0x00000: Reserved	
				[30:26]: External request status	Status will be valid after start bit is cleared: 0x0: Request was successful 0x02: Invalid request	
				[31]: Start	Start bit polling sequence If [31] = 1, pause for 10µs and issue subsequent MODE READ REQUEST to ERIREQ If [31] = 0, continue to next step	
3	MODE READ REQUEST	ERIDATA0	0x2B0000	[15:0]: Logic die temperature recorded	[15:0]: Temperature in ˚C using two's compliment representation Examples: 0˚C: (0x0000) 95C: (0x005F) 125˚C (0x007D)	1, 2
				[31:16]: Reserved	0x000000: Reserved	
4	MODE READ REQUEST	ERIDATA1	0x2B0001	[15:0]: Top DRAM (closest to lid)	[15:0]: Temperature in ˚C using two's compliment representation Examples: 0˚C:0x0000) 95C: (0x005F) 125˚C (0x007D)	1, 2
				[31:16]: Reserved	0x000000: Reserved	
5	MODE READ REQUEST	ERIDATA2	0x2B0002	[15:0]: Bottom DRAM (closest to logic die)	[15:0]: Temperature in ˚C using two's compliment representation Examples: 0˚C: (0x0000) 95C: (0x005F) 125˚C: (0x007D)	1, 2
				[31:16]: Reserved	0x0000: Reserved	

Notes:
1. The reported temperature is accurate within ±5˚C.
2. HMC functionality is only guaranteed within the operational range that is specified in the data sheet.

The temperature history ERI is used to check historical high temperatures in the HMC. If the maximum operational threshold for temperature has been met or exceeded, the temperature will be logged in the NVM space permanently and reported when this ERI is executed. If the maximum operational threshold has never been exceeded, the values reported when this ERI is executed will correspond to the maximum temperature reached after the previous cold reset.

Table 34: Temperature History ERI Sequence

Step	Command	Register Name	Register Address	Register Fields	Register Field Value	Notes
1	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x0B: Temperature history	
				[30:8]: Reserved	0x000000: Reserved	
				[31]: Start	0x1: Inform HMC of valid request	
2	MODE READ REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x0B: Temperature history	
				[25:8]: Reserved	0x00000: Reserved	
				[30:26]: External request status	Status will be valid after start bit is cleared: 0x0: Request was successful 0x02: Invalid request	
				[31]: Start	Start bit polling sequence If [31] = 1, pause for 10µs and issue subsequent MODE READ REQUEST to ERIREQ If [31] = 0, continue to next step	
3	MODE READ REQUEST	ERIDATA0	0x2B0000	[15:0]: Max logic die temperature recorded	[7:0]: Temperature in ˚C Positive temperature: Equal to decimal equivalent of hex value Example: (0x005F = 95˚C)	1
				[31:16]: Reserved	0x0000: Reserved	
4	MODE READ REQUEST	ERIDATA1	0x2B0001	[15:0]: Max DRAM die temperature recorded	[7:0]: Temperature in ˚C Positive temperature: Equal to decimal equivalent of hex value Example: (0x005F = 95˚C)	1
				[31:16]: Reserved	0x0000: Reserved	

Note: 1. The reported temperature is accurate within ±5˚C.

Table 35: DRAM Repair Health Status ERI Sequence

Step	Command	Register Name	Register Address	Register Fields	Register Field Value
1	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x20: DRAM repair health status
				[30:8]: Reserved	0x000000: Reserved
				[31]: Start	0x1: Inform HMC of valid request
2	MODE READ REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x20: DRAM repair health status
				[25:8]: Reserved	0x00000: Reserved
				[30:26]: External request status	Status will be valid after start bit is cleared: 0x0: Request was successful 0x02: Invalid request 0x14: Critical log warning
				[31]: Start	Start bit polling sequence: If [31] = 1, pause for 10 µsec and issue subsequent MODE READ REQUEST to ERIREQ If [31] = 0, continue to next step
3	MODE READ REQUEST	ERIDATA0	0x2B0000	[15:0]: Command/address TSV repair health status	[0] = 0: Vault 0 repairs available [0] = 1: Vault 0 repair warning [1] = 0: Vault 1 repairs available [1] = 1: Vault 1 repair warning ⋮ [15] = 0: Vault 15 repairs available [15] = 1: Vault 15 repair warning
				[31:16]: Reserved	0x0000: Reserved
4	MODE READ REQUEST	ERIDATA1	0x2B0001	[15:0]: DQ TSV repair health status	[0] = 0: Vault 0 repairs available [0] = 1: Vault 0 repair warning [1] = 0: Vault 1 repairs available [1] = 1: Vault 1 repair warning ⋮ [15] = 0: Vault 15 repairs available [15] = 1: Vault 15 repair warning
				[31:16]: Reserved	0x0000: Reserved

Table 35: DRAM Repair Health Status ERI Sequence (Continued)

Step	Command	Register Name	Register Address	Register Fields	Register Field Value
5	MODE READ REQUEST	ERIDATA2	0x2B0002	[15:0]: DRAM array repair health status	[0] = 0: Vault 0 repairs available [0] = 1: Vault 0 repair warning [1] = 0: Vault 1 repairs available [1] = 1: Vault 1 repair warning ⋮ [15] = 0: Vault 15 repairs available [15] = 1: Vault 15 repair warning
				[31:16]: Reserved	0x0000: Reserved
6	MODE READ REQUEST	ERIDATA3	0x2B0003	[15:0]: Dynamic repair status	[0] = 0 : Vault 0 ok [0] = 1 : Vault 0 repair pending upon cold reset … [15] = 0 : Vault 15 ok [15] = 1 : Vault 15 repairs pending upon cold reset
				[31:16]: Reserved	0x0000: Reserved

DRAM Array Initialization

The DRAM array can be initialized with a custom 16B user data pattern that is repeated throughout the array and aligned on 0 and 16B boundaries. This is a two step process:

1. Early in the initialization, the host must communicate the desired pattern using the User DRAM Pattern Definition ERI.
2. The host must then set the DRAM Initialization Mode field of the vault control register with the user-defined pattern prior to an INIT CONTINUE command. After the INIT CONTINUE command, the DRAM array will be initialized by the vault controller with the custom pattern.

Table 36: User DRAM Pattern Definition ERI

Step	Command	Register Name	Register Address	Register Fields	Register Field Value
1	MODE WRITE REQUEST	ERIDATA0	0x2B0000	[31:0]	User pattern [31:0] (least significant bytes)
2	MODE WRITE REQUEST	ERIDATA1	0x2B0001	[31:0]	User pattern [63:32]
3	MODE WRITE REQUEST	ERIDATA2	0x2B0002	[31:0]	User pattern [95:64]
4	MODE WRITE REQUEST	ERIDATA3	0x2B0003	[31:0]	User pattern [127:96] (most significant bytes)

Table 36: User DRAM Pattern Definition ERI (Continued)

Step	Command	Register Name	Register Address	Register Fields	Register Field Value
5	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: REGISTER REQUEST command	0x0F: Set custom user pattern
				[30:8]: Reserved	0x000000: Reserved
				[31]: Start	0x1: Inform HMC of valid request
6	MODE READ REQUEST	ERIREQ	0x2B0004	[7:0]: REGISTER REQUEST command	0x0F: Set custom user pattern
				[25:8]: Reserved	0x00000: Reserved
				[30:26]: External request status	Status will be valid after start bit is cleared: 0x0: Request was successful 0x02: Invalid request
				[31]: Start	Start bit polling sequence: If [31] = 1, pause 10µs and issue subsequent mode read request to ERIREQ If [31] = 0, continue to next step

Sideband DRAM Access

The HMC has debug and test capabilities that allow reading and writing through sideband (JTAG or I^2C) directly to the DRAM array using the Sideband DRAM Access ERI. If writing with the Sideband DRAM Access ERI, the data written will be the pattern that has been defined by executing the User DRAM Pattern Definition ERI prior to each execution of the Sideband DRAM Access ERI. If reading from the DRAM array with the Sideband DRAM Access ERI, then the data read will be stored in the ERIDATA[3:0] registers upon clearing of the start bit following the Sideband DRAM Access ERI command execution. All in-band traffic should be quiesced to avoid any conflicts in the array that may result in unintended repairs.

Table 37: Sideband DRAM Access ERI (Read)

Step	Command	Register Name	Register Address	Register Fields	Register Field Value	Notes
1	MODE WRITE REQUEST	ERIDATA0	0x2B0000	[3:0]	Address: Byte[3:0] = 0x0	
				[23:4]	Address: DRAM[19:0]	
				[27:24]	Address: Bank[3:0]	1
				[31:28]	Address: Vault[3:0]	
2	MODE WRITE REQUEST	ERIDATA1	0x2B0001	[0]	0 = Read	
				[31:1]	Reserved	

Table 37: Sideband DRAM Access ERI (Read) (Continued)

Step	Command	Register Name	Register Address	Register Fields	Register Field Value	Notes
3	MODE WRITE REQUEST	ERIDATA2	0x2B0002	[31:0]	Reserved	
4	MODE WRITE REQUEST	ERIDATA3	0x2B0003	[31:0]	Reserved	
5	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: REGISTER REQUEST command	0x0E: Sideband DRAM Access	
				[30:8]: Reserved	0x000000: Reserved	
				[31]: Start	0x1: Inform HMC of valid request	
6	MODE READ REQUEST	ERIREQ	0x2B0004	[7:0]: REGISTER REQUEST command	0x0E: Sideband DRAM Access	
				[25:8]: Reserved	0x00000: Reserved	
				[30:26]: External request status	Status will be valid after start bit is cleared: 0x0: Request was successful 0x02: Invalid request	
				[31]: Start	Start bit polling sequence: If [31] = 1, pause 10µs and issue subsequent mode read request to ERIREQ If [31] = 0, continue to next step	
7	MODE READ REQUEST	ERIDATA0	0x2B0000	[31:0]	DRAM Data [31:0]	
8	MODE READ REQUEST	ERIDATA1	0x2B0001	[31:0]	DRAM Data [63:32]	
9	MODE READ REQUEST	ERIDATA2	0x2B0002	[31:0]	DRAM Data [95:64]	
10	MODE READ REQUEST	ERIDATA3	0x2B0003	[31:0]	DRAM Data [127:96]	

Note: 1. For 2GB (4-high) HMC devices, address bit Bank[3] will always be 0.

Table 38: Sideband DRAM Access ERI (Write)

Step	Command	Register Name	Register Address	Register Fields	Register Field Value	Notes
1	Execute the user DRAM Pattern Definition ERI to define data pattern to be written					
2	MODE WRITE REQUEST	ERIDATA0	0x2B0000	[3:0]	Address: Byte[3:0] = 0x0	
				[23:4]	Address: DRAM[19:0]	
				[27:24]	Address: Bank[3:0]	1
				[31:28]	Address: Vault[3:0]	

Table 38: Sideband DRAM Access ERI (Write) (Continued)

Step	Command	Register Name	Register Address	Register Fields	Register Field Value	Notes
3	MODE WRITE REQUEST	ERIDATA1	0x2B0001	[0]	1 = Write	
				[31:1]	Reserved	
4	MODE WRITE REQUEST	ERIDATA2	0x2B0002	[31:0]	Reserved	
5	MODE WRITE REQUEST	ERIDATA3	0x2B0003	[31:0]	Reserved	
6	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: REGISTER REQUEST command	0x0E: Sideband DRAM Access	
				[30:8]: Reserved	0x000000: Reserved	
				[31]: Start	0x1: Inform HMC of valid request	
7	MODE READ REQUEST	ERIREQ	0x2B0004	[7:0]: REGISTER REQUEST command	0x0E: Sideband DRAM Access	
				[25:8]: Reserved	0x00000: Reserved	
				[30:26]: External request status	Status will be valid after start bit is cleared: 0x0: Request was successful 0x02: Invalid request	
				[31]: Start	Start bit polling sequence: If [31] = 1, pause 10µs and issue subsequent mode read request to ERIREQ If [31] = 0, continue to next step	

Note: 1. For 2GB (4-high) HMC devices, address bit Bank[3] will always be 0.

NVM Log Read ERI

The HMC logs select events in internal non-volatile memory (NVM), which can be accessed by the host or sideband processor. The NVM log can be read at any time after INIT Continue completion by using the NVM Log Read ERI. The events logged include Dynamic Repair addresses, Static Repair addresses, and maximum temperatures for logic and DRAM. There are two ERI commands used to read out the entire log file; initially the Log Read Start command is issued and returns log data, then Log Read Next commands are issued until the log has been completely read. The log should be read completely and concatenated in order to ensure that all data associated with each entry has been read. Entries vary in length, but are made up of a multiple of 32 bits and the final entry will read ERIDATAx [31] (valid bit) set to 0. The following table details how to read and interpret the log file.

Table 39: NVM Log Read Start and NVM Log Read Next ERI Sequence

Step	Command	Register Name	Register Address	Register Fields	Register Field Value
1	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x21: NVM Log Read Start
				[30:8]: Reserved	0x000000: Reserved
				[31]: Start	0x1: Inform HMC of valid request
2	MODE READ REQUEST	ERIREQ	0x2B0004	[25:0]: Reserved	0x000000: Reserved
				[30:26]: External request status	Status will be valid after start bit is cleared: 0x01: Request caused an internal error 0x02: Request was invalid 0x03: Multi-cycle request complete
				[31]: Start	Start bit polling sequence: If [31] = 1, pause for 10 µsec and issue subsequent MODE READ REQUEST to ERIREQ If [31] = 0, continue to next step
3	MODE READ REQUEST	ERIDATA0	0x2B0000	[31:0]: Log Data	First NVM Log data entry
4	MODE READ REQUEST	ERIDATA1	0x2B0001	[31:0]: Log Data	Subsequent NVM Log data entry
5	MODE READ REQUEST	ERIDATA2	0x2B0002	[31:0]: Log Data	Subsequent NVM Log data entry
6	MODE READ REQUEST	ERIDATA3	0x2B0003	[31:0]: Log Data	Subsequent NVM Log data entry
7	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x22: NVM Log Read Next
				[30:8]: Reserved	0x000000: Reserved
				[31]: Start	0x1: Inform HMC of valid request

Table 39: NVM Log Read Start and NVM Log Read Next ERI Sequence (Continued)

Step	Command	Register Name	Register Address	Register Fields	Register Field Value
8	MODE READ REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x22: NVM Log read next
				[25:8]: Reserved	0x000000: Reserved
				[30:26]: External request status	Status will be valid after start bit is cleared: 0x01: Request caused an internal error 0x02: Invalid request 0x03: Multi-cycle request complete
				[31]: Start	Start bit polling sequence: If [31] = 1, pause for 10 µsec and issue subsequent MODE READ REQUEST to ERIREQ If [31] = 0, continue to next step
9	MODE READ REQUEST	ERIDATA0	0x2B0000	[31:0]: Log Data	Subsequent NVM Log data entry
10	MODE READ REQUEST	ERIDATA1	0x2B0001	[31:0]: Log Data	Subsequent NVM Log data entry
11	MODE READ REQUEST	ERIDATA2	0x2B0002	[31:0]: Log Data	Subsequent NVM Log data entry
12	MODE READ REQUEST	ERIDATA3	0x2B0003	[31:0]: Log Data	Subsequent NVM Log data entry
13	Repeat steps 7 through 12 until Valid bit (ERIDATAx [31]) = 0, indicating the last valid entry in the NVM log				

Table 40: Maximum Temperature Log Entries

Logs maximum logic die or DRAM die temperature recorded to date

Log Fields	Log Field Description
[7:0]: Info	[7:0]: Maximum Temperature in ˚C Positive temperature: Equal to decimal equivalent of hex value Example: (0x005F = 95˚C)
[15:8]: Reserved	0x00 Reserved
[18:16]: Entries Remaining	0x0
[23:19]: Reserved	0x0000: Reserved
[29:24]: Type	0x01: Maximum DRAM Temperature Log 0x02: Maximum Logic Temperature Log
[30]: Sequence	0: First entry since cold reset 1: Subsequent entry since cold reset
[31]: Valid	1: Entry is valid

Table 41: Static Repair Log Entry

Data about static repair event logged when it occurred

Entry in Sequence	Log Fields	Log Field Description
First	[15:0]: Reserved	0x0000: Reserved
	[17:16]: Entries Remaining	0x1
	[23:18]: Reserved	0x00: Reserved
	[29:24]: Type	0x04: Static Repair
	[30]: Sequence	0: First entry since cold reset 1: Subsequent entry since cold reset
	[31]: Valid	1: Entry is valid
Second	[0]: Reserved	0: Reserved
	[19:1]: DRAM Address	DRAM Address [19:1]
	[23:20]: Bank Address	Bank Address [3:0]
	[27:24]: Vault Address	Vault Address [3:0]
	[30:28]: Reserved	Reserved (may be non-zero)
	[31]: Valid	1: Entry is valid

Table 42: Dynamic Repair Log Entry

Data about dynamic repair event, logged when it occurred

Entry in Sequence	Log Fields	Log Field Description
First	[15:0]: Reserved	0x0000: Reserved
	[17:16]: Length	0x1
	[23:18]: Reserved	0x00: Reserved
	[29:24]: Type	0x03: Dynamic Error Repair
	[30]: Sequence	0: First entry since cold reset 1: Subsequent entry since cold reset
	[31]: Valid	1: Entry is valid
Second	[0]: Reserved	0: Reserved
	[19:1]: DRAM Address	DRAM Address [19:1]
	[23:20]: Bank Address	Bank Address [3:0]
	[27:24]: Vault Address	Vault Address [3:0]
	[30:28]: Reserved	Reserved (may be non-zero)
	[31]: Valid	1: Entry is valid

Table 43: BIST Repaired DRAM Row Log Entry

Data about repairs to the DRAM that were implemented by running the BIST ERI

Entry in Sequence	Log Fields	Log Field Description
First	[15:0]: Reserved	0x0000: Reserved
	[17:16]: Entries Remaining	0x1
	[23:18]: Reserved	0x00: Reserved
	[29:24]: Type	0x10: Row Repaired by BIST
	[30]: Sequence	0: First entry since cold reset 1: Subsequent entry since cold reset
	[31]: Valid	1: Entry is valid
Second	[6:0]: Reserved	0x00: Reserved
	[19:7]: DRAM Address	DRAM Address [19:7]
	[23:20]: Bank Address	Bank Address [3:0]
	[27:24]: Vault Address	Vault Address [3:0]
	[30:28]: Reserved	Reserved (may be non-zero)
	[31]: Valid	1: Entry is valid

Table 44: BIST Repaired DRAM Column Log Entry

Data about repairs to the DRAM implemented by running the BIST ERI

Entry in Sequence	Log Fields	Log Field Description
First	[15:0]: Reserved	0x0000: Reserved
	[17:16]: Entries Remaining	0x1
	[23:18]: Reserved	0x00: Reserved
	[29:24]: Type	0x11: Column repaired by BIST
	[30]: Sequence	0: First entry since cold reset 1: Subsequent entry since cold reset
	[31]: Valid	1: Entry is valid
Second	[19:0]: Reserved	Reserved (May be non-zero)
	[23:20]: Bank Address	Bank Address [3:0]
	[27:24]: Vault Address	Vault Address [3:0]
	[30:28]: Reserved	Reserved (may be non-zero)
	[31]: Valid	1: Entry is valid

Table 45: BIST Repaired TSV Entry

Data about repairs to the TSV (3D-interconnect) implemented by running the BIST ERI

Entry in Sequence	Log Fields	Log Field Description
First	[3:0]: Vault Address	Vault Address
	[15:4]: Reserved	0x0000: Reserved
	[17:16]: Entries Remaining	0x0
	[23:18]: Reserved	0x00: Reserved
	[29:24]: Type	0x13: BIST Repaired TSV
	[30]: Sequence	0: First entry since cold reset 1: Subsequent entry since cold reset
	[31]: Valid	1: Entry is valid

Reset and Power Down Considerations

It is important that the HMC not be powered down or cold reset while in the process of repairing or writing to non-volatile memory. In order to ensure that the HMC completes critical tasks prior to shutting down, the Shutdown ERI must be executed prior to powering down or cold resetting the device. After the command has successfully completed, no further operations will be supported and power may be removed or the device reset.

The HMC has a built in mechanism that allows a "soft" link power state control such that the LxRXPS pins can be overridden during runtime. If the Soft Link Power State ERI is executed and changes any link's current power state, all link power state control must use this ERI on all links until hardware control using the LxRXPS pins is regained by a cold reset. All requirements as outlined in the Power-On and Initialization section of the HMC Gen2 data sheet still apply, including the appropriate setting of LxRXPS pins and Link Configuration ERI. The Soft Link Power-Down ERI requires that all links be configured (all ERIDATA registers used) each time the ERI is executed.

Table 46: Shutdown ERI

Used to allow a safe power down or cold reset

Step	Command	Register Name	Register Address	Register Fields	Register Field Value
1	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: REGISTER REQUEST command	0x28: Shutdown
				[30:8]: Reserved	0x000000: Reserved
				[31]: Start	0x1: Inform HMC of valid request

Table 46: Shutdown ERI (Continued)

Used to allow a safe power down or cold reset

Step	Command	Register Name	Register Address	Register Fields	Register Field Value
2	MODE READ REQUEST	ERIREQ	0x2B0004	[7:0]: REGISTER REQUEST command	0x28: Shutdown
				[25:8]: Reserved	0x000000
				[30:26]: External request status	Status will be valid after start bit is cleared: 0x00: Request was successful 0x01: Request caused an internal error 0x02: Invalid request
				[31]: Start	Start bit polling sequence: If [31] = 1, pause 10µs and issue subsequent mode read request to ERIREQ If [31] = 0, proceed with reset or power down

Table 47: Soft Link Power State ERI

Used to allow the over-ride of LxRXPS power state after entering runtime

Step	Command	Register Name	Register Address	Register Fields	Register Field Value
1	MODE WRITE REQUEST	ERIDATA0	0x2B0000	[0]: Power	0: Override L0RXPS pin and force link state inactive (Sleep or Down) 1: Override L0RXPS pin and force link state Active
				[31:1]: Reserved	0x0000000
2	MODE WRITE REQUEST	ERIDATA1	0x2B0001	[0]: Power Down	0: Override L1RXPS pin and force link state inactive (Sleep or Down) 1: Override L1RXPS pin and force link state Active
				[31:1]: Reserved	0x0000000
3	MODE WRITE REQUEST	ERIDATA2	0x2B0002	[0]: Power Down	0: Override L2RXPS pin and force link state inactive (Sleep or Down) 1: Override L2RXPS pin and force link state Active
				[31:1]: Reserved	0x0000000
4	MODE WRITE REQUEST	ERIDATA3	0x2B0003	[0]: Power Down	0: Override L3RXPS pin and force link state inactive (Sleep or Down) 1: Override L3RXPS pin and force link state Active
				[31:1]: Reserved	0x0000000

Table 47: Soft Link Power State ERI (Continued)

Used to allow the over-ride of LxRXPS power state after entering runtime

Step	Command	Register Name	Register Address	Register Fields	Register Field Value
5	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: REGISTER REQUEST command	0x11: Power-down
				[30:8]: Reserved	0x000000: Reserved
				[31]: Start	0x1: Inform HMC of valid request
6	MODE READ REQUEST	ERIREQ	0x2B0004	[7:0]: REGISTER REQUEST command	0x11: Power-down
				[25:8]: Reserved	0x000000
				[30:26]: External request status	Status will be valid after start bit is cleared: 0x00: Request was successful 0x01: Request caused an internal error 0x02: Invalid request
				[31]: Start	Start bit polling sequence: If [31] = 1, pause 10µs and issue subsequent mode read request to ERIREQ If [31] = 0, proceed with reset or power down

Built-In Self Test and Repair

The built-in self test (BIST) consists of using built-in algorithms implemented in hardware and software within the device to test the integrity of the DRAM array. Testing is under autonomous control when the operation is initiated by the host. Micron determines the breadth of the test suite and the range of algorithms included within DRAM BIST.

Use of the DRAM BIST registers is optional but recommended, particularly following significant temperature fluctuation as experienced during manufacturing and attachment to a printed circuit board. The DRAM BIST registers are runtime registers and may only be loaded with the I^2C or JTAG sideband interface after the start bit of the INIT Continue ERI has been cleared (0). If a vault initialization error status is returned by the execution of the INIT Continue ERI, see INIT Continue Error Status Handling table for further details prior to running BIST.

When running the DRAM BIST WITH REPAIR command sequence, the "Disable NVM Write" bit must not be set or repairs will not take place.

The host is responsible for quiescing traffic on all links prior to running DRAM BIST. **Any traffic to the array during DRAM BIST will cause BIST failures and can cause permanent damage to the device.**

The state of HMC after DRAM BIST or repair depends upon the type of command run and the whether or not repairs will be made.

Table 48: DRAM BIST and Manual Repair Command Results

Command	Faults Found/Repairs to be Performed	HMC Logic and DRAM Status
DRAM BIST WITHOUT REPAIR	Faults may or may not be found/ Repairs will not be performed	Status bits will be returned at completion of ERI and start bit will be cleared when MODE READs are performed as shown in Table 49 (page 48). DRAM will be initialized based upon value set with User Pattern Definition ERI and DRAM Initialization Mode field in the vault control register.
DRAM BIST WITH REPAIR	No faults found/ No repairs required	Status bits will be returned at completion of ERI when MODE READs are performed as shown in Table 49 (page 48). DRAM will be initialized based upon value set with User Pattern Definition ERI and DRAM Initialization Mode field in the vault control register.
DRAM BIST WITH REPAIR or MANUAL REPAIR	Between 1 to 64 faults found/ Repairs will be performed	The required repairs will be performed, start bit will be cleared, and status will be returned when MODE READs are performed as shown in Table 49 (page 48). Up to 64 DRAM repairs and up to 2 TSV repairs will be performed. **A cold reset must be completed before any further operations are carried out.**
DRAM BIST WITH REPAIR	More than 64 faults found/ Repairs will not be performed	Status bits will be returned at completion of ERI when MODE READs are performed as shown in Table 49 (page 48). If more than 64 repairs are found to be required in one run of the DRAM BIST with repairs, the repairs will not be made. This condition should only be seen if the device has a serious issue that may or may not be related to the state of the DRAM array. In this case, repairs are not written in order to avoid using all repair space for an issue that is unrelated to a needed DRAM repair. A cold reset is not required because repairs were not performed.

Table 49: DRAM BIST with Repair ERI Sequence

Step	Command	Register Name	Register Address	Register Field	Register Field Value
1	MODE WRITE REQUEST	ERIDATA0	0x2B0000	[15:0]: Vault mask	Bit 0 = 0: Test Vault 0 Bit 0 = 1: Mask Vault 0 Bit 1 = 0: Test Vault 1 Bit 1 = 1: Mask vault 1 ... Bit 15 = 0: Test Vault 15 Bit 15 = 1: Mask vault 15
				[17:16]: Vaults in parallel[1]	0x0: Perform BIST on all vaults in parallel 0x1: Perform BIST on one vault at a time 0x2: Perform BIST on four vaults in parallel 0x3: Perform BIST on eight vaults in parallel
				[31:18]: Reserved	0x00000: Reserved

Table 49: DRAM BIST with Repair ERI Sequence (Continued)

Step	Command	Register Name	Register Address	Register Field	Register Field Value
2	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x07: DRAM BIST with repair
				[15:8]: Type	0x00: Reserved
				[21:16]: Target location	0x00: Ignored
				[25:22]: Size	0x00: Ignored
				[30:26]: External request status	0x00: Read only
				[31]: Start	1: Inform HMC of valid request
3	MODE READ REQUEST	ERIREQ	0x2B0004	[25:0]: Reserved	0x000000 Reserved
				[30:26]: ERI Status	0x00: ERI successful 0x01: ERI internal error (repair not successful) 0x02: Invalid command (repair not successful) 0x14: Critical log warning 0x15: Critical repair warning (repair not successful) 0x16: Repair warning
				[31]: Start	Start bit polling sequence: If [31] = 1: Pause for 10µs and issue subsequent mode read request to ERIREQ If [31] = 0: Continue to next step
4	MODE READ REQUEST	ERIDATA0	0x2B0000	[15:0]: Vault repair required	Bit 0 = 0: Vault 0 has no element failures (no repairs needed) Bit 0 = 1: Vault 0 has one or more elements requiring repairs Bit 1 = 0: Vault 1 has no element failures (no repairs needed) Bit 1 = 1: Vault 1 has one or more elements requiring repairs ... Bit 15 = 0: Vault 15 has no element failures (no repairs needed) Bit 15 = 1: Vault 15 has one or more elements requiring repairs
				[31:16]: Vault repair status	Bit 16 = 0: Vault 0 is repairable Bit 16 = 1: At least one element in Vault 0 is not repairable Bit 17 = 0: Vault 1 is repairable Bit 17 = 1: At least one element in Vault 1 is not repairable … Bit 31 = 0: Vault 15 is repairable Bit 31 = 1: At least one element in Vault 15 is not repairable

Table 49: DRAM BIST with Repair ERI Sequence (Continued)

Step	Command	Register Name	Register Address	Register Field	Register Field Value
5	MODE READ REQUEST	ERIDATA1	0x2B0001	[31:0]: Vault 0–7 DRAM fail counts	Bits 3:0 = Vault 0 DRAM error count Bits 7:4 = Vault 1 DRAM error count ... Bits 31:28 = Vault 7 DRAM error count
6	MODE READ REQUEST	ERIDATA2	0x2B0002	[31:0]: Vault 8-15 DRAM fail counts	Bits 3:0 = Vault 8 DRAM error count Bits 7:4 = Vault 9 DRAM error count ... Bits 31:28 = Vault 15 DRAM error count
7	MODE READ REQUEST	ERIDATA3	0x2B0003	[4:0]: Rerun request	Bit 0 = 1: Request to rerun DRAM BIST for more errors Bit 1 = 1: Temperature error, rerun at lower temp Bit 2 = 1: DRAM training error, rerun at different temp or voltage Bit 3: Greater than 64 repairs needed Bit 4 = 1: DRAM BIST locked out by prior repair process, power cycle required
				[15:5]: Reserved	Reserved
				[18:16] Types of repairs performed	Bit 16 = 1: TSV(s) Repaired Bit 17 = 1: Row(s) Repaired Bit 18 = 1: Column(s) Repaired
				[31:19]: Reserved	0x0000: Reserved

Note: 1. Ensure that the power delivery network and supplies are able to provide the required current for the number of parallel vaults being run in the BIST command.

Table 50: DRAM BIST Without Repair ERI Sequence

Step	Command	Register Name	Register Address	Register Field	Register Field Value
1	MODE WRITE REQUEST	ERIDATA0	0x2B0000	[15:0]: Vault mask	Bit 0 = 0: Test Vault 0 Bit 0 = 1: Mask Vault 0 Bit 1 = 0: Test Vault 1 Bit 1 = 1: Mask vault 1 ... Bit 15 = 0: Test Vault 15 Bit 15 = 1: Mask vault 15
				[17:16]: Vaults in parallel[1]	0x0: Perform BIST on all vaults in parallel 0x1: Perform BIST on one vault at a time 0x2: Perform BIST on four vaults in parallel 0x3: Perform BIST on eight vaults in parallel
				[31:18]: Reserved	0x00000: Reserved

Table 50: DRAM BIST Without Repair ERI Sequence (Continued)

Step	Command	Register Name	Register Address	Register Field	Register Field Value
2	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x08: DRAM BIST without repair
				[15:8]: Type	0x00: Reserved
				[21:16]: Target location	0x00: Ignored
				[25:22]: Size	0x00: Ignored
				[30:26]: External request status	0x00: Read only
				[31]: Start	1: Inform HMC of valid request
3	MODE READ REQUEST	ERIREQ	0x2B0004	[25:0]: Reserved	0x000000 Reserved
				[30:26]: ERI Status	0x00: ERI successful 0x01: ERI internal error 0x02: Invalid command 0x14: Critical log warning 0x15: Critical repair warning 0x16: Repair warning
				[31]: Start	Start bit polling sequence: If [31] = 1: pause for 10µs and issue subsequent mode read request to ERIREQ If [31] = 0: continue to next step
4	MODE READ REQUEST	ERIDATA0	0x2B0000	[15:0]: Vault repair required	Bit 0 = 0: Vault 0 has no element failures (no repairs needed) Bit 0 = 1: Vault 0 has one or more elements requiring repairs Bit 1 = 0: Vault 1 has no element failures (no repairs needed) Bit 1 = 1: Vault 1 has one or more elements requiring repairs ... Bit 15 = 0: Vault 15 has no element failures (no repairs needed): Bit 15 = 1: Vault 15 has one or more elements requiring repairs
				[31:16]: Vault repair status	Bit 16 = 0: Vault 0 is repairable Bit 16 = 1: At least one element in Vault 0 is not repairable Bit 17 = 0: Vault 1 is repairable Bit 17 = 1: At least one element in Vault 1 is not repairable … Bit 31 = 0: Vault 15 is repairable Bit 31 = 1: At least one element in Vault 15 is not repairable

Table 50: DRAM BIST Without Repair ERI Sequence (Continued)

Step	Command	Register Name	Register Address	Register Field	Register Field Value
5	MODE READ REQUEST	ERIDATA1	0x2B0001	[31:0]: Vault 0–7 DRAM fail counts	Bits 3:0 = Vault 0 DRAM error count Bits 7:4 = Vault 1 DRAM error count ... Bits 31:28 = Vault 7 DRAM error count
6	MODE READ REQUEST	ERIDATA2	0x2B0002	[31:0]: Vault 8–15 DRAM fail counts	Bits 3:0 = Vault 8 DRAM error count Bits 7:4 = Vault 9 DRAM error count ... Bits 31:28 = Vault 15 DRAM error count
7	MODE READ REQUEST	ERIDATA3	0x2B0003	[4:0]: Rerun request	Bit 0 = 1: Request to rerun DRAM BIST to correct additional errors Bit 1 = 1: Temperature error, rerun at lower temp Bit 2 = 1: DRAM training error, rerun at different temp or voltage Bit 3: Greater than 64 repairs needed Bit 4: DRAM BIST locked out by prior repair process, power cycle required
				[15:5]: Reserved	Reserved
				[18:16]: Types of repairs needed	Bit 16 = 1: TSV repair(s) needed Bit 17 = 1: Row repair(s) needed Bit 18 = 1: Column repair(s) needed
				[31:19]: Reserved	0x0000: Reserved

Note: 1. Ensure that the power delivery network and supplies are able to provide the required current for the number of parallel vaults being run in the BIST command.

Manual DRAM Repair ERI Sequence

If a DRAM array defect is at a known address, it is possible to manually repair the DRAM array by using the Manual DRAM Repair ERI. A manual repair may be desirable if testing outside of BIST has indicated a failure that has not been repaired by Dynamic Repair, Static Repair, or DRAM BIST. It is recommended that the NVM Log be read using the NVM Log read commands to verify that a repair was not already completed for this address prior to running the Manual DRAM Repair ERI sequence. When running the Manual DRAM Repair ERI sequence, the Disable NVM Write bit must be set to 0 and the DRAM Repair Health Status ERI must indicate that repairs are available, or repairs will not take place. After completion of the Manual DRAM Repair ERI sequence, a cold reset or power cycle is required before any other operations can be carried out. A block of addresses is repaired when the Manual DRAM Repair ERI is executed; therefore, before making multiple repairs, the array should be checked for errors remaining following the cold reset after each Manual DRAM Repair ERI is executed.

Table 51: Manual DRAM Repair ERI Sequence

Step	Command	Register Name	Register Address	Register Field	Register Field Value
1	MODE WRITE REQUEST	ERIDATA0	0x2B0000	[31:28]: Vault Address	Vault Address [3:0] for targeted repair
				[27:24]: Bank Address	Bank Address [3:0] for targeted repair
				[23:4]: DRAM Address	DRAM Address [19:0] for targeted repair
				[3:0]: Reserved	0x0: Reserved
2	MODE WRITE REQUEST	ERIDATA1	0x2B0001	[31:28]: Inverted Vault Address	Bitwise inversion of targeted Vault Address [3:0]
				[27:24]: Inverted Bank Address	Bitwise inversion of targeted Bank Address [3:0]
				[23:4]: Inverted DRAM Address	Bitwise inversion of targeted DRAM Address [19:0]
				[3:0]: Reserved	0xF: Bitwise inversion of ERIDATA0[3:0] from previous step
3	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x09: MANUAL REPAIR
				[15:8]: Type	0x00: Reserved
				[21:16]: Target location	0x00: Ignored
				[25:22]: Size	0x00: Ignored
				[30:26]: External request status	0x00: Read only
				[31]: Start	1: Inform HMC of valid request
4	MODE READ REQUEST	ERIREQ	0x2B0004	[25:0]: Reserved	0x000000 Reserved
				[30:26]: ERI Status	0x00: ERI successful 0x01: ERI internal error 0x02: Invalid command
				[31]: Start	Start bit polling sequence: If [31] = 1: pause for 10µs and issue subsequent mode read request to ERIREQ If [31] = 0: continue to next step
5	MODE READ REQUEST	ERIDATA0	0x2B0000	[15:0]: Reserved	Reserved
				[31:16]: Vault repair status	Bit 16 = 0: Address in vault 0 is repairable Bit 16 = 1: Address in vault 0 is not repairable ... Bit 31 = 0: Address in vault 15 is repairable Bit 31 = 1: Address in vault 15 is not repairable
6	MODE READ REQUEST	ERIDATA1	0x2B0001	Reserved	Reserved
7	MODE READ REQUEST	ERIDATA2	0x2B0002	Reserved	Reserved

Table 51: Manual DRAM Repair ERI Sequence (Continued)

Step	Command	Register Name	Register Address	Register Field	Register Field Value
8	MODE READ REQUEST	ERIDATA3	0x2B0003	[16:0]: Reserved	Reserved
				[17]	1: Address repaired
				[31:18]: Reserved	Reserved

SerDes Bring-up and Debug

HMC provides two features that can help with analyzing the performance of the SerDes or debugging a potential issue: eye metrics and PRBS verification. The registers associated with these features are all runtime registers and require that the Link Configuration ERI and INIT Continue ERI be run prior to reading or writing the registers or ERI in this section.

Eye Metrics

Each HMC SerDes has a built-in mechanism to measure the incoming data eye metrics: height (in voltage reference taps) and width (in unit delay taps). The values indicate the size of the inner eye at the bit error ratio (BER) of $1e^{-6}$. These metrics can be used to estimate the signal integrity at each HMC receiver lane. They can be read through eye metrics registers on a per-lane basis and are updated continuously by the HMC. Reading the eye metrics registers repeatedly and aggregating the results will provide a higher degree of accuracy.

The SerDes Rx eye width registers provide the width of the received data eye, as measured at the HMC receiver lane. The value read will be a five-bit hexidecimal value representing the eye width in number of delay taps and can be converted to UI by dividing by the value 32 (decimal). See Table 53 for per-lane addresses.

Table 52: SerDes Rx Eye Width

Name	Start Bit	Size	Type	Reset Value	Description	Notes
Reserved	0	10	RO	0x000	Reserved	1
Rx eye width	10	5	RO	0x00	The latest available eye width measurement	
Reserved	15	17	RO	0x00000	Reserved	1

Note: 1. Value may be nonzero during runtime.

Table 53: SerDes Rx Eye Width Addresses

Individual lane addresses to be read for SerDes Rx eye width

Lane	Link 0	Link 1	Link 2	Link 3
Lane 0	0x2000AA	0x2100AA	0x2200AA	0x2300AA
Lane 1	0x2000EA	0x2100EA	0x2200EA	0x2300EA
Lane 2	0x2001AA	0x2101AA	0x2201AA	0x2301AA
Lane 3	0x2001EA	0x2101EA	0x2201EA	0x2301EA
Lane 4	0x2002AA	0x2102AA	0x2202AA	0x2302AA

Table 53: SerDes Rx Eye Width Addresses (Continued)

Individual lane addresses to be read for SerDes Rx eye width

Lane	Link 0	Link 1	Link 2	Link 3
Lane 5	0x2002EA	0x2102EA	0x2202EA	0x2302EA
Lane 6	0x2003AA	0x2103AA	0x2203AA	0x2303AA
Lane 7	0x2003EA	0x2103EA	0x2203EA	0x2303EA
Lane 8	0x2008AA	0x2108AA	0x2208AA	0x2308AA
Lane 9	0x2008EA	0x2108EA	0x2208EA	0x2308EA
Lane 10	0x2009AA	0x2109AA	0x2209AA	0x2309AA
Lane 11	0x2009EA	0x2109EA	0x2209EA	0x2309EA
Lane 12	0x200AAA	0x210AAA	0x220AAA	0x230AAA
Lane 13	0x200AEA	0x210AEA	0x220AEA	0x230AEA
Lane 14	0x200BAA	0x210BAA	0x220BAA	0x230BAA
Lane 15	0x200BEA	0x210BEA	0x220BEA	0x230BEA

The SerDes Rx eye height registers provide the height of the received data eye, as measured at the HMC receiver lane. The value read will be a eight-bit hexadecimal value representing the eye height in voltage taps and can be converted to mV by multiplying by 7.8 (decimal). See Table Table 55 for per-lane addresses.

Table 54: SerDes Rx Eye Height

Name	Start Bit	Size	Type	Reset Value	Description	Notes
Rx eye height	0	8	RO	0x32	The latest available eye height measurement	
Reserved	8	24	RO	0x000000	Reserved	1

Note: 1. Value may be nonzero during runtime.

Table 55: SerDes Rx Eye Height Addresses

Individual lane addresses to be read for SerDes Rx eye height

Lane	Link 0	Link 1	Link 2	Link 3
Lane 0	0x200093	0x210093	0x220093	0x230093
Lane 1	0x2000D3	0x2100D3	0x2200D3	0x2300D3
Lane 2	0x200193	0x210193	0x220193	0x230193
Lane 3	0x2001D3	0x2101D3	0x2201D3	0x2301D3
Lane 4	0x200293	0x210293	0x220293	0x230293
Lane 5	0x2002D3	0x2102D3	0x2202D3	0x2302D3
Lane 6	0x200393	0x210393	0x220393	0x230393
Lane 7	0x2003D3	0x2103D3	0x2203D3	0x2303D3
Lane 8	0x200893	0x210893	0x220893	0x230893
Lane 9	0x2008D3	0x2108D3	0x2208D3	0x2308D3
Lane 10	0x200993	0x210993	0x220993	0x230993

Table 55: SerDes Rx Eye Height Addresses (Continued)

Individual lane addresses to be read for SerDes Rx eye height

Lane	Link 0	Link 1	Link 2	Link 3
Lane 11	0x2009D3	0x2109D3	0x2209D3	0x2309D3
Lane 12	0x200A93	0x210A93	0x220A93	0x230A93
Lane 13	0x200AD3	0x210AD3	0x220AD3	0x230AD3
Lane 14	0x200B93	0x210B93	0x220B93	0x230B93
Lane 15	0x200BD3	0x210BD3	0x220BD3	0x230BD3

PRBS Verification ERI

While the link configuration ERI is used to initiate a specific PRBS pattern to be generated and checked, additional steps must be taken to verify the synchronization of the PRBS checking circuitry and check the results. The PRBS Verification ERI Sequence is used to check whether each lane is synchronized and if there are errors beyond a bit error ratio (BER) of $1e^{-6}$. Steps 3 through 6 can be truncated to read only the desired link's status by reading only the associated ERIDATA register after step 2 if desired. Each time the PRBS Verification ERI sequence is executed, the status will be reset after the values are read. Therefore, the results from the first time the PRBS Verification ERI is run after link training may not be valid, and one or more subsequent runs is required.

Table 56: PRBS Verification ERI Sequence

Step	Command	Register Name	Register Address	Register Fields	Register Field Value	Notes
1	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x25: PRBS Verification	
				[15:8]: Type	0x00: Reserved	
				[21:16]: Target location	0x00: Ignored	
				[25:22]: Size	0x00: Ignored	
				[30:26]: External request status	0x0: Read only	
				[31]: Start	0x1: Inform HMC of valid request	
2	MODE READ REQUEST	ERIREQ	0x2B0004	Start bit polling sequence If [31] = 1, pause for 10µs and issue subsequent MODE READ REQUEST to ERIREQ If [31] = 0, continue to next step		
3	MODE READ REQUEST	ERIDATA0	0x2B0000	[31:0]: Link 0 Synchronization and Error Status	Bit 0: Lane 0 Synchronization Status Bit 1: Lane PRBS Errors ... Bit30: Lane 15 Synchronization Status Bit 1: Lane PRBS Errors	1

Table 56: PRBS Verification ERI Sequence (Continued)

Step	Command	Register Name	Register Address	Register Fields	Register Field Value	Notes
4	MODE READ REQUEST	ERIDATA1	0x2B0001	[31:0]: Link 1 Synchronization and Error Status	Bit 0: Lane 0 Synchronization Status Bit 1: Lane PRBS Errors ... Bit30: Lane 15 Synchronization Status Bit 1: Lane PRBS Errors	1
5	MODE READ REQUEST	ERIDATA2	0x2B0002	[31:0]: Link 2 Synchronization and Error Status	Bit 0: Lane 0 Synchronization Status Bit 1: Lane PRBS Errors ... Bit30: Lane 15 Synchronization Status Bit 1: Lane PRBS Errors	1
6	MODE READ REQUEST	ERIDATA3	0x2B0003	[31:0]: Link 3 Synchronization and Error Status	Bit 0: Lane 0 Synchronization Status Bit 1: Lane PRBS Errors ... Bit30: Lane 15 Synchronization Status Bit 1: Lane PRBS Errors	1

Note: 1. Error status is only valid when lane is synchronized.

Firmware Patching

There are many functions of the HMC which are controlled or impacted by a simple internal processor. The firmware which this processor executes is stored internal to the HMC in one-time programmable non-volatile memory (NVM) and therefore has limitations in terms of upgrade ability. There is, however, a procedure for writing patches to an unused portion of NVM which has been reserved for this purpose. Patches are version-specific and care must be taken to ensure that the firmware is not corrupted in any way. It is critical that voltages be within specification on all rails during this process. If voltages drop below specification during the Patch Apply ERI execution, permanent and irreversible damage to the device is likely.

The patch file, which must be obtained directly from Micron, will be in Intel HEX file format and the file must be parsed before sending the contents using the Patch Load ERI. The Patch Load and Patch Apply ERIs must be executed prior to reaching runtime (before initiating the INIT Continue ERI) and a cold reset is required following successful application.

A single example line showing the expected format is shown in Figure 5 (page 58) and the corresponding ERIDATA byte locations are shown in Figure 6 (page 58). The data size, address, end-of-file, and CRC fields are all present but must not be sent to the HMC through the ERI functions. Because the Intel HEX format is little endian, care must be taken in the realignment of the byte locations. A full file example is shown below.

Figure 5: Intel HEX Format Example

Shows one line of example file format to illustrate the pertinent data to be loaded into the HMC via the Patch Load ERI.

Digital size	Address	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	CRC
:10	0000	01	23	45	67	89	AB	CD	EF	DE	AD	BE	EF	A1	A2	A3	A4	A5

Figure 6: Patch ERIDATA Register Ordering Example

ERIDATA0 = 0x67452301
ERIDATA1 = 0xEFCDAB89
ERIDATA2 = 0xEFBEADDE
ERIDATA3 = 0xA4A3A2A1

Table 57: Patch Load and Patch Apply ERI Process

Step	Command	Register Name	Register Address	Register Field	Register Field Value
1	MODE WRITE REQUEST	ERIDATA0	0x2B0000	[7:0]	Hex Data D0
				[15:8]	Hex Data D1
				[23:16]	Hex Data D2
				[31:24]	Hex Data D3
2	MODE WRITE REQUEST	ERIDATA1	0x2B0001	[7:0]	Hex Data D4
				[15:8]	Hex Data D5
				[23:16]	Hex Data D6
				[31:24]	Hex Data D7
3	MODE WRITE REQUEST	ERIDATA2	0x2B0002	[7:0]	Hex Data D8
				[15:8]	Hex Data D9
				[23:16]	Hex Data D10
				[31:24]	Hex Data D11
4	MODE WRITE REQUEST	ERIDATA3	0x2B0003	[7:0]	Hex Data D12
				[15:8]	Hex Data D13
				[23:16]	Hex Data D14
				[31:24]	Hex Data D15
5	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x26: Patch Load
				[30:8]: Reserved	0x000000: Reserved
				[31]: Start	0x1: Inform HMC of valid request

Table 57: Patch Load and Patch Apply ERI Process (Continued)

Step	Command	Register Name	Register Address	Register Field	Register Field Value
6	MODE READ REQUEST	ERIREQ	0x2B0004	[25:0]: Reserved	0x000000: Reserved
				[30:26]: External request status	Status will be valid after start bit is cleared: 0x0: ERI was successful 0x01: Request caused an internal error 0x02: Request was invalid
				[31]: Start	Start bit polling sequence: If [31] = 1, pause for 10 µsec and issue subsequent MODE READ REQUEST to ERIREQ If [31] = 0, continue to next step
7	**Repeat Steps 1 though 6 until entire patch file is loaded. ":00000001FF" will indicate end of patch file.**				
8	MODE WRITE REQUEST	ERIREQ	0x2B0004	[7:0]: Register request command	0x27: Patch Apply
				[30:8]: Reserved	0x000000: Reserved
				[31]: Start	0x1: Inform HMC of valid request
9	MODE READ REQUEST	ERIREQ	0x2B0004	[25:0]: Reserved	0x000000: Reserved
				[30:26]: External request status	Status will be valid after start bit is cleared: 0x0: ERI was successful 0x01: Request caused an internal error 0x02: Request was invalid
				[31]: Start	Start bit polling sequence: If [31] = 1, pause for 10 µsec and issue subsequent MODE READ REQUEST to ERIREQ If [31] = 0, continue to next step
10	MODE READ REQUEST	ERIDATA0	0x2B0000	[15:0]: Status	0x00: Patch applied successfully 0x01: Patch applied successfully but not blown 0x02: Patch is empty 0x03: Checksum Error 0x04: Unrecognized patch file 0x05: Validation failed 0x06: Validation failed after some NVM blown 0x07: Table in NVM is full
				[31:16]: Error Pointer	If Status contains an error, Error Pointer will contain address where error occurred

Patch Load and Patch Apply ERI Example

```
:10000000 1600010000000140A076060000000000 7C
:10001000 00000040227406000000000000000040 C4
:10002000 23740600000000002274001000009010 ED
:10003000 A07601102147008490100000023740010 66
:10004000 15011520010000809F76060000000000 C9
:10005000 02000090001200709010009509A947D0 8E
:00000001FF
```

```
#ERI Loading patch 0: 0x00010016 0x40010000 0x000676a0 0x00000000
ERIDATA1 <= 0x00010016;
ERIDATA2 <= 0x40010000;
ERIDATA3 <= 0x000676A0;
ERIDATA4 <= 0x00000000;
ERIREQ <= 0x80000026;

#ERI Loading patch 1: 0x40000000 0x00067422 0x00000000 0x40000000
ERIDATA1 <= 0x40000000;
ERIDATA2 <= 0x00067422;
ERIDATA3 <= 0x00000000;
ERIDATA4 <= 0x40000000;
ERIREQ <= 0x80000026;

#ERI Loading patch 2: 0x00067423 0x00000000 0x10007422 0x10900000
ERIDATA1 <= 0x00067423;
ERIDATA2 <= 0x00000000;
ERIDATA3 <= 0x10007422;
ERIDATA4 <= 0x10900000;
ERIREQ <= 0x80000026;

#ERI Loading patch 3: 0x100176a0 0x84004721 0x00001090 0x10007423
ERIDATA1 <= 0x100176A0;
ERIDATA2 <= 0x84004721;
ERIDATA3 <= 0x00001090;
ERIDATA4 <= 0x10007423;
ERIREQ <= 0x80000026;

#ERI Loading patch 4: 0x20150115 0x80000001 0x0006769f 0x00000000
ERIDATA1 <= 0x20150115;
ERIDATA2 <= 0x80000001;
ERIDATA3 <= 0x0006769F;
ERIDATA4 <= 0x00000000;
ERIREQ <= 0x80000026;

#ERI Loading patch 5: 0x90000002 0x70001200 0x95001090 0xd047a909
ERIDATA1 <= 0x90000002;
ERIDATA2 <= 0x70001200;
ERIDATA3 <= 0x95001090;
ERIDATA4 <= 0xD047A909;
ERIREQ <= 0x80000026;

#ERI Apply patch
ERIREQ <= 0x80000027;
```

Revision History

Rev. E – 4/16

- Added note to Vault Control Register table reserved bits that values may be non-zero during runtime
- Removed "host" from "host parallel loopback" to avoid confusion
- Added 0x02 (invalid request) return value to all ERIs
- Simplified ERIREQ Mode Writes to show which bits are reserved and should simply be 0
- Added Chaining topology command to External Request Register (ERIREQ) Table
- Added Chaining Topology ERI definition table
- Updated reset value of retry limit to match the latest firmware (.9C) reset value
- Updated Register Types in the Introduction to more accurately describe ERIs
- Added Init to Register Type of the "stop on fatal error" field in the Global Configuration Registers table
- Updated description of the stop on fatal error field in Global Configuration Registers table to include that all fatal errors will cause the device to stop returning response packets
- Corrected error in Patch Load and Patch Apply ERI Process table, as a single step was mistakenly separated into two
- Clarified BIST vault fail counts are DRAM only (not TSV)
- Updated dynamic repair status of the DRAM Repair Health Status ERI Sequence table to clarify that the warning means there's a pending repair upon cold reset
- Added BIST log entries to decode of NVM Log Read ERI (added in .9B FW)
- Updated INIT Continue Error Status Handling table, added header, and improved suggested actions
- Added notes on BIST that supplies must be correctly sized to support parallelism options
- Changed recommended value for demand scrubbing field of the Vault Control Register table
- Updated "vault critical" to "vault initialization" to avoid confusion with the inband ERRSTAT of the same name
- Updated introduction to ERI section
- Cleaned up obsolete references to errata and devices prior to 0x10 product revision
- Removed "host mode" from link configuration register (now shown as reserved) to avoid confusion (not usable outside of Micron)

Rev. D – 5/15

- Reordered and categorized registers based on usage
- Added Sideband DRAM ERI description
- Added description for power down considerations and Shutdown ERI
- Changed "read only" value in link config ERI to properly reflect expected 0x0 value for external request status
- Added DRAM Manual Repair description and ERI
- Clarified BIST With Repair output status
- Updated all ERI commands into the ERI general section

- Added NVM Log Read section and ERIs
- Added Patching description and ERIs
- Added introduction for SerDes Bring-up and Debug section
- Fixed Vault Control MUE Repair Enable field from "RESERVED" to Init
- Added SerDes PRBS Verification ERI
- Removed SerDes PRBS metrics direct registers (replaced with ERI)
- Added note regarding which half of the link gets used for half-width configurations
- Updated Temperature History ERI to reflect maximum temperature logging vs. reporting
- Added Link Configuration bit 26 for Serial TX to RX Loopback
- Added ERI Status return for DRAM Repair Health Status in ERIREQ read
- Added Soft Link Power-Down ERI
- Updated Firmware Feature Set field to indicate major/minor/patched revisions
- Added note regarding quiescing in-band traffic when using sideband DRAM access
- Updated ERIREQ reads after command to reflect that the command is also read back

Rev. C – 11/14

- Updated the code used in the I^2C Configuration Register Load Example section
- Updated ERI Status values for INIT Continue and BIST ERIs
- Added vault parallelism options for BIST
- Added description of Start/Size addressing scheme
- Updated example code
- Updated ERI Status return value 0x03 description
- Corrected DRAM Repair Health Status ERI Command (showed 0x09, is 0x20)
- Added ERIDATA3 (Dynamic Repair Status) to Repair Health Status ERI
- Relocated and renamed Disable NVM/Bootstrap register to better indicate this is INIT time configuration field
- Added Lane Deskew Status, Link Token Status, and Link Training Sync Status fields
- Fixed gap in Link Retry Register (bits 22/23 are reserved but were missing)
- Clarified input buffer token count register to clearly state max token count 219
- Removed note regarding reset value for Init retry packet transmit number to match Revision 2.0 and newer devices

Rev. B – 07/14

- Updated Configuration ERI Sequences section
- Updated the DRAM BIST section
- Removed note regarding retry status field, which host will always see as 0x1
- Added Request Identification Register
- Updated note regarding initialization mode to point out it's used by BIST as well as at power up or cold reset
- Updated input buffer maximum value to note method for receiving max count
- Updated PLLA and PLLB lock status register values to correct values and to reflect full and half width possiblities.
- Modified Bootstrap Register field that was noted as "reserved" and assumed to be zero. Now reads "Boot Flag", which is expected to be non-zero.

- Changed Temperature History Mode Write command to reflect proper command code
- Provided description for Firmware Feature Set
- Noted that the following commands are "reserved" until implemented: 0x01: REGISTER WRITE 0x02: REGISTER WRITE NEXT 0x03: REGISTER READ 0x04: REGISTER READ NEXT
- Removed reference to DFE, as this is not modifiable
- Fixed table 14 which didn't count steps properly
- Added PRBS examples and xref note
- Removed unsupported temperatures as examples in Temperature ERI
- Added valid range for K0 and K2 coefficients
- Added Error Abort Mode indicator and Link Retry State fields to Link Retry State register
- Cleaned up note 1 and 3 in Link Retry Register to avoid contradiction
- Retry Timeout Period corrected from 0x3: 384ns to 0x3: 410ns
- Renamed “Retry Status” bit to “Retry Enable”
- Added SerDes Bringup and Debug section
- Removed note stating "Hardware reset value is 0x1; however, firmware overrides to 0x0 if value is not set by host." as this causes confusion because it cannot be checked or overridden during tINIT
- Changed name of "Data ECC correction" field to more accurately be described as "Data ECC correction disable"
- Changed Command/Address retry to debug feature, as it should not be disabled during normal operation
- Modified Command Parity Retry register field to properly reflect required debug usage
- Removed Global Control Register's Clear Error bit
- Removed note regarding reset value for Init retry packet transmit number to match Revision 2.0 and newer devices.
- Corrected DRAM Repair Health Status ERI command

Rev. A – 12/13

- Initial release

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