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Hardware User Manual

SKARAB ADC4X3G-14 Mezzanine

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ISSUE HISTORY

Description of Change	Issue No.	Edited by	Date
Initial Release	1	GT	12-December-2017
Removed host library code description since no longer required.	2	GT	21-August-2018

Contents

1. Introduction

1.1. Scope and Limitations

This document details how to use the SKARAB ADC4X3G-14 mezzanine. It provides details on the interfaces of the SKARAB ADC4X3G-14 mezzanine. An overview is provided of the hardware functionality of the SKARAB ADC4X3G-14 mezzanine.

1.2. Applicable Documents

1.3. Document Layout

Section 1 reflects the content of the document, and provides the reader with associated reference material.
Section 2 details the SKARAB ADC4X3G-14 mezzanine interfaces.

2. SKARAB ADC4X3G-14 Interfaces

2.1. Front Panel Interfaces

2.1.1. REF IN

Provides the 10MHz external reference input clock.

Connector type: SMA
Frequency: 10MHz
Input level: +8dBm
Input impedance: 50Ω

The SKARAB ADC4X3G-14 mezzanine is able to function without an external 10MHz reference input clock with the following limitations:

- The accuracy of the ADC sample clock will be determined by the accuracy of the on-board VCXO.
- It will not be possible to synchronise the HMC7044 PLL output clocks

2.1.2. ADC IN 0, 1, 2, 3

ADC analogue inputs.

Connector type: SMA
Full scale input level:

- Transformer only analogue input stage (default):
  - Approximately +9dBm at 942.5MHz single input tone
  - Approximately +12dBm at 1842MHz single input tone
- PGA analogue input stage configured for +15dB gain:
  - Approximately -6dBm at 942.5MHz single input tone
  - Approximately -1dBm at 1842MHz single input tone

Input impedance: 50Ω

2.1.3. LED 0, 1, 2

LED 0: flash for each GPS PPS pulse received
LED 1: flash while ARM microcontroller running
LED 2: solid on when PLL1 and PLL2 of HMC7044 PLL locked and reporting valid input 10MHz reference clock

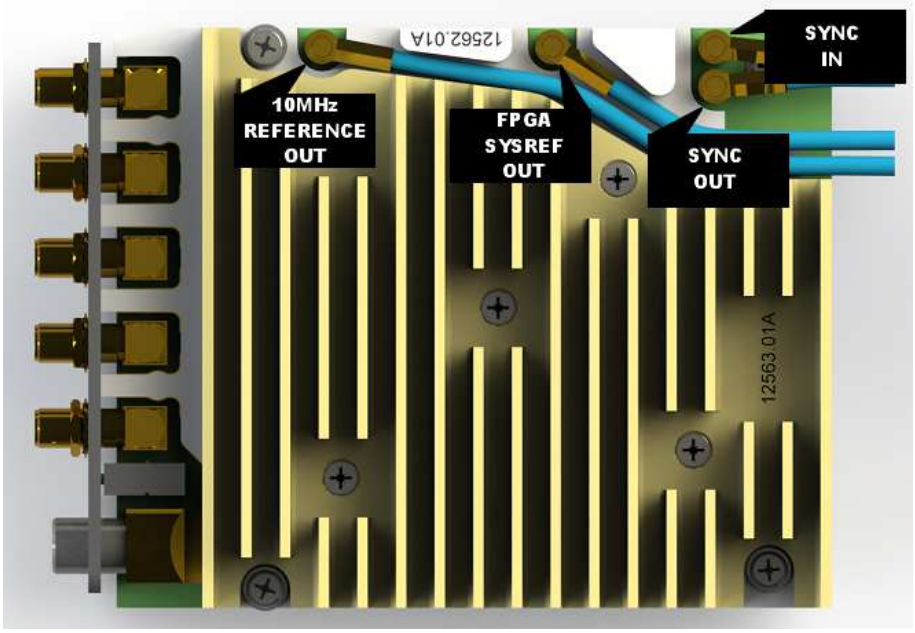
2.1.4. X0

Connector type: LEMO EPG.0B.309.HLN
Mating connector: LEMO FGG.0B.309.CLAD52 / FGG.0B.309.CYCD42

PIN NUMBER	DIRECTION	PIN DESCRIPTION
1	Output	Optional power to external GPS (different component build options): GND (default), +3V3 or +5V
2	Input	RS232 UART receive input from external GPS
3	Output	RS232 UART transmit output to external GPS GPS UART configuration: 9600 8N1
4	Input	External trigger input +5V / +3V3 LVCMOS input
5	GND	
6	Input	Optional external GPS PPS input (different component build options): No connect (default), +3V3 / +5V LVCMOS input with optional pull up or pull down resistor
7	GND	
8	Input	Optional external GPS PPS input or ARM microcontroller UART receive input (different component build options): RS232 level GPS PPS input (default) or RS232 UART receive input to ARM microcontroller
9	Output	RS232 UART transmit output from ARM microcontroller ARM UART configuration: 115200 8N1

2.2. Board Interfaces

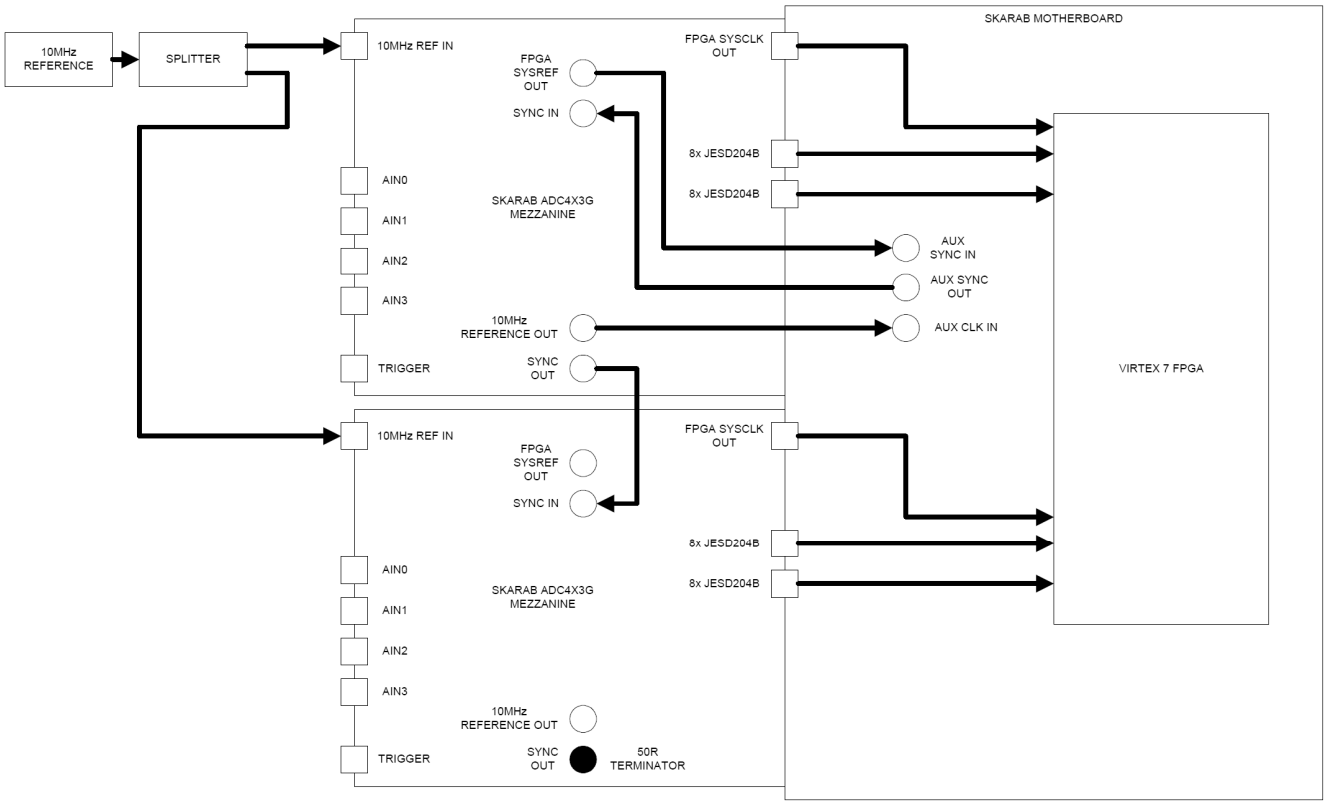
2.2.1. Board SMP Connections



Connector type: SMP

- 10MHz REFERENCE OUT: 10MHz reference clock to the SKARAB Motherboard. The FPGA firmware requires this clock to synchronise the HMC7044 PLL on the SKARAB ADC4X3G-14 mezzanine.
- FPGA SYSREF OUT: 2.9296875MHz SYSREF clock output from HMC7044 PLL to the SKARAB Motherboard. The FPGA firmware requires this clock to perform JESD204B synchronisation on the ADC32RF45 / ADC32RF80 ADCs on the SKARAB ADC4X3G-14 mezzanine.
- SYNC IN: SYNC signal input from the SKARAB Motherboard. There is a single SYNC signal used to synchronise either the PLL or the ADCs. Synchronising the PLL restarts the output clock dividers and delays to ensure they start up in phase. Synchronising the ADC restarts the JESD204B initial lane alignment sequence (ILA).
- SYNC OUT: SYNC output to next SKARAB ADC4X3G-14 mezzanine. Used to daisy chain the SYNC signal to multiple SKARAB ADC4X3G-14 mezzanines so that they sample synchronously. Terminated by a 50Ω SMP terminator on last board in the daisy chain.

The following diagram details how the above connections are made to the SKARAB Motherboard. It also demonstrates how the SYNC signal can be daisy chained to more than one SKARAB ADC4X3G-14 mezzanine.



The ADC sample clock frequency is 3GHz. The FPGA SYSREF clock frequency is 2.9296875MHz. The FPGA SYSCLK clock frequency is 187.5MHz.

The ADCs are JESD204B subclass 1 devices. This means that they use a SYSREF clock to synchronise local multiframe clocks across multiple devices (between the ADCs and the FPGA catching the JESD204B frames).

2.2.2. Mezzanine Connector

NAME	PIN NUMBER	DESCRIPTION
VCC	A40, B40, C40, D40, E40, F40, G40	Not connected
Vsen+	H40	Not connected
Vsen-	J40	Not connected
VCCm	K40	Not connected

GND	A39, B39, C39, D39, E39, F39, G39, H39, J39, K39, A36, B36, C36, D36, E36, F36, G36, H36, J36, K36, A35, D35, F35, G35, K35, A34, B34, C34, D34, E34, F34, G34, H34, J34, K34, A33, D33, G33, K33, A32, B32, C32, D32, E32, F32, G32, H32, J32, K32, A31, D31, G31, K31, A30, B30, C30, D30, E30, F30, G30, H30, J30, K30, A29, D29, G29, K29, A28, B28, C28, D28, E28, F28, G28, H28, J28, K28, A27, D27, G27, K27, A26, B26, C26, D26, E26, F26, G26, H26, J26, K26, A25, D25, G25, K25, A24, B24, C24, D24, E24, F24, G24, H24, J24, K24, A23, D23, G23, K23, A22, B22, C22, D22, E22, F22, G22, H22, J22, K22, A21, D21, G21, K21, A20, B20, C20, D20, E20, F20, G20, H20, J20, K20, A19, D19, G19, K19, A18, B18, C18, D18, E18, F18, G18, H18, J18, K18, A17, D17, G17, K17, A16, B16, C16, D16, E16, F16, G16, H16, J16, K16, A15, D15, G15, K15, A14, B14, C14, D14, E14, F14, G14, H14, J14, K14, A13, D13, G13, K13, A12, B12, C12, D12, E12, F12, G12, H12, J12, K12, A11, D11, G11, K11, A10, B10, C10, D10, E10, F10, G10, H10, J10, K10, A9, D9, G9, K9, A8, B8, C8, D8, E8, F8, G8, H8, J8, K8, A7, D7, G7, K7, A6, B6, C6, D6, E6, F6, G6, H6, J6, K6, A5, D5, G5, K5, A4, B4, C4, D4, E4, F4, G4, H4, J4, K4, F3, H3, K3, F2, H2, K2, F1, G1, H1, J1, K1	Ground
12V	A38, B38, C38, D38, E38, F38, G38, H38, J38, K38	+12V, primary power source for mezzanine module
5V	A37, B37, C37, D37, E37, F37, G37, H37, J37, K37	+5V
OPT	E35, F35, E33, F33, E31, F31, E29, F29, E27, F27, E25, F25, E23, F23, E21, F21, E19, F19, E17, F17, E15, F15, E13, F13, E11, F11, E9, F9, E7, F7, E5, F5	Not connected
RXP	H5	Not connected
RXN	J5	
TXP	B5	JESD204B ADC 0 Channel B Lane 3
TXN	C5	
RXP	H7	Not connected
RXN	J7	
TXP	B7	JESD204B ADC 0 Channel B Lane 2
TXN	C7	
RXP	H9	Not connected
RXN	J9	

TXP	B9	JESD204B ADC 0 Channel B Lane 1
TXN	C9	
RXP	H11	Not connected
RXN	J11	
TXP	B11	JESD204B ADC 0 Channel B Lane 0
TXN	C11	
RXP	H13	Not connected
RXN	J13	
TXP	B13	JESD204B ADC 0 Channel A Lane 0
TXN	C13	
RXP	H15	Not connected
RXN	J15	
TXP	B15	JESD204B ADC 0 Channel A Lane 1
TXN	C15	
RXP	H17	Not connected
RXN	J17	
TXP	B17	JESD204B ADC 0 Channel A Lane 2
TXN	C17	
RXP	H19	Not connected
RXN	J19	
TXP	B19	JESD204B ADC 0 Channel A Lane 3
TXN	C19	
RXP	H21	Not connected
RXN	J21	
TXP	B21	JESD204B ADC 1 Channel B Lane 3
TXN	C21	
RXP	H23	Not connected
RXN	J23	
TXP	B23	JESD204B ADC 1 Channel B Lane 2
TXN	C23	
RXP	H25	Not connected
RXN	J25	
TXP	B25	JESD204B ADC 1 Channel B Lane 1
TXN	C25	
RXP	H27	Not connected
RXN	J27	
TXP	B27	JESD204B ADC 1 Channel B Lane 0
TXN	C27	
RXP	H29	Not connected
RXN	J29	
TXP	B29	JESD204B ADC 1 Channel A Lane 0
TXN	C29	
RXP	H31	Not connected
RXN	J31	
TXP	B31	JESD204B ADC 1 Channel A Lane 1
TXN	C31	
RXP	H33	Not connected
RXN	J33	
TXP	B33	JESD204B ADC 1 Channel A Lane 2
TXN	C33	
RXP	H35	Not connected
RXN	J35	
TXP	B35	JESD204B ADC 1 Channel A Lane 3
TXN	C35	
Tm	A3	Temperature output – output voltage between 0 and +2V representing the temperature of the mezzanine module. LMT84DCKT device on SKARAB ADC4X3G-14 mezzanine.
AD2	B3	I2C address – pulled up on the mezzanine module, optionally

AD1	C3	pulled down to ground or floated on the SKARAB Motherboard. The I2C addresses for the four mezzanine sites are: Mezzanine site 0: "000" Mezzanine site 1: "001" Mezzanine site 2: "010" Mezzanine site 3: "011"
AD0	D3	
Hn	E3	Present detect – pulled high on the SKARAB Motherboard, the SKARAB ADC4X3G-14 mezzanine module grounds this pin. Used by the SKARAB Motherboard to determine whether a mezzanine module has been plugged in and to automatically bypass the mezzanine JTAG chain if a mezzanine site is open.
CK1oN	G3	FPGA SYSCLK clock output – output FPGA SYSCLK clock from the SKARAB ADC4X3G-14 mezzanine module for the JESD204B lanes.
CK1oP	G2	
CK1iN	J3	Reference clock input – optional clock input to HMC7044 PLL as a build option. Default is not connected.
CK1iP	J2	
SCL	A2	I2C serial interface – standard I2C serial interface to the ARM microcontroller on the SKARAB ADC4X3G-14 mezzanine. Tested at 400kHz. +3V3 voltage level. The SKARAB Motherboard is the I2C master.
SDA	A1	
TCK	B2	JTAG interface – JTAG interface to the ARM microcontroller on the SKARAB ADC. The JTAG voltage level is +3V3.
TDO	C2	
TMS	B1	
TDI	C1	
SD	D2	Interrupt – active low interrupt, pulled high on the SKARAB Motherboard. Pulled to ground by the SKARAB ADC4X3G-14 mezzanine module to signal a GPS PPS pulse.
RST_N	E2	Reset – active low reset, pulled high on the SKARAB ADC4X3G-14 mezzanine module. Pulled to ground by the SKARAB Motherboard to reset the ARM microcontroller on the mezzanine module.
1W	D1	1-wire interface – the SKARAB ADC4X3G-14 mezzanine module has a 1-wire EEPROM device. This stores the mezzanine module configuration and serial number. The 1-wire interface voltage level is +3V3.
Fn_E	E1	Fault not Enable – SKARAB Motherboard has a 4k7Ω pull up to +3V3. SKARAB Motherboard pulls this signal low to disable the mezzanine module, allows it to float high to enable the mezzanine module. The SKARAB ADC4X3G-14 mezzanine module drives this signal with the external trigger input. The external trigger voltage level is +3V3.