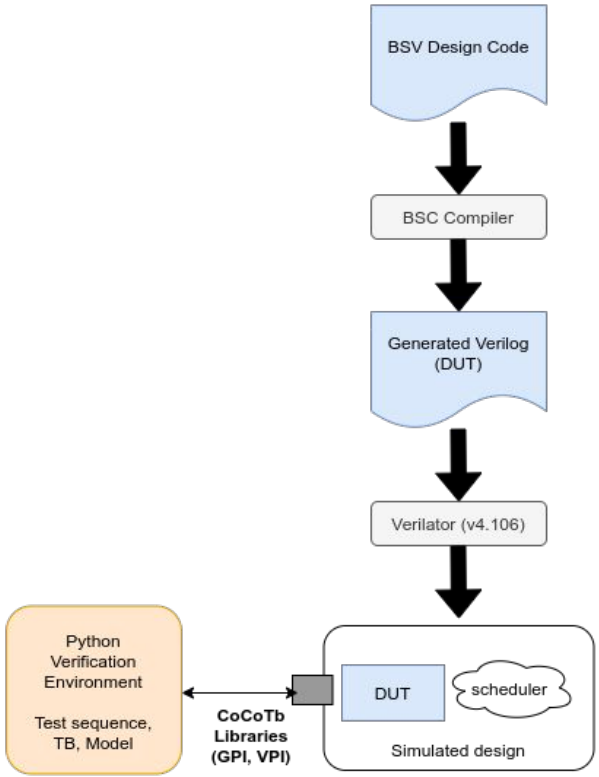
BSV Design Simulation

Tools Setup

Simulation Flow

- Verilog is generated from BSV Design Files (.bsv) using Bluespec Compiler (BSC)
- Verilator Simulates the design using the Verilog files
- CoCoTb is a Python package that interacts which the Verilated design to drive and observe design signals



Tools Required

- Python in Pyenv
- BSC
- Verilator
- CoCoTb
- cocotb_coverage

Reference Links

- BSC (https://github.com/B-Lang-org/bsc)
- Verilator (https://www.veripool.org/verilator/)
- CoCoTb (https://docs.cocotb.org/en/stable/)
- Steps for the demo today:
  - https://gitlab.com/lavanyajagan/tool_install/-/blob/main/README.md