Study of Adder and Subtractor Circuits

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In this experiment, we discuss binary addition and subtraction operations and its practical implementation using logic gates to build adder and subtractor circuits. We also discuss the implementation of the carry and borrow bits and the construction of N-bit adder/subtractor circuits.

I. OBJECTIVE

1. To construct half and full adder circuit and verify its working
2. To construct half and full subtractor circuit and verify its working
3. To construct a full adder-subtractor circuit and verify its working

II. THEORY

Binary Addition

Addition of binary numbers follow the same logical rules as that of decimal numbers. 1 bit addition rules are shown below. To accomodate the carry bit, we use two bits of output.

$$\begin{array}{rcrcrcr} & 0 & & 0 & & 1 & & 1 \\ + & 0 & + & 1 & + & 0 & + & 1 \\ \hline & 00 & & 01 & & 01 & & 11 \end{array}$$

Half Adder Circuit

The logic table for the 1 bit addition can be formed as follows, (where C represents the carry bit)

A	B	Q	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

TABLE I: 1-bit Adder with Carry-Out

One can observe that we can implement sum Q using an `XOR` gate and carry bit C using an `AND` gate.

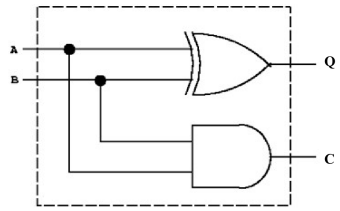

FIG. 1: Schematic for the half adder circuit

Full Adder Circuit

To add two or more bits together we need to account for the carry-in bit from the previous operation. A full adder circuit accepts a carry in bit C_{N-1} along with inputs A and B. The truth table will be formed as follows.

C_{N-1}	A	B	Q	C_N
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

TABLE II: One-bit Full Adder with Carry-In & Carry-Out

We can observe that we can implement sum Q using an `XOR` of the 3 inputs (an odd number of 1s results in a 1). Hence the full adder can be constructed from two half adders and an `OR` gate.

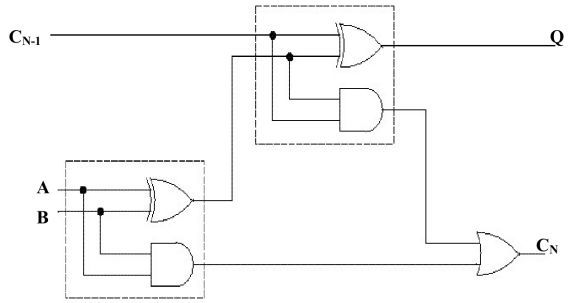

FIG. 2: Schematic for the full adder circuit

Now, to construct a 2-bit adder, we can combine a full adder with a half adder. Any arbitrary N-bit adder can thus be constructed by a cascading series of full adders, also called a *ripple carry adder* (since the carry bit ripples from one stage to the next).

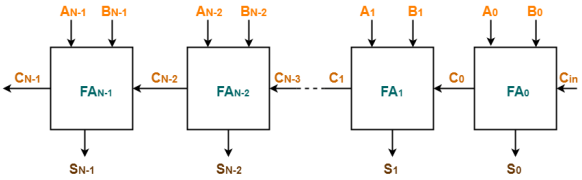

FIG. 3: Schematic for an N-bit ripple carry adder

However in a real circuit, gates take time to switch states, so 32-bit or 64-bit ripple carry adders might take a significant amount of time (∼100 ns) to settle into their final sum. For this other adder circuits are used, like the *carry look-ahead adder* which solves the delay by calculating the carry signals in advance.

Binary Subtraction

Subtraction of binary numbers can be performed in a similar fashion. 1 bit subtraction rules are shown below. Here, to accomodate the borrow, we use two bits of output.

$$\begin{array}{rrrrrrrr} & 0 & & 0 & & 1 & & 1 \\ - & 0 & - & 1 & - & 0 & - & 1 \\ \hline & 00 & & 11 & & 01 & & 00 \end{array}$$

Half Subtractor Circuit

The logic table for the 1 bit subtraction is shown below (where B_N represents the borrow bit)

A	B	Q	B_N
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

TABLE III: 1-bit subtractor with borrow

One can observe that we can implement sum Q using an `XOR` gate and borrow bit B_N using an `AND` gate with input A inverted.

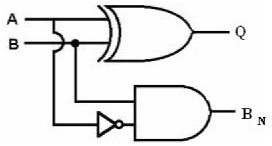

FIG. 4: Schematic for the half subtractor circuit

Full Subtractor Circuit

A full subtractor circuit accepts a minuend (A) and the subtrahend (B) and a borrow (B_{N-1}) as inputs from a previous circuit.

B_{N-1}	A	B	Q	B_N
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

TABLE IV: 1-bit Full Subtractor with B_{N-1} & B_N

A full subtractor circuit can be constructed by combining two half subtractor circuits and an `OR` gate.

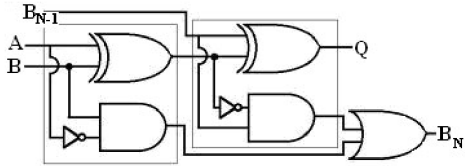

FIG. 5: Schematic for the full subtractor circuit

Full Adder Subtractor Circuit

To use the same circuit to perform both addition and subtraction, one can replace the `NOT` gate of the subtractor circuit by an `XOR` gate. Here, the second input for the `XOR` gate decides the function of the circuit, either addition or subtraction. If the second input for `XOR` is 0, the circuit will do addition and if 1, it will do subtraction. Hence they act as a *control bits* (X_1 and X_2).

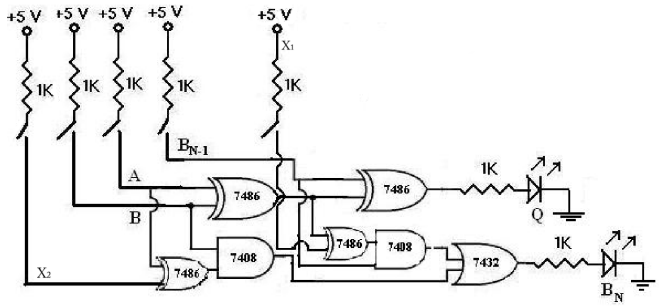

FIG. 6: Full Adder-Subtractor Circuit Diagram

N-bit subtractor circuits can also be built using ripple borrow subtractor technique, similar to the one described before.

III. EXPERIMENTAL SETUP

Apparatus

1. Digital ICs (XOR-7486, AND-7408, OR-7432, NOT-7404)
2. Resistors (1 kΩ)
3. D.C. Power supply (5V)
4. LEDs
5. Connecting Wires
6. Multimeters

Circuit Diagrams

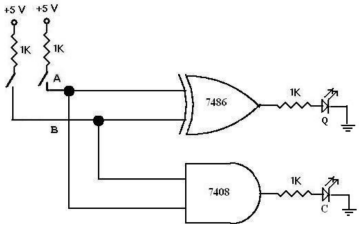

FIG. 7: Half Adder Circuit Diagram

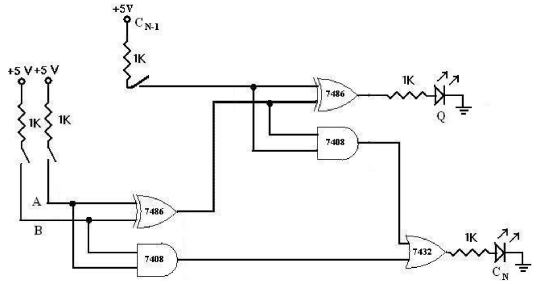

FIG. 8: Full Adder Circuit Diagram

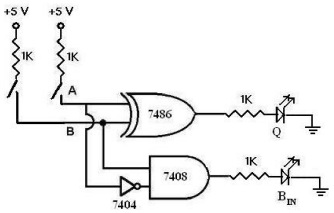

FIG. 9: Half Subtractor Circuit Diagram

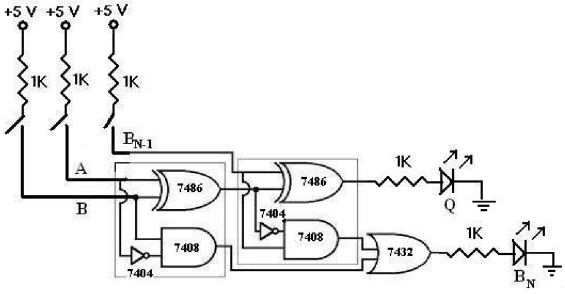

FIG. 10: Full Subtractor Circuit Diagram

Pinout Diagrams

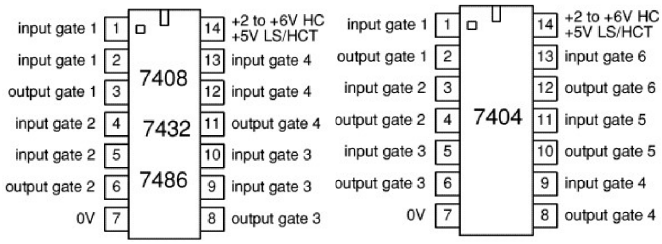

FIG. 11: Pin connections for different ICs used in this experiment

IV. OBSERVATIONS

The ICs were powered by 5V DC, `HIGH` inputs from 5V line, `LOW` inputs from ground. Outputs monitored with LEDs (LED on means 1, 0 otherwise).

A. Half Adder Circuit

Using the circuit given in Fig. 7.

A	B	Q	B_N
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

TABLE V: Observation table for the half adder circuit

B. Full Adder Circuit

Using the circuit given in Fig. 8.

B_{N-1}	A	B	Q	B_N
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

TABLE VI: Observation table for the full adder circuit

C. Half Subtractor Circuit

Using the circuit given in Fig. 9.

A	B	Q	B_N
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

TABLE VII: Observation table for the half subtractor circuit

D. Full Subtractor Circuit

Using the circuit given in Fig. 10.

B_{N-1}	A	B	Q	B_N
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

TABLE VIII: Observation table for the full subtractor circuit

E. Full Adder-Subtractor Circuit

Using the circuit given in Fig. 6.

B_{N-1}	A	B	Q	B_N
$X_1 = X_2 = 1$ (Full Subtractor)				
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1
$X_1 = X_2 = 0$ (Full Adder)				
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

TABLE IX: Observation table for the full adder-subtractor circuit

V. DISCUSSION & CONCLUSION

In this experiment we explored binary addition and subtraction and their practical implementation using logic gates. We discussed construction of N-bit adders/subtractors using ripple carry circuits. We also discussed the need for carry and borrow bits, their integration in full adder/subtractor circuits, and finally designing a combined adder-subtractor controlled by a signal.

VI. PRECAUTIONS

1. Make sure the connections are proper before switching on the circuit.
2. Make sure to connect a resistor parallel to the LED as to not burn out the LED.

VII. APPLICATIONS

Adders & Subtractors are wildly used in a computer's ALU (Arithmetic and Logic Unit) to perform operations as well as in CPUs and GPUs. They are also used in microcontrollers for arithmetic additions, program counters, timers and in networking and digital signal processing systems.

[1] SPS, *Study of Boolean Logic Operations using Digital ICs*, NISER (2023).

[2] P. Horowitz and W. Hill, *The art of electronics* (Cambridge University Press, 2015).