# Study of Common Emitter Transistor Amplifier Circuit

Gayatri P
*2nd year, Integrated M.Sc. Physics*
*Roll No.: 2211185*
(Dated: November 9, 2023)

A single-stage common emitter RC coupled amplifier is a simple and elementary amplifier circuit. The main purpose of this circuit is pre-amplification that is to make weak signals to be stronger enough for further amplification. In this experiment, we design RC coupled common emitter transistor amplifier circuit and study its characterstics, including how it responds to different frequencies.

## I. OBJECTIVE

To design a common emitter transistor (NPN) amplifier circuit, and to obtain the frequency response curve of the amplifier and to determine the mid-frequency gain, $A_{\text{mid}}$, lower and higher cutoff frequency of the amplifier circuit.

## II. THEORY

The most common circuit configuration for an NPN transistor is that of the Common Emitter Amplifier and that a family of curves known commonly as the Output Characteristics Curves, relates the Collector current ($I_C$), to the output or Collector voltage ($V_{CE}$), for different values of Base current ($I_B$). All types of transistor amplifiers operate using AC signal inputs which alternate between a positive value and a negative value. Presetting the amplifier circuit to operate between these two maximum or peak values is achieved using a process known as Biasing. Biasing is very important in amplifier design as it establishes the correct operating point of the transistor amplifier ready to receive signals, thereby reducing any distortion to the output signal. The single stage common emitter amplifier circuit shown below uses what is commonly called "Voltage Divider Biasing". The Base voltage ($V_B$) can be easily calculated using the simple voltage divider formula below:

$$V_B = \frac{V_{CC} R_2}{R_1 + R_2} \tag{1}$$

Thus the base voltage is fixed by biasing and it is independent of base current as long as the current in the divider circuit is large compared to the base current. Thus assuming $I_B \approx 0$, one can do the approximate analysis of the voltage divider network without using the transistor gain, $\beta$, in the calculation. Note that the approximate approach can be applied with a high degree of accuracy when the following condition is satisfied:

$$\beta R_E \geq 10 R_2 \tag{2}$$

### Load line and Q-point

A static or DC load line can be drawn onto the output characteristics curves of the transistor to show all the possible operating points of the transistor from fully "ON" ($I_C = V_{CC}/(R_C + R_E)$) to fully "OFF" ($I_C = 0$). The quiescent operating point or Q-point is a point on this load line which represents the values of $I_C$ and $V_{CE}$ that exist in the circuit when no input signal is applied. Knowing $V_B$, $I_C$ and $V_{CE}$ can be calculated to locate the operating point of the circuit as follows,

$$V_E = V_B - V_{BE} \tag{3}$$

So, the emitter current,

$$I_E \approx I_C = \frac{V_E}{R_E} \tag{4}$$

$$\text{and, } V_{CE} = V_{CC} - I_C(R_C + R_E) \tag{5}$$

It can be noted here that the sequence of calculation does not need the knowledge of $\beta$ and $I_B$ is not calculated. So the Q-point is stable against any replacement of the transistor. Since the aim of any small signal amplifier is to generate an amplified input signal at the output with minimum distortion possible, the best position for this Q-point is as close to the centre position of the load line as reasonably possible, thereby producing a Class A type amplifier operation, i.e. $V_{CE} = 1/2 V_{CC}$.

### Coupling and Bypass Capacitors

In CE amplifier circuits, capacitors $C_1$ and $C_2$ are used as Coupling Capacitors to separate the AC signals from the DC biasing voltage. The capacitors will only pass AC signals and block any DC component. Thus they allow coupling of the AC signal into an amplifier stage without disturbing its Q point. The output AC signal is then superimposed on the biasing of the following stages. Also a bypass capacitor, CE is included in the Emitter leg circuit. This capacitor is an open circuit component for DC bias, meaning that the biasing currents and voltages are not affected by the addition of the capacitor maintaining a good Q-point stability. However, this bypass capacitor acts as a short circuit path across the emitter resistor at high frequency signals increasing the voltage gain to its maximum. Generally, the value of the bypass capacitor, CE is chosen to provide a reactance of at most, 1/10th the value of $R_E$ at the lowest operating signal frequency.

### Amplifier Operation

Once the Q-point is fixed through DC bias, an AC signal is applied at the input using coupling capacitor $C_1$. During positive half cycle of the signal $V_B$E increases leading to increased $I_B$. Therefore $I_C$ increases by $\beta$ times leading to decrease in the output voltage, $V_{CE}$. Thus the CE amplifier produces an amplified output with a phase reversal. The voltage Gain of the common emitter amplifier is equal to the ratio of the change in the output voltage to the change in the input voltage. Thus,

$$A_V = \frac{V_{out}}{V_{in}} = \frac{\Delta V_{CE}}{\Delta V_{BE}} \tag{6}$$

The input ($Z_i$) and output ($Z_o$) impedances of the circuit can be computed for the case when the emitter resistor $R_E$ is completely bypassed by the capacitor, $C_E$:

$$Z_i = R_1 \parallel R2 \parallel \beta r_e \text{ and } Z_o = R_C \parallel r_o \tag{7}$$

where $r_e$ (26 mV/I$_E$) and $r_o$ are the emitter diode resistance and output dynamic resistance (can be determined from output characteristics of transistor). Usually $r_o \geq 10R_C$, thus the gain can be approximated as

$$\begin{aligned} A_V &= \frac{V_{out}}{V_{in}} \\ &= \frac{-\beta I_B (R_C \parallel r_o)}{I_B \beta r_e} \approx -\frac{R_C}{r_e} \end{aligned} \tag{8}$$

The negative sign accounts for the phase reversal at the output.

**Note:** In the circuit diagram provided below, the emitter resistor is split into two in order to reduce the gain to avoid distortion. So the expression for gain is modified as,

$$A_V = -\frac{R_C}{(R_{E1} + r_e)} \tag{9}$$

### Frequency Response Curve

The performance of an amplifier is characterized by its frequency response curve that shows output amplitude (or, more often, voltage gain) plotted versus frequency (often in log scale). Typical plot of the voltage gain of an amplifier versus frequency is shown in the figure below. The frequency response of an amplifier can be divided into three frequency ranges. The frequency response begins with the lower frequency range designated between 0 Hz and lower cutoff frequency. At lower cutoff frequency, $f_L$ , the gain is equal to 0.707 A$_{mid}$. A$_{mid}$ is a constant mid-band gain obtained from the mid-frequency range. The third, the higher frequency range covers frequency between upper cutoff frequency and above. Similarly, at higher cutoff frequency, $f_H$, the gain is equal to 0.707 A$_{mid}$. Beyond this the gain decreases with frequency increases and dies off eventually.

*a.* ***The Lower Frequency Range:*** Since the impedance of coupling capacitors increases as frequency decreases, the voltage gain of a BJT amplifier decreases as frequency decreases. At very low frequencies, the capacitive reactance of the coupling capacitors may become large enough to drop some of the input voltage or output voltage. Also, the emitter-bypass capacitor may become large enough so that it no longer shorts the emitter resistor to ground.

*b.* ***The Higher Frequency Range:*** The capacitive reactance of a capacitor decreases as frequency increases. This can lead to problems for amplifiers used for high-frequency amplification. The ultimate high cutoff frequency of an amplifier is determined by the physical capacitances associated with every component and of the physical wiring. Transistors have internal capacitances that shunt signal paths thus reducing the gain. The high cutoff frequency is related to a shunt time constant formed by resistances and capacitances associated with a node.

### Design

Before designing the circuit, one needs to know the circuit requirement or specifications. The circuit is normally biased for $V_{CE}$ at the mid-point of load line with a specified collector current. Also, one needs to know the value of supply voltage $V_{CC}$ and the range of $\beta$ for the transistor being used (available in the datasheet of the transistor).

Here the following specifications are used to design the amplifier,

$$V_{CC} = 12 \text{ V and } I_C = 1 \text{ mA}$$

Start by making $V_E = 0.1V_{CC}$. Then $R_E = V_E/I_E$ (Use $I_E \approx I_C$). Since $V_{CE} = 0.5V_{CC}$, Voltage across $R_C = 0.4V_{CC}$, i.e. $R_C = 4R_E$.

In order that the approximation analysis can be applied, $R_2 \leq 0.1\beta R_E$. Here $\beta$ is the minimum rated value in the specified range provided by the datasheet (in this case $\beta = 50$). Finally, $R_1 = (V_1/V_2)R_2$, $V_1$ ($= V_{CC} - V_2$)and $V_2$ ($= V_E + V_{BE}$) are voltages across $R_1$ and $R_2$ respectively. Based on these guidelines the components are estimated and the nearest commercially available values are used.

### Applications

The application of RC coupled amplifiers in music systems, has excellent audio fidelity over a wide range of frequencies. Therefore, they are widely used as voltage amplifiers (preamplifiers) Ex: in public address systems. They are also used in radio or TV Receivers as small signal amplifiers.

## III. EXPERIMENTAL SETUP

### Circuit components

1. Transistor (CL100 or equivalent)
2. Power supply
3. 6 resistors of various specifications
4. 3 Capacitors
5. Function Generator
6. Oscilloscope
7. Multimeters
8. Connecting wires
9. Breadboard

### Circuit Diagram

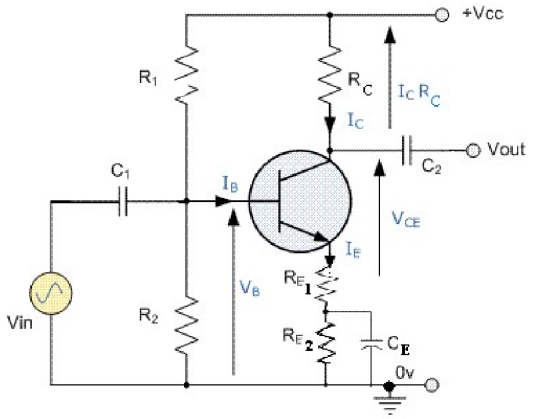


FIG. 1: Circuit diagram for the setup.

## IV. DATA ANALYSIS

- $V_{CC} = 12$ V
- $V_i$ (pp) $= 200$ mV
- $\beta = 168$
- $R_1 = 26.81\,k\Omega$
- $R_2 = (4.65 + 0.222) = 4.872\,k\Omega$
- $R_C = 3.849\,k\Omega$
- $R_{E1} = 0.4678\,k\Omega$, $R_{E2} = 0.5624\,k\Omega$, hence $R_E = 1.03\,k\Omega$
- $C_1 = 1.017\,\mu$F, $C_2 = 0.985\,\mu$F
- $C_E = 95.4\,\mu$F

We measured the following values from the D.C. analysis of the circuit.

| Parameter | Computed Value | Observed Value |
|---|---|---|
| $V_B$ (V) | 1.845 | 1.808 |
| $V_E$ (V) | 1.145 | 1.216 |
| $I_C \approx I_E$ (mA) | 1.11 | 1.19 |
| $V_{CE}$ (V) | 6.57 | 6.19 |

TABLE I: D.C. analysis of the circuit

From Table I, we can find the Q-point of the circuit as (6.19 V, 1.19 mA).

Hence, $r_e = 26\text{mV}/I_E = 21.85\,\Omega$. From Eq. (7),

$$\begin{aligned} Z_i &= R_1 \parallel R2 \parallel \beta r_e \\ &= \left(\frac{1}{26810} + \frac{1}{4872} + \frac{1}{168 \times 21.85}\right)^{-1} \\ &= 1.941\,\text{k}\Omega \end{aligned}$$

Similarly,

$$\begin{aligned} Z_o &= R_C \parallel r_o \\ &= \left(\frac{1}{R_C} + \frac{1}{r_o}\right)^{-1} \\ &\approx R_C = 3.849\,\text{k}\Omega \end{aligned}$$

Since $r_o$ is is the range of $\sim 100$ k$\Omega$, we can ignore it.

Also, we can find the theoretical value of $A_V$ in mid-frequency range from Eq. (9),

$$\begin{aligned} A_V &= \frac{3849}{467.8 + 21.85} = 7.861 \\ \text{or, Gain} &= 17.91\,\text{dB} \end{aligned}$$

Here is the plot of the frequency response curve of the circuit.

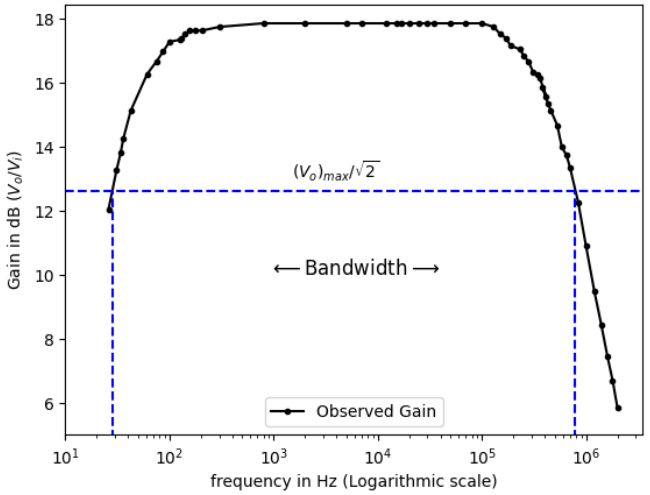


FIG. 2: Frequency response curve: $A_V$ vs. frequency plot

From Fig. 2, we can estimate the following values,

- Mid frequency Gain: 17.84 dB (or $V_o/V_i = 7.8$)
- Cut-off frequencies: 28.58 Hz and 784.16 kHz and
- Mid-frequency range: 800 Hz to 100 kHz and
- Bandwidth: 784.13 kHz

## V. ERROR ANALYSIS

From Eq. (9), we can find the error in the theoretical value of $A_V$ from,

$$\Delta A_V = \sqrt{\left(\frac{\partial A_V}{\partial R_C}\Delta R_C\right)^2 + \left(\frac{\partial A_V}{\partial R_{E1}}\Delta R_{E1}\right)^2 + \left(\frac{\partial A_V}{\partial r_e}\Delta r_e\right)^2} = 0.004$$

Using $\Delta R_C = 0.001$ kΩ, $\Delta R_{E1} = 0.1$ Ω and $\Delta I_E = 0.01$ mA, where $r_e = 26$ mV$/I_E$.

## VI. RESULTS AND DISCUSSION

We have successfully constructed a RC coupled common emitter transistor amplifier circuit, and anaysed its frequency response curve. We found that the gain is maximum and stable in the mid-frequency range. The bandwidth of the frequency response came out to be from 25.58 Hz to 784.16 kHz.

Using data from the D.C. analysis of the circuit, the input and output impedance of the circuit was calculated as $Z_i = 1.941$ kΩ and $Z_o = 3.849$ kΩ.

Similarly, the theoretical value of the mid-frequency gain was calculated as $7.861 \pm 0.004$ (or 17.91 dB). The observed value of mid-frequency gain is 7.8 (or 17.84 dB).

## VII. PRECAUTIONS

1. Vary the input signal frequency slowly.
2. Connect electrolytic capacitors carefully.

[1] SPS. Lab manual. *Website*, 2023. `https://www.niser.ac.in/sps/sites/default/files/7-RC%20coupled%20transistor%20amplifier.pdf`.