Study of Propagation Delay and Racing Condition in JK Flip-Flops

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I. OBJECTIVE

To study the propagation delay, racing condition along with rise and fall times of a JK flip-flop by analysing the oscilloscope waveforms.

II. THEORY

The JK flip flop, named after Jack Kilby who invented it is the most commonly used flip-flop. It is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs $S = R = 1$. Due to this additional clocked input, a JK flip-flop has four possible output combinations – 1, 0, *hold* and *toggle*.

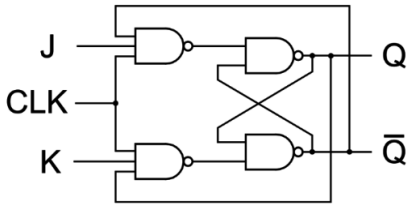


FIG. 1: Circuit diagram of a JK flip-flop

Assume the clock signal is 1. If $J = 1$ and $K = 0$, it behaves as a typical SR latch, i.e. $Q = 1$ and $Q' = 0$. Similarly for $J = 0$ and $K = 1$, $Q = 0$ and $Q' = 1$. If both $J = K = 0$, then it remains in the same state as it was before i.e. the `HOLD` state. But if both $J = K = 1$, the flip-flop changes state whenever a clock pulse occurs; i.e., the clock pulse toggles the flip-flop again and again until the Clk goes to 0. This is called is **race-around condition** (Fig. 2).

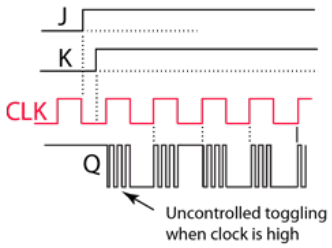


FIG. 2: Diagram depicting JK racing when the clock is high

To eliminate the race around condition, the following methods can be used:

- **Increasing the delay of flip-flop**
  The propagation delay (Δt) should be made greater than the duration of the clock pulse (T). But it is not a good solution as increasing the delay will decrease the speed of the system.
- **Use of edge-triggered flip-flop**
  If the clock is `HIGH` for a time interval less than the propagation delay of the flip flop then racing around condition can be eliminated. This is done by using the edge-triggered flip flop rather than using the level-triggered flip-flop.
- **Use of master-slave JK flip-flop**
  If the flip flop is made to toggle over one clock period then racing around condition can be eliminated. This is done by using Master-Slave JK flip-flop.

Now, practically a signal cannot travel instantaneously. Hence any signal will take some finite amount of time to transition between two a lower threshold and an upper threshold. **Rise time** measures the time taken for the signal to go from 10% to 90% of the signal high level. Similarly, **fall-time** measures the time taken for the signal to go from 90% to 10% of the signal high level.

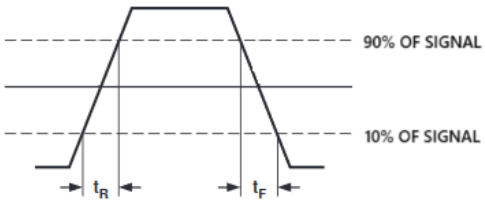


FIG. 3: Rise and fall times depicted in a timing diagram

So far we have assumed that at the clock edge, the flip-flop samples the input (or clock signal) and accordingly changes the output immediately. But practically, the flip-flop requires a certain time to respond to the change. Thus any change in the output of the flip flop will occur after a certain delay, also known as the **propagation delay**.

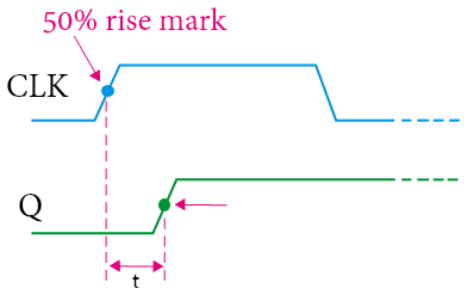


FIG. 4: Propagation delay depicted between the clock and Q

III. APPARATUS

1. ICs (3 input NAND-7410, NAND-7400)
2. DC Power Supply (5V)
3. Oscilloscope
4. Connecting Wires
5. Multimeters
6. Breadboard

IV. OBSERVATION AND CALCULATIONS

By anaylysing the oscilloscope output of a JK flip-flop, we have calculated the following parameters.

Rise and Fall Time

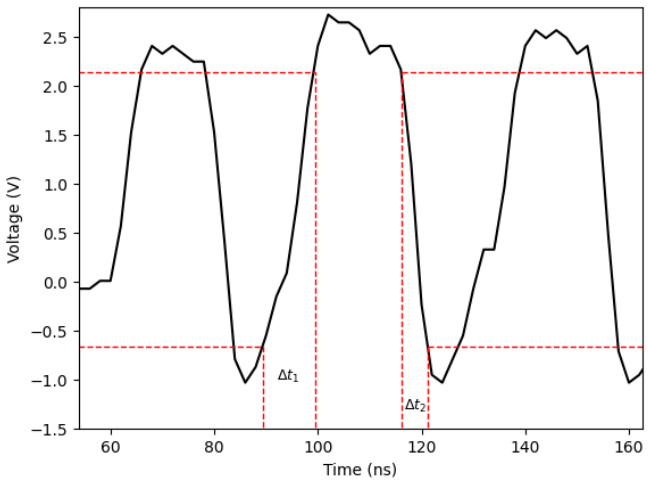
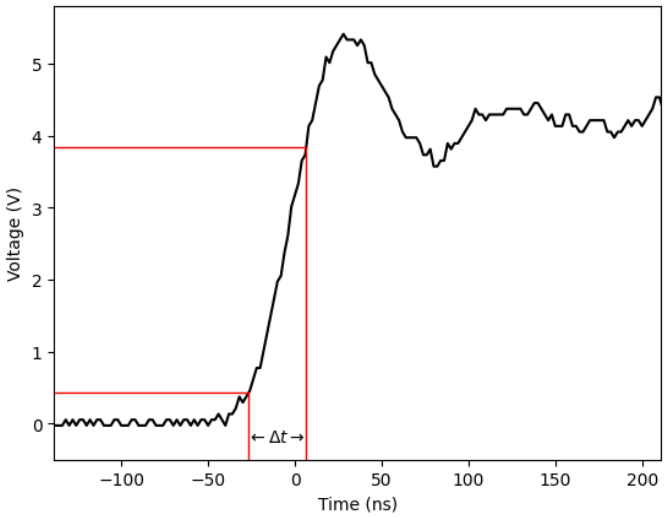
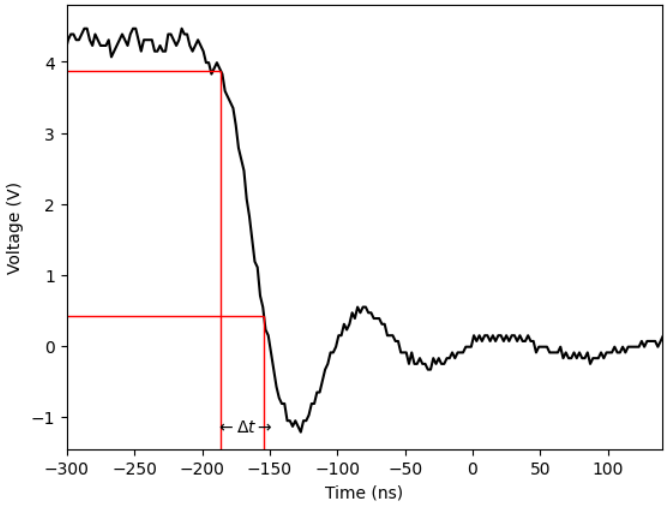


FIG. 5: Rise and fall times calculated from 10% to 90% marks (Δt_1 and Δt_2 respectively) for the JK output Q



(a)



(b)

FIG. 6: Plots depicting (a) rise time and (b) fall time of the clock signal

The rise and fall time of the clock signal came out to be almost equal at 32.9 ns and 31.8 ns respectively. Similarly, the rise and fall time of the JK output (Q) came out to be 10.15 ns and 5.11 ns. Here, the rise time is almost double the fall time.

Racing Condition

From the fig. 7, one can calculate the average time period of the toggling output as,

$$T_{\text{toggle}} = 36.1 \text{ ns}$$
$$\implies f_{\text{toggle}} = 27.7 \text{ MHz}$$

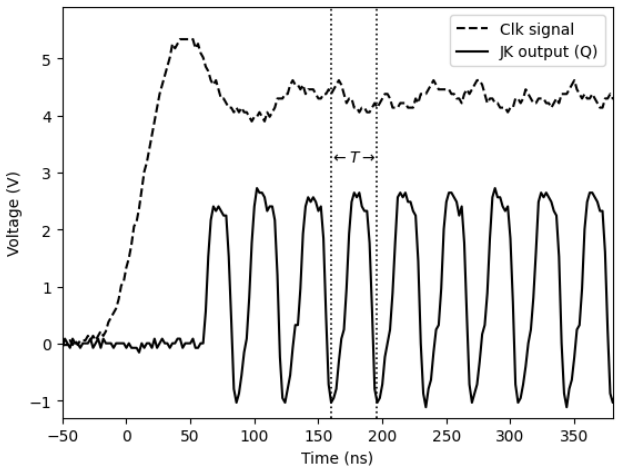


FIG. 7: Race-around condition depicted for the output Q once the clock goes high. T refers to the time period between successive toggles.

The high frequency ($\sim 10^7$ Hz) explains why one cannot observe racing condition by just observing the output through an LED.

Propagation Delay

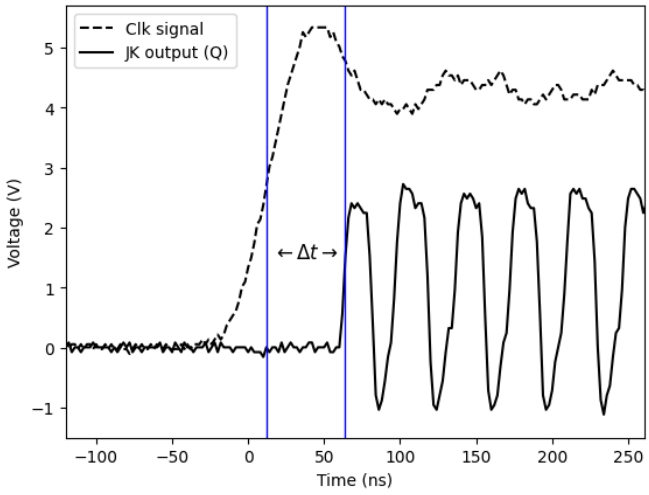


FIG. 8: Propagation delay depicted between the clock signal and the output Q as Δt

The propagation delay of the flip-flop is measured from the 50% rise mark of the clock signal to 50% that of the JK output (Q). This value came about to be around 51.2 ns.

As mentioned earlier, one of the ways to avoid the racing condition was to make the the propagation delay (Δt) should be made greater than the duration of the clock pulse (T), hence $T < 51.2$ ns.

V. DISCUSSION & CONCLUSION

In this experiment, we have calculated the typical values for rise and fall times, propagation delay and the race-around frequency for a JK flip flop constructed using NAND gates. These are the parameters measured for the output Q:

- Rise time: 10.15 ns
- Fall time: 5.11 ns
- Race-around frequency: 27.7 MHz
- Propagation delay: 51.2 ns

Moreover, the measured values for the rise and fall times of the clock signal are 32.9 ns and 31.8 ns respectively.

A typical JK flip-flop on an IC has propagation delay of around 4 ns. This is comparitively smaller than what we observed since in our case the circuit was built on a breadboard and the (relatively) longer wires create bigger delays.

Although small, these values are significant in designing any bigger circuit. For example, consider the case where there are two flip-flops with a 10 ns delay between them. If you use a clock that runs at 50 MHz (20 ns period) you will be safe. However if you use a 200 MHz clock (5 ns period) the design will fail to work properly. The longer the propagation delay, the slower the clock is able to run. Hence the speed of the system is ultimately dependent on these values.