Design and Study of IC 555 Multivibrator Circuits

Gayatri P
2nd year, Integrated M.Sc. Physics
Roll No.: 2211185
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In the experiment, we discuss the design and construction of different multivibrator circuits using the IC 555 timer. We also briefly talk about the design and principle of the IC 555 chip.

I. OBJECTIVE

To design and study the following circuits using IC 555:
1. An astable multivibrator
2. A monostable multivibrator
3. A bistable multivibrator

II. THEORY

Sequential Logic circuits can be used to build more complex circuits like counters, shift registers, latches or memories, but for these types of circuits to operate in a sequential manner, they require some kind of a clock pulse or timing signal which can cause them to change their state. Clock pulses are generally square-shaped waves that are produced by a single pulse generator circuit such as a Multivibrator which oscillates between a `HIGH` and a `LOW` state. Sequential logic circuits that use the clock signal for synchronization change their state on either the rising or falling edge, or both of the clock signal.

A duty cycle or power cycle is the fraction of one period in which a signal or system is active. Generally, these signals have an even 50% duty cycle, i.e. it has a 50% `ON` time and a 50% `OFF` time. There are basically three types of pulse generation circuits depending on the number of stable states,

- **Astable** has no stable states — it continually switches from one state to the other at a fixed frequency.
- **Monostable** in which one of the states is stable, but the other state is unstable (or transient). A trigger pulse causes the circuit to enter the unstable state. After entering the unstable state, the circuit will return to the stable state after a set time. Such a circuit is useful for creating a timing period of fixed duration in response to some external event.
- **Bistable** in which the circuit is stable in either state. It can be flipped from one state to the other by an external trigger pulse.

IC 555 Timer

Initially called the "The IC Time Machine", the 555 timer is an integrated circuit used in a variety of timer, delay, pulse generation, and oscillator applications and is one of the most popular timing ICs.

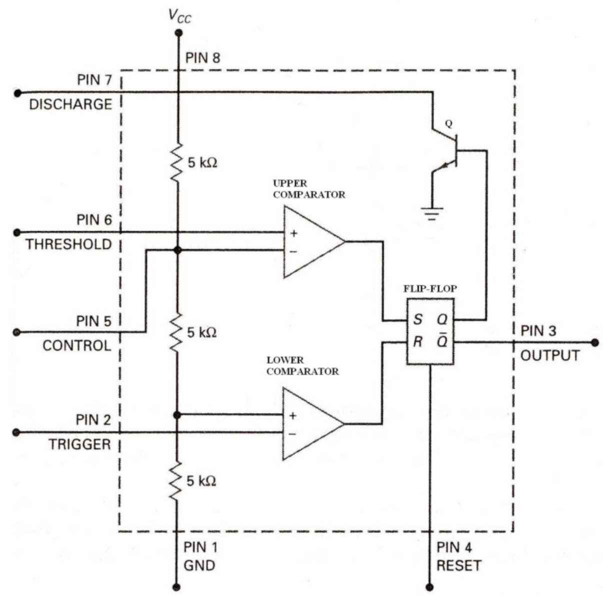


FIG. 1: Functional block diagram of IC 555

The 555 time typically comes with 8 pins:

Pin 1: *(Ground)* All voltages are measured with respect to this terminal.

Pin 2: *(Trigger)* The output of the timer depends on the amplitude of the external trigger pulse applied to this pin. When a negative going pulse of amplitude greater than $1/3\,V_{CC}$ is applied to this pin, the output of the timer high. The output remains high as long as the trigger terminal is held at a low voltage.

Pin 3: *(Output)* The output of the timer is measured with respect to ground. There are two ways by which a load can be connected to the output terminal – either between pin 3 and ground or between pin 3 and supply voltage $+V_{CC}$. When the output is low the load current flows through the load connected between pin 3 and $+V_{CC}$ into the output terminal and is called *sink current.* The current through the grounded load is zero when the output is low. For this reason the load connected between pin 3 and $+V_{CC}$ is called the *normally on load* and that connected between pin 3 and ground is called *normally off-load.* On the other hand, when the output is high the current through the load connected between pin 3 and $+V_{CC}$ is zero. The output terminal supplies current to the normally off load. This current is called *source current.* The maximum value of sink or source current is 200mA.

Pin 4: *(Reset)* The 555 timer can be reset (disabled) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to $+V_{CC}$ to avoid any possibility of false triggering.

Pin 5: *(Control Voltage)* An external voltage applied to this terminal changes the threshold as well as trigger voltage. Thus by imposing a voltage on this pin or by connecting a pot between this pin and ground, the pulse width of the output waveform can be varied. When not used, the control pin should be bypassed to ground with a 0.01 μF Capacitor to prevent any noise problems.

Pin 6: *(Threshold)* When the voltage at this pin is greater than or equal to the threshold voltage $2/3\,V_{CC}$, the output of the timer low.

Pin 7: *(Discharge)* This pin is connected internally to the collector of transistor Q. When the output is high Q is OFF and acts as an open circuit to external capacitor C connected across it. On the other hand, when the output is low, Q is saturated and acts as a short circuit, shorting out the external capacitor C to ground.

Pin 8: *($+V_{CC}$)* The supply voltage of +5V to + 18V is applied to this pin with respect to ground.

Operation

Represented with a block diagram (Fig. 1) a 555 timer consists of 2 comparators, a flip-flop, a voltage divider, a discharge transistor and an output stage. The 555 Timers name comes from the fact that there are three 5kΩ resistors connected together internally producing a voltage divider network between the supply voltage at pin 8 and ground at pin 1. The voltage across this series resistive network holds the negative inverting input of comparator two at $2/3\,V_{CC}$ and the positive non-inverting input to comparator one at $1/3\,V_{CC}$.

The two comparators produce an output voltage dependent upon the voltage difference at their inputs which is determined by the charging and discharging action of the externally connected RC network. The outputs from both comparators are connected to the two inputs of the flip-flop which in turn produces either a `HIGH` or `LOW` level output at Q based on the states of its inputs. The output from the flip-flop is used to control a high current output switching stage to drive the connected load producing either a `HIGH` or `LOW` voltage level at the output pin.

The 555 can operate in either mono/bi-stable or astable mode, depending on the connections to and the arrangement of the external components. Thus, it can either produce a single pulse when triggered, or it can produce a continuous pulse train as long as it remains powered.

A. Astable Multivibrator

These circuits are not stable in any state and switch outputs after predetermined time periods. The result of this is that the output is a continuous square/rectangular wave with the properties depending on values of external resistors and capacitors. Thus, while designing these circuits following parameters need to be determined – the frequency of the wave and its duty cycle.

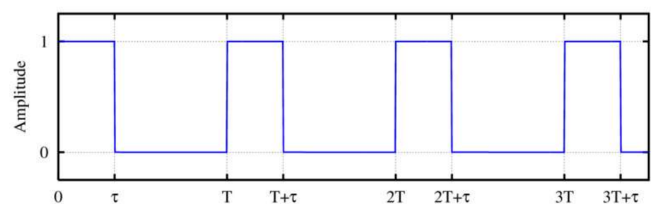


FIG. 2: A periodic rectangular waveform with frequency $1/T$ and a duty cycle of $\tau/T \times 100\%$

1. *With duty cycle more than 50%*

An astable multivibrator can be designed as shown in the circuit diagram (with typical component values) using IC 555, for a duty cycle of more than 50%. The corresponding voltage across the capacitor and voltage at output is also shown. The astable function is achieved by charging/discharging a capacitor through resistors connected, respectively, either to V_{CC} or GND. Switching between the charging and discharging modes is handled by resistor divider $R_1 - R_3$, two Comparators, and an RS Flip-Flop in IC 555. The upper or lower comparator simply generates a positive pulse if V_{CC} goes above 2/3 V_{CC} or below 1/3 V_{CC}. And these positive pulses either `SET` or `RESET` the Q output.

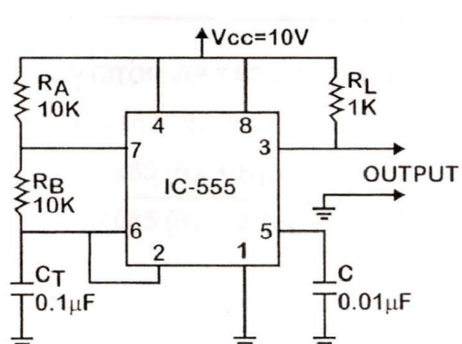


FIG. 3: Circuit diagram of an astable multivibrator with duty cycle more than 50%

The time for charging C from 1/3 to 2/3 V_{CC} (ON)

$$= 0.693\,(R_A + R_B)\,C$$

The time for discharging C from 2/3 to 1/3 V_{CC} (OFF)

$$= 0.693\,R_B\,C$$

The total oscillation period,

$$T_{\text{osc}} = 0.693\,(R_A + 2R_B)\,C$$

$$\implies f_{\text{osc}} = \frac{1.44}{(R_A + 2R_B)C} \tag{1}$$

$$\text{and, Duty Cycle} = \frac{R_A + R_B}{R_A + 2R_B} \tag{2}$$

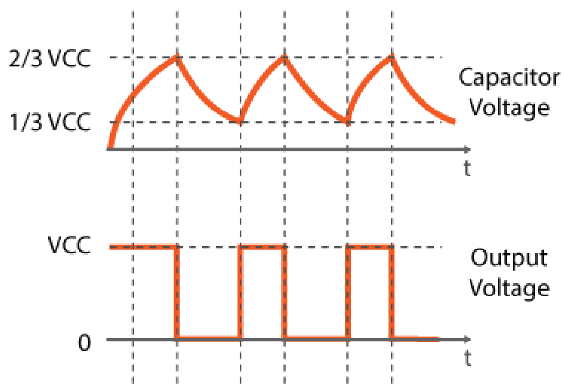


FIG. 4: The voltage across the capacitor compared with the output voltage across time (for an arbitrary duty cycle)

2. *With duty cycle less than 50%*

Here a diode D_1 is connected between the discharge and threshold terminals (as also across RB). Thus the capacitor now charges only through R_A (since R_B is shorted by diode conduction during charging) and discharges through R_B. Another optional diode D_2 is also connected in series with R_B in reverse direction for better shorting of R_B. Therefore, the frequency of oscillation and duty cycle are

$$f_{\text{osc}} = \frac{1.44}{(R_A + R_B)C} \tag{3}$$

$$\text{Duty Cycle} = \frac{R_A}{R_A + 2R_B} \tag{4}$$

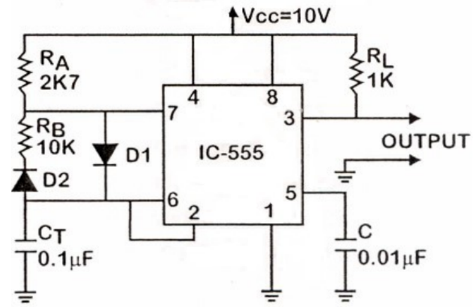


FIG. 5: Circuit diagram of an astable multivibrator with duty cycle less than 50%

3. *With duty cycle variable from 0 to 100%*

Here a potentiometer, R_X, is used so that $R_A = R_1 + R_2$, $R_B = R_X - R_2 + R_3$. A diode is now connected across a variable R_B. Thus a variable duty cycle is achieved. Therefore, the frequency of oscillation and duty cycle can be derived as follows.

$$f_{\text{osc}} = \frac{1.44}{(R_1 + R_X + R_3)C} \tag{5}$$

$$\text{Min. Duty Cycle} = \frac{R_1}{R_1 + R_X + R_3} \tag{6}$$

$$\text{Max. Duty Cycle} = \frac{R_1 + R_X}{R_1 + R_X + R_3} \tag{7}$$

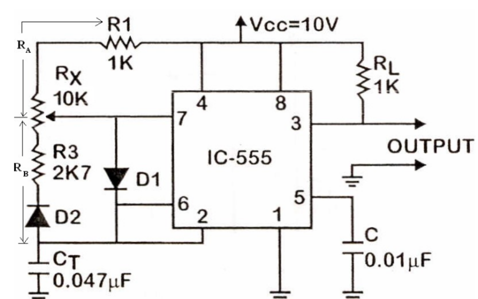


FIG. 6: Circuit diagram of an astable multivibrator with variable duty cycle from 0 to 100%

B. Monostable Multivibrator

Monostable multivibrator or a one shot multivibrator is a pulse generating circuit where the duration of this pulse is determined by the RC network connected externally. When a negative pulse is applied to the trigger input (pin 2) of the Monostable oscillator, the internal comparator, detects this input and "sets" the state of the flip-flop, changing the output from a `LOW` state to a `HIGH` state. This action turns "OFF" the discharge transistor connected to pin 7, removing the short circuit across the external timing capacitor, C.

This allows the timing capacitor to start to charge up through resistor, R until the voltage across the capacitor reaches the threshold (pin 6) voltage of $2/3\, V_{CC}$ set up by the internal voltage divider network. At this point the comparator's output goes HIGH and "resets" the flip-flop back to its original state which in turn turns "ON" the transistor and discharges the capacitor to ground through pin 7. This causes the output to change its state back to the original stable LOW value awaiting another trigger pulse to start the timing process over again. Then as before, the Monostable Multivibrator has only 1 stable state.

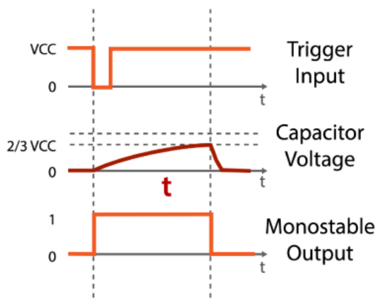


FIG. 7: The voltage across the capacitor compared with the output voltage and the input trigger across time

The Monostable 555 Timer circuit triggers on a negative-going pulse applied to pin 2 and this trigger pulse must be much shorter than the output pulse width allowing time for the timing capacitor to charge and then discharge fully. Once triggered, the 555 Monostable will remain in this HIGH unstable output state until the time period set up by the RC network has elapsed. The amount of time that the output voltage remains HIGH or at a logic 1 level, is given by the following time constant equation,

$$T = 1.1\, RC \tag{8}$$

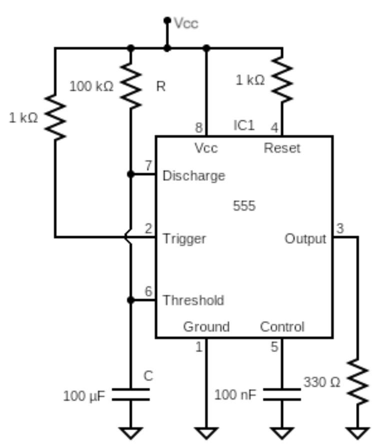


FIG. 8: Circuit diagram of a monostable multivibrator

C. Bistable Multivibrator

In these circuits, the output is stable in both states. The states are switched using an external trigger but unlike the monostable multivibrator, it does not return back to its original state. Another trigger is needed for this to happen. This operation is similar to a flip-flop. There are no RC timing networks and hence no design parameters. The following circuit can be used to design a bistable multivibrator. The trigger and reset inputs (pins 2 and 4 respectively on a 555) are held high via pull-up resistors while the threshold input (pin 6) is simply grounded. Thus configured, pulling the trigger momentarily to ground acts as a SET and transitions the output pin (pin 3) to V_{CC} (high state). Pulling the threshold input to supply acts as a RESET and transitions the output pin to ground (low state).

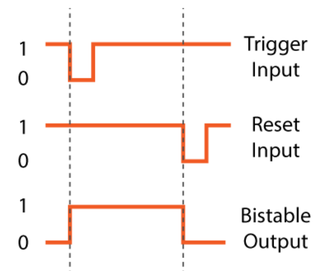


FIG. 9: The input and reset triggers along with the multivibrator output voltage waveforms

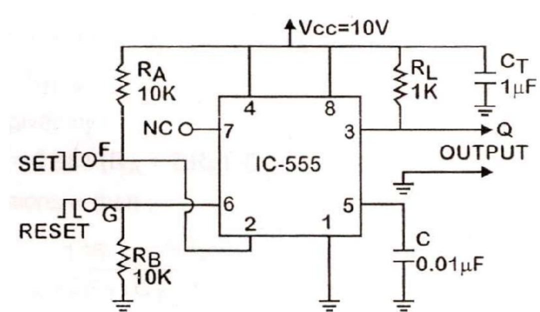


FIG. 10: Circuit diagram of a bistable multivibrator

III. APPARATUS

1. IC 555
2. Resistors
3. Potentiometer
4. Capacitors
5. Diodes
6. Multimeters
7. Oscilloscope
8. D.C. Power Supply (10V)
9. Connecting Wires
10. Breadboard

IV. OBSERVATION AND CALCULATIONS

1. Astable Multivibrator

(a) With duty cycle more than 50%

- $R_A = 9.87$ kΩ, $R_B = 9.75$ kΩ
- $C_T = 10.30$ nF

Parameter	Theoretical Value	Observed Value	Error
f_{osc}	492.3 ± 0.6 Hz	490.2 Hz	−0.3%
Duty Cycle	66.80 ± 0.02 %	66.7%	−0.1%

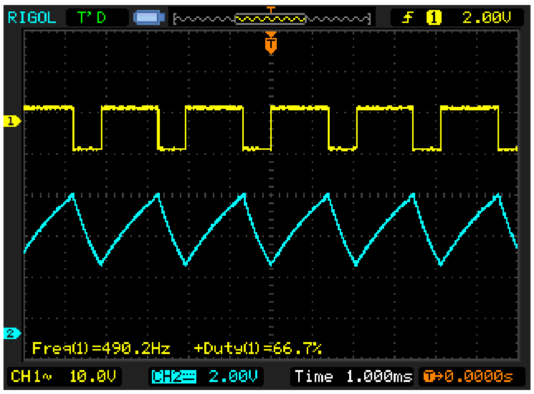


FIG. 11: Oscilloscope output of an astable multivibrator (above) with duty cycle 66.7% and the voltage across C_T (below)

(b) With duty cycle less than 50%

- $R_A = 2.844$ kΩ, $R_B = 9.75$ kΩ
- $C_T = 10.3$ nF

Parameter	Theoretical Value	Observed Value	Error
f_{osc}	1.148 ± 0.002 kHz	1.020 kHz	−12.5%
Duty Cycle	22.58 ± 0.06 %	22.4%	−0.8%

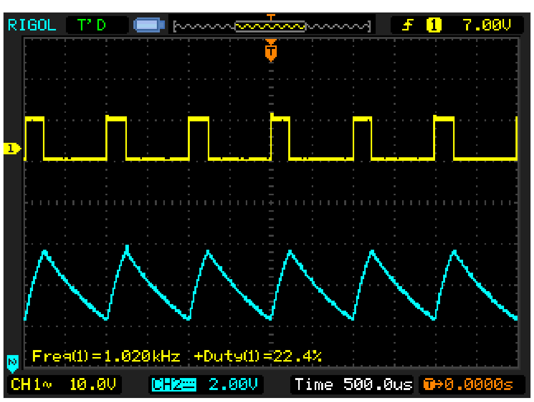
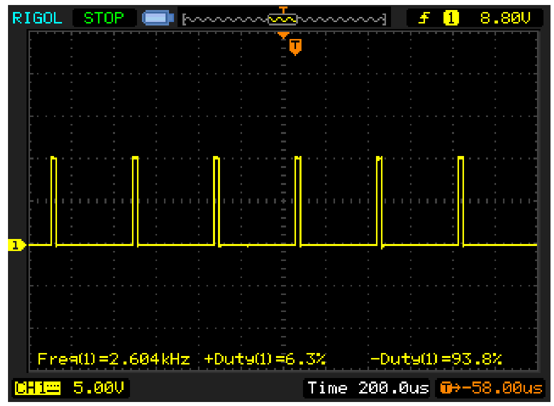


FIG. 12: Oscilloscope output of an astable multivibrator (above) with duty cycle 22.4% and the voltage across C_T (below)

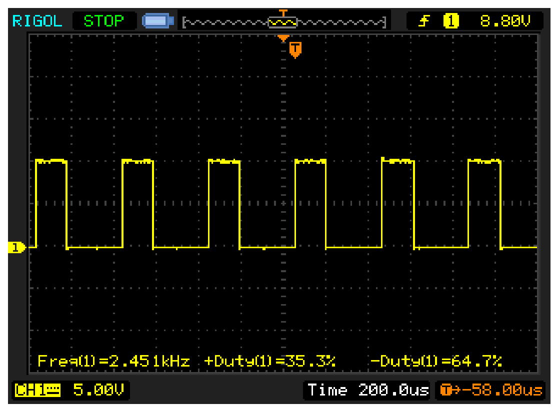
(c) With variable duty cycle from 0 to 100%

- $R_1 = 0.975$ kΩ, $R_3 = 2.844$ kΩ
- $R_X = 10.19$ kΩ
- $C_T = 10.3$ nF
- Theoretical $f_{osc} = 2.150 \pm 0.005$ kHz

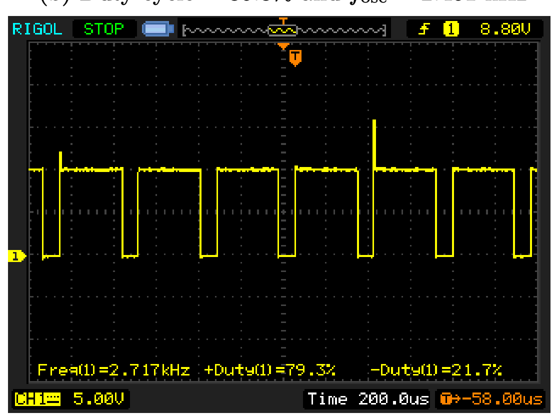
Oscilloscope Outputs



(a) Duty cycle = 6.3% and $f_{osc} = 2.604$ kHz



(b) Duty cycle = 35.3% and $f_{osc} = 2.451$ kHz



(c) Duty cycle = 79.3% and $f_{osc} = 2.717$ kHz

FIG. 13: Oscilloscope outputs of an astable multivibrator with variable duty cycle

R_A (kΩ)	R_B (kΩ)	Observed f_{osc} (kHz)	Duty Cycle (%) Observed	Duty Cycle (%) Theoretical	Error
0.978	12.984	2.604	6.3	6.97 ± 0.01	−9.6%
5.541	8.784	2.451	35.3	39.55 ± 0.08	−10.7%
7.585	6.647	2.525	51.5	54.14 ± 0.08	−4.9%
11.11	2.846	2.717	79.3	79.69 ± 0.09	−0.3%

Minimum duty cycle = 6.3%
Maximum duty cycle = 79.3%
Avg. f_{osc} = (2.574 ± 0.114) kHz

2. Monostable Multivibrator

- $R = 99.7$ kΩ, $C = 96\,\mu$F
- Pulse width (Output High Duration):
  - Observed: 10.96 s
  - Calculated: (10.53 ± 0.02) s
  - Error: 3.9%

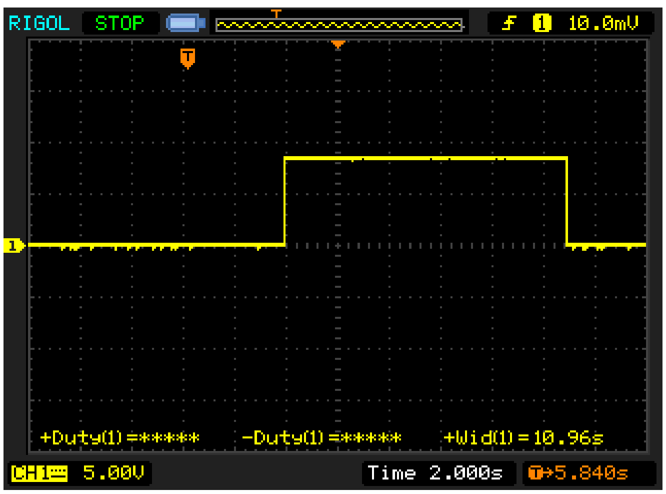
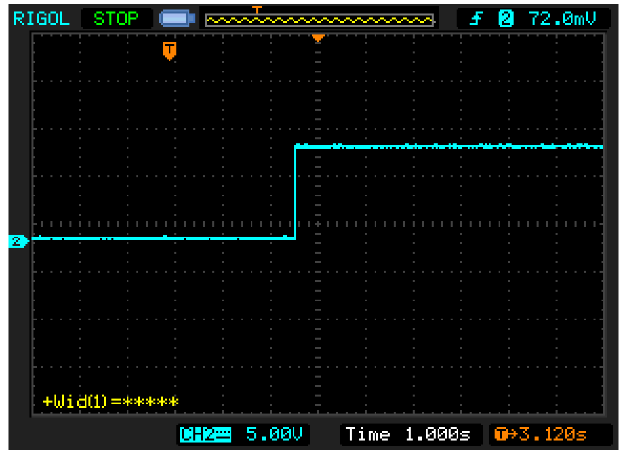


FIG. 14: Oscilloscope output of a monostable multivibrator with pulse width = 10.96 s

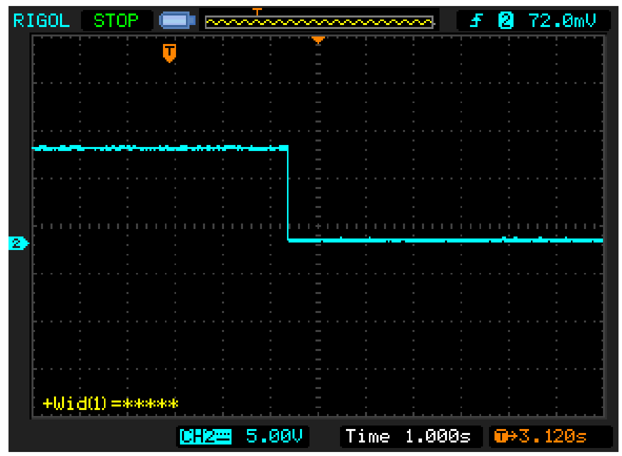
3. Bistable Multivibrator

According to Fig. 10, F refers to the `TrIGGER` pin which is used output the `SET` state and and G refers to the `THRESHOLD` which is used to get the `RESET` state.

Point	Connected to	Output
F	Ground	SET
G	V_{CC}	RESET



(a)



(b)

FIG. 15: Oscilloscope outputs of a bistable multivibrator for (a) SET condition and (b) RESET condition

V. DISCUSSION & CONCLUSION

In this experiment, we have successfully built and studied the properties of multivibrator circuits using the IC 555 timer.

We built an astable multivibrator where the astable function was achieved through acharging and discharging capacitors through resistors and we varied the duty cycle and the frequency of the resulting rectangular wave by varying the resistance and capacitance values. Using a potentiometer, we were able to vary the duty cycle of the output wave from 6.3% to 79.3% around an oscillating frequency of 2.574 kHz.

We also built a monostable multivibrator with a pulse width of 10.96s, which was triggered by a negative pulse applied to the `TRIGGER` pin. Furthermore, we also built a bistable multivibrator with two stable states, `SET` and `RESET`, both of which are again externally triggered.

VI. PRECAUTIONS

1. Make sure all the connections are proper before switching on the circuit.
2. Make sure to give 10V as the power supply (V_{CC}).
3. Make sure to ground the oscilloscope probes or else they will show distorted output.

VII. APPLICATIONS

Astable multivibrators have widespread usage across a variety of domains like communication systems – for frequency generation and modulation, in timing and control circuits, in testing equipment – to serve as signal generators to provide inputs for device testing, and in power supply systems – where they act as oscillators.

[1] SPS, *Design and Study of IC 555 Multivibrator Circuits*, NISER (2024).
[2] P. Horowitz and W. Hill, *The art of electronics* (Cambridge University Press, 2015).