Study of Counter Circuits

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In this experiment, we construct and study counter circuits using JK flip-flops including ripple up/down, MOD-N and ring counters. We discuss the concept of frequency division in building counter ripple counter circuits. We also build a synchronous ring counter and study its working.

I. OBJECTIVE

To construct and study the operations of the following circuits.

1. A 4-bit binary ripple Up-counter
2. A 4-bit binary ripple Down-counter
3. A Mod-N counter
4. A Ring counter

II. THEORY

One of the applications of sequential logic flip-flop circuits are counter circuits. A binary counter can count from 0 to $2^n - 1$, where n is the total number of bits in the counter. They can be constructed using a series of flip-flops where each flip-flop represents one bit of information.

Based on the application of clock pulse, there are two types of counter circuits:

- **Asynchronous Counters** or ripple counters where the flip flops do not receive the same clock pulse at the same time. Each flip flop is triggered by the output of the previous flip flop, and therefore there exists some propagation delay.
- **Synchronous Counters** where all the flip flops receive the same clock pulse at the same time and their outputs change simultaneously. This will result in the no propagation delay between the flip flops.

Frequency Division

A frequency divider can be constructed from J-K flip-flops by taking the output of one cell to the clock input of the next. The J and K inputs of each flip-flop are set to 1 to produce a toggle at each cycle of the clock input. For each two toggles of the first cell, a toggle is produced in the second cell, so its output is at half the frequency of the first. The output of the fourth cell is hence 1/16 the clock frequency. The same device is useful as a binary counter.

Hence the output at any point has an exact 50% duty cycle. The final output clock signal will have a frequency value equal to the input clock frequency divided by the MOD number of the counter. Such circuits are known as *divide-by-n* counters, where n is the number of counter stages used.

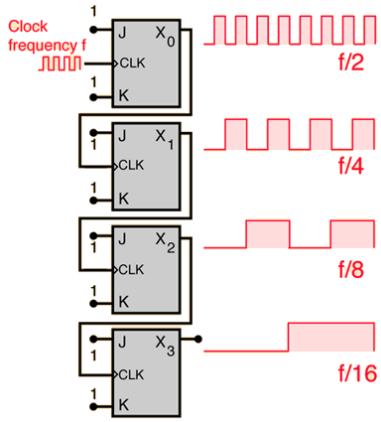

FIG. 1: An example of a frequency division circuit using JK flip flops

A. Binary Ripple Up Counter

A 4-bit or MOD-16 ripple up counter can be constructed from 4 J-K flip-flops by taking the output of one cell to the clock input of the next. The J and K inputs of each flip-flop are set to 1 to produce a toggle at each cycle of the clock input. For each two toggles of the first cell, a toggle is produced in the second cell, so its output is at half the frequency of the first. The output of the fourth cell is 1/16 the clock frequency.

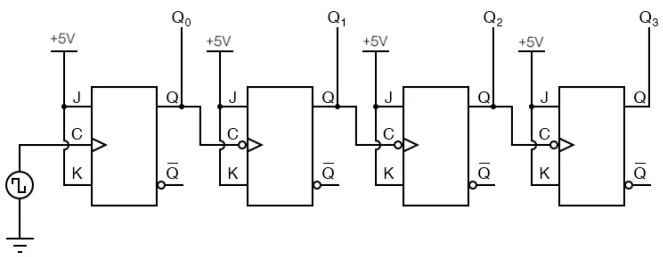

FIG. 2: Circuit diagram for a 4-bit binary ripple up counter. The PRESET and CLR pins are connected to HIGH

The counting sequence corresponding to each input pulse is based on its binary representation in 4-bits (i.e. from 0000 to 1111). On supplying the 15th pulse the counter reads 1111 (decimal 15). The next clock pulse after count 1111 will cause the counter to try to increment to 10000 (decimal 16). However, that 1 bit is not held by any flip-flop and is therefore lost. As a result, the counter actually reverts to 0000, and the count begins again.

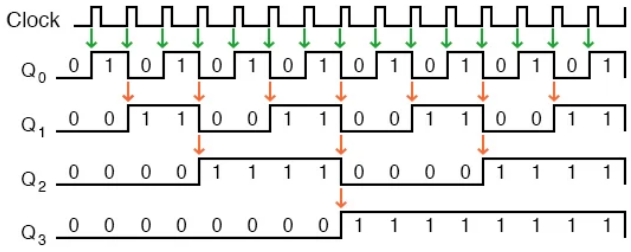

FIG. 3: The ripple up circuit would yield the following output waveforms, when clocked by a repetitive source of pulses from a function generator

B. Binary Ripple Down Counter

The binary ripple down-counter decreases the count by one each time a pulse occurs at the input. Here, the complement output of one flip-flop is connected to the clock input of the subsequent flip-flop. This toggles at each negative edge of the clock pulse ($1 \rightarrow 0$ transition), which is equivalent to a normal output toggling for the positive edge of the clock pulse (0 to 1 transition). Thus, the counter starts from 1111 with the first pulse after it is reset and reverts back to 0000 on the 16th pulse.

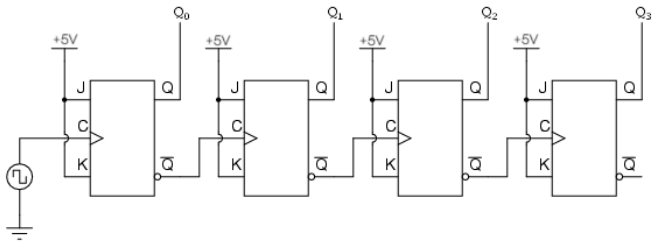

FIG. 4: Circuit diagram for a 4-bit binary ripple down counter. The PRESET and CLR pins are connected to HIGH

C. Modulus-N Counter

The modulus of a counter is the number of discrete states a counter can take up. A counter with n no. of flip flops will have 2^n number of possible states. So counters with modulus $2, 4, 8, \ldots$ can be built up using $1, 2, 3, \ldots$ flip flops.

If one has to design a counter with N states where N is not a power of 2, we can construct a counter of the next higher power of 2, such that $2^n > N$ and then arrange the circuit in such a way that it skips some of its natural states restricting it to N.

The simplest way of doing this is the *direct clearing method*, where a gate circuit is used to clear all the flip flops as the desired count is reached. For this an additional combinational logic circuit, a 4-input NAND gate is required, whose output is connected to clear (`CLR`) terminal of all the flip flops. This will feed a reset pulse to the counter during state N so that immediately after state $N-1$.Hence, the flip-flops are reset and the counter starts counting again.

For example here is the circuit diagram for a MOD-12 counter. This will feed a reset pulse during state 12 (1100). So the counter will run from 0000 to 1011 and then loop back again to 0000 on the 12th pulse.

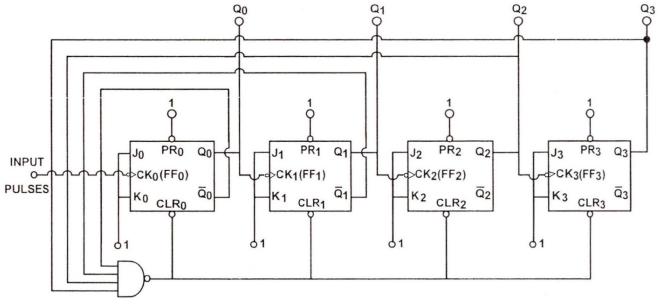

FIG. 5: Circuit diagram for a MOD-12 ripple up counter

D. Ring Counter

A *shift register* is a type of digital circuit using a cascade of flip-flops where the output of one flip-flop is connected to the input of the next. They share a single clock signal, which causes the data stored in the system to shift from one location to the next. A ring counter is a special type of Shift register where the output of the last flip flop is passed to the first flip flop as an input. This configuration creates a cyclic shift of the data bits through the flip-flops.

When a clock signal is applied to the ring counter, the data bits are shifted from one flip-flop to the next with each clock cycle. As a result, the ring counter generates a sequence of binary states that repeat after a specific number of clock cycles, depending on the number of flip-flops in the circuit.

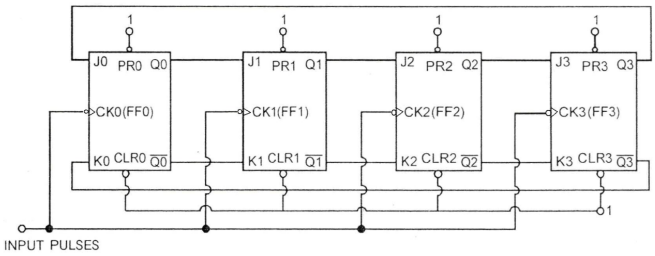

FIG. 6: Circuit diagram for a ring counter

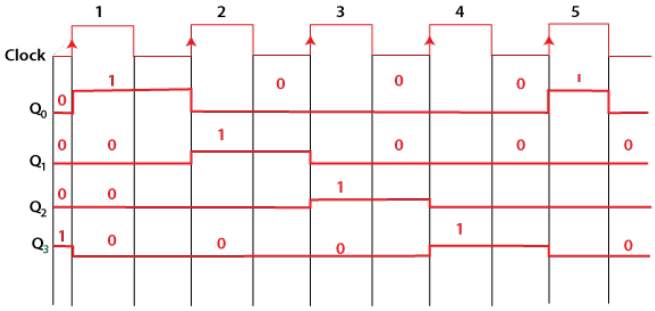

FIG. 7: Signal diagram for a ring counter circuit

Ring counter is extremely fast but it is uneconomical in the number of flip-flops. This is overcome by a modified circuit known as a Johnson counter or switchtail ring counter or twisted counter, where the outputs of the last flip-flop are crossed over and then fed back to the first flip-flop. That is the normal and complement output of the last flip-flop are connected to the K and J inputs of the first flip-flop respectively.

III. EXPERIMENTAL SETUP

Apparatus

1. ICs:
   (a) JK Flip-flop (FF-7476)
   (b) 4-input NAND (7420)
2. Resistors (1 kΩ)
3. DC Power Supply (5V)
4. Function Generator
5. Oscilloscope
6. Breadboard
7. Connecting Wires

IC Pinout Diagrams

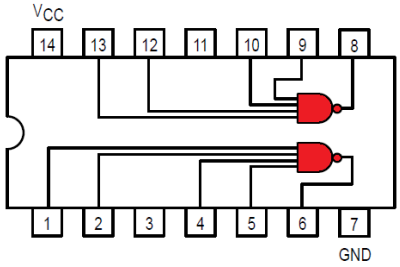

FIG. 8: IC pinout diagram for a 4 input NAND gate (IC 7420)

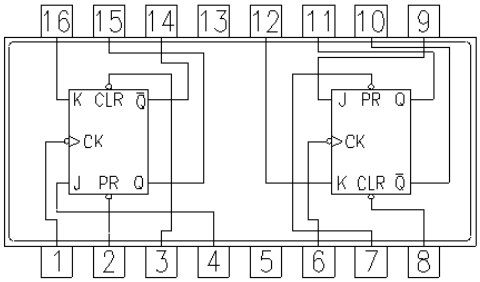

FIG. 9: IC pinout diagram for a JK flip flop (IC 7476)

IV. OBSERVATIONS

1. Ripple Up Counter

	Binary Count				
Input Pulse	Q_3 2^3	Q_2 2^2	Q_1 2^1	Q_0 2^0	Decimal Count
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	2
3	0	0	1	1	3
4	0	1	0	0	4
5	0	1	0	1	5
6	0	1	1	0	6
7	0	1	1	1	7
8	1	0	0	0	8
9	1	0	0	1	9
10	1	0	1	0	10
11	1	0	1	1	11
12	1	1	0	0	12
13	1	1	0	1	13
14	1	1	1	0	14
15	1	1	1	1	15
16	0	0	0	0	0 (RESET)

TABLE I: Characterstic Table for a Ripple Up Counter Circuit (Refer Fig. 2)

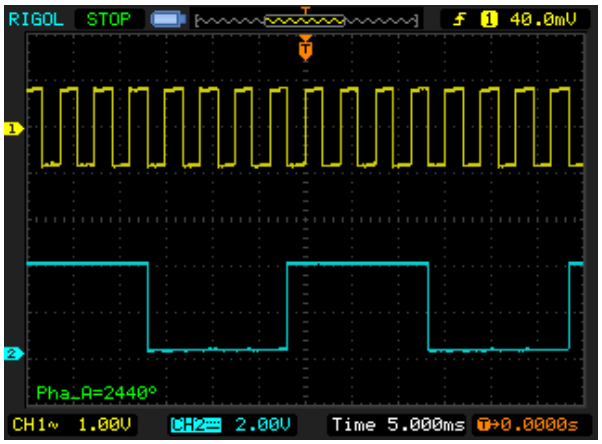

FIG. 10: The oscilloscope output for the least (above) and the most significant bit (below), i.e. Q_0 and Q_3 in a 4-bit ripple up counter circuit. One can observe that the frequency of Q_3 is 1/4th that of Q_0

2. MOD-12 Ripple Up Counter

	Binary Count				
Input Pulse	Q_3 2^3	Q_2 2^2	Q_1 2^1	Q_0 2^0	Decimal Count
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	2
3	0	0	1	1	3
4	0	1	0	0	4
5	0	1	0	1	5
6	0	1	1	0	6
7	0	1	1	1	7
8	1	0	0	0	8
9	1	0	0	1	9
10	1	0	1	0	10
11	1	0	1	1	11
12	0	0	0	0	0 (RESET)

TABLE II: Characterstic Table for a MOD-12 Ripple Up Counter Circuit (Refer Fig. 5)

3. Ring Counter

Input Pulses	Binary States			
	Q_3	Q_2	Q_1	Q_0
0	0	0	0	1
1	0	0	1	0
2	0	1	0	0
3	1	0	0	0
4	0	0	0	1
5	0	0	1	0
6	0	1	0	0
7	1	0	0	0
8	0	0	0	1

TABLE III: Characterstic Table for a Ring Counter Counter Circuit (Refer Fig. 6)

4. Ripple Down Counter

	Binary Count				
Input Pulse	Q_3 2^3	Q_2 2^2	Q_1 2^1	Q_0 2^0	Decimal Count
0	0	0	0	0	0
1	1	1	1	1	15
2	1	1	1	0	14
3	1	1	0	1	13
4	1	1	0	0	12
5	1	0	1	1	11
6	1	0	1	0	10
7	1	0	0	1	9
8	1	0	0	0	8
9	0	1	1	1	7
10	0	1	1	0	6
11	0	1	0	1	5
12	0	1	0	0	4
13	0	0	1	1	3
14	0	0	1	0	2
15	0	0	0	1	1
16	0	0	0	0	0 (RESET)

TABLE IV: Characterstic Table for a Ripple Down Counter Circuit (Refer Fig. 4)

V. DISCUSSION & CONCLUSION

In this experiment, we have constructed and studied counter circuits using JK flip-flops. We discussed asynchronous or ripple counters and how the concept of frequency division is used to count binary numbers. We then implemented this logic in building and testing MOD-16 (4-bit) ripple up and ripple down circuits. We also were able to build a MOD-N ($N = 12$ in our case) ripple up circuit using an additional 4 input NAND gate.

Furthermore, we discussed the working and construction of ring counters along with their application and disadvantages, including the use of modified ring counter circuit to fix its problems.

VI. PRECAUTIONS

1. The logic states of the J, K inputs must not be allowed to change when clock is high.
2. For the ring counter preset the first flip-flop to give 1 at its normal output before applying pulse.
3. Watch out for any loose connections.

VII. APPLICATIONS

Counter circuits have various applications. They are used to measure the frequency of a signal by counting the no of cycles in a particular given time period, to generate timing signals like pulse-width modulated (PWM) signals, to perform binary arithmetic operations, data stor-

age and in digital signal processing for filtering and signal analysis. These signals are commonly used in power electronics to control the speed of motors and regulate the brightness of LEDs.

The binary sequence generated by the ring counters can be used for various applications, such as sequencing, pattern generation, and control operations.

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[1] SPS, *Study of Counter Circuits*, NISER (2023).

[2] P. Horowitz and W. Hill, *The art of electronics* (Cambridge University Press, 2015).