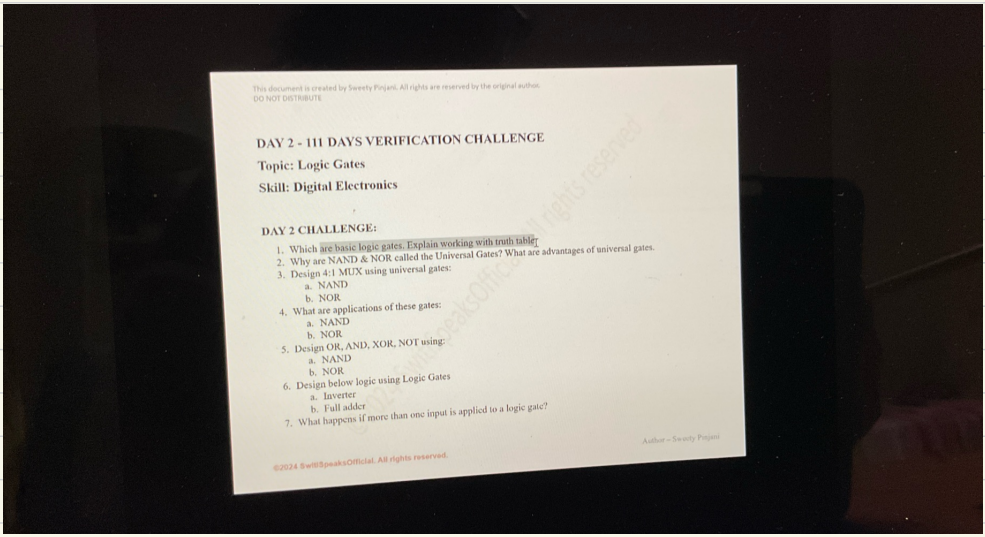

DAY 2 - 111 DAYS VERIFICATION CHALLENGE

Topic: Logic Gates

Skill: Digital Electronics

DAY 2 CHALLENGE:

1. Which are basic logic gates. Explain working with truth table.
2. Why are NAND & NOR called the Universal Gates? What are advantages of universal gates.
3. Design 4:1 MUX using universal gates:
   a. NAND
   b. NOR
4. What are applications of these gates:
   a. NAND
   b. NOR
5. Design OR, AND, XOR, NOT using:
   a. NAND
   b. NOR
6. Design below logic using Logic Gates
   a. Inverter
   b. Full adder
7. What happens if more than one input is applied to a logic gate?

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Day 2

2nd Sept 2024

A1) Basic logic gates

(a) AND

A	B	out
0	0	0
0	1	0
1	0	0
1	1	1

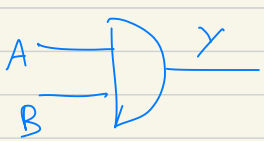
(b) OR

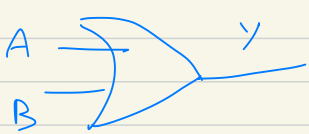
A	B	out
0	0	0
0	1	1
1	0	1
1	1	1

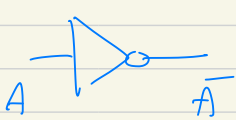
(c) NOT

A	out
0	1
1	0

These are called basic gates as they make the building blocks of digital electronics.







A2) NAND & NOR are called universal gates because using only NAND or NOR all the gates can be implemented. Any circuit can be implemented from those as well

The advantage of universal gates?

The main advantage is the number of transistors used. The no. of tx used is more in case of OR & AND gates. ∵ of the inverting nature of the gates.

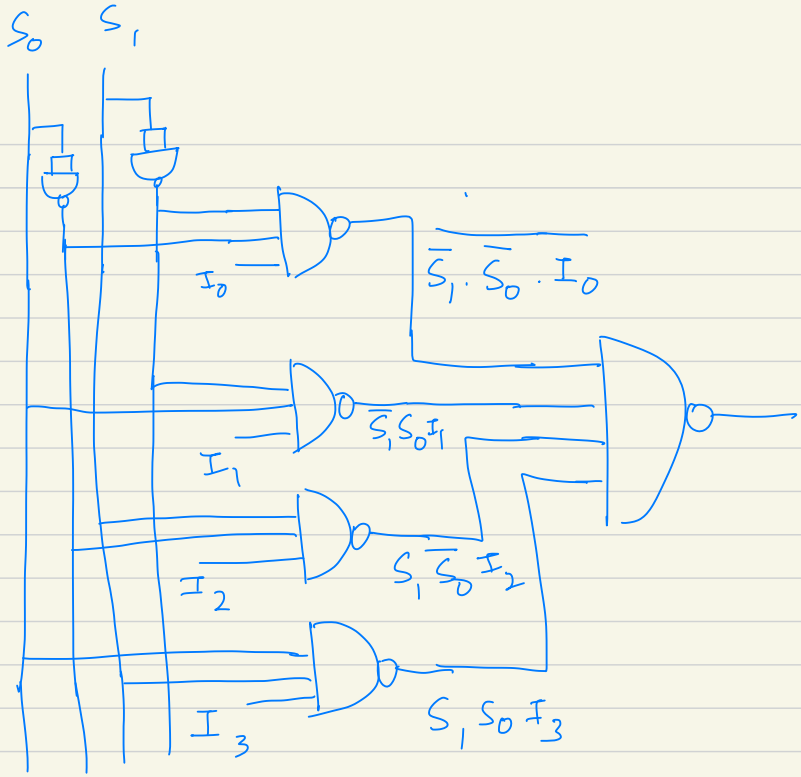
A3) 4:1 Mux using NAND

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$Y = \overline{S_1} \cdot \overline{S_0} I_0 + \overline{S_1} \cdot S_0 I_1 + S_1 \cdot \overline{S_0} I_2 + S_1 \cdot S_0 \cdot I_3$$

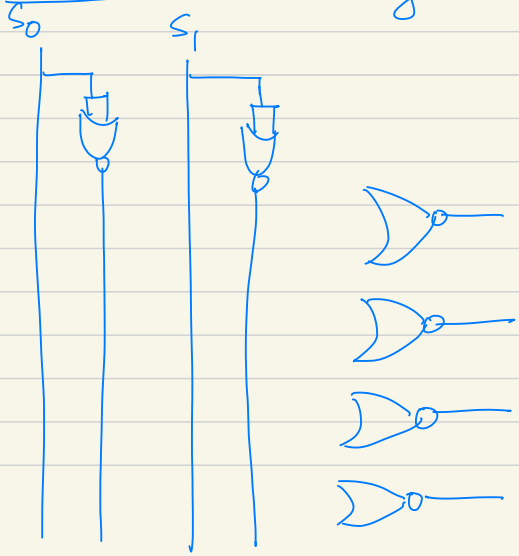
(A = $\overline{S_1} \cdot \overline{S_0} I_0$, B = $\overline{S_1} \cdot S_0 I_1$, C = $S_1 \cdot \overline{S_0} I_2$, D = $S_1 \cdot S_0 \cdot I_3$)

$$= \overline{A + B + C + D} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$$



4 : 1 Mux using NAND gates only

4 : 1 Mux using NOR gates only



S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

A B C

$$Y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

D

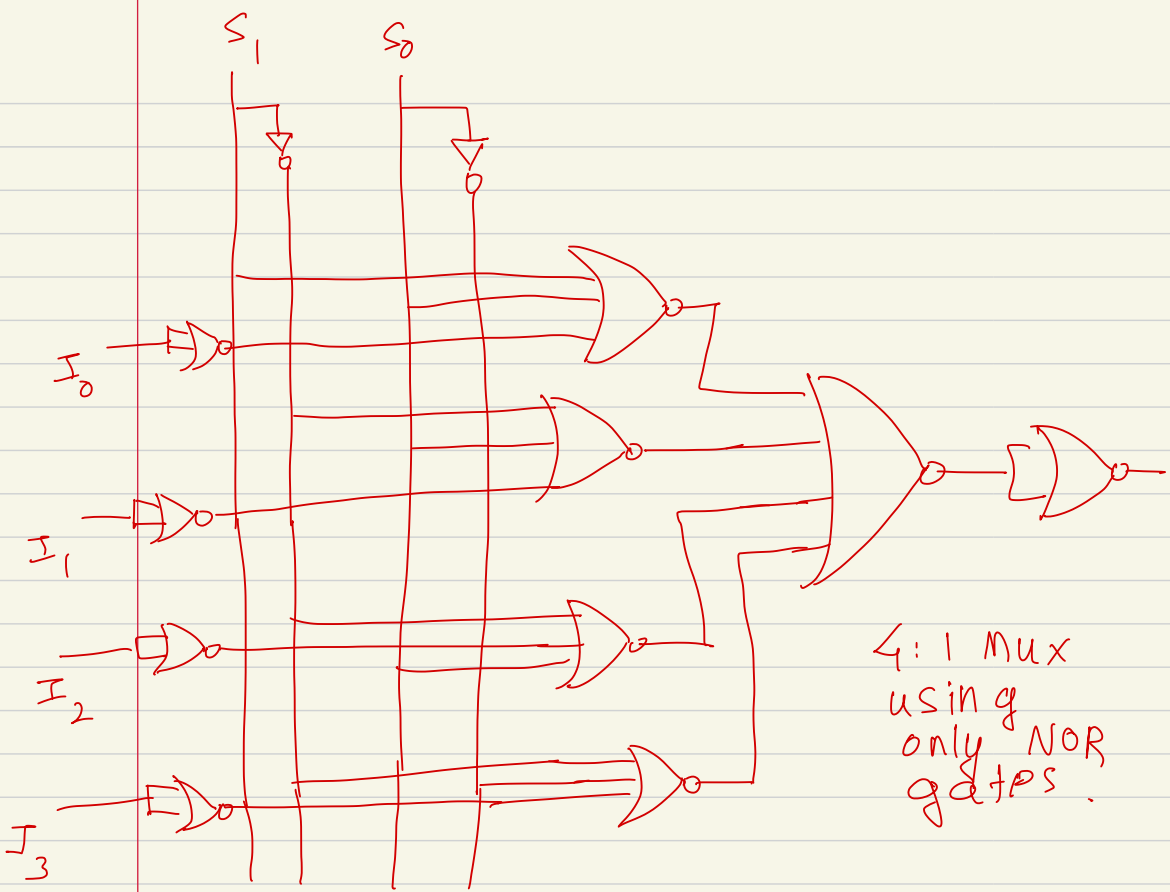
$$\overline{\bar{S}_1 \bar{S}_0 I_0} = \overline{\bar{S}_1 + \bar{S}_0 + \bar{I}_0} = S_1 + S_0 + \bar{I}_0$$

$$= \overline{\overline{S_1 \bar{S}_0 I_0} + \overline{\bar{S}_1 S_0 I_1} + \overline{S_1 \bar{S}_0 I_2} + \overline{S_1 S_0 I_3}}$$

$$\left(\text{or } \overline{A \cdot B \cdot C \cdot D} = \bar{A} + \bar{B} + \bar{C} + \bar{D} \right)$$

$$= \overline{\overline{S_1 + \bar{S}_0 + \bar{I}_0} + \left(\overline{\bar{S}_1 + \bar{S}_0 + \bar{I}_1}\right) + \left(\overline{\bar{S}_1 + S_0 + \bar{I}_2}\right) + \left(\overline{\bar{S}_1 + \bar{S}_0 + \bar{I}_3}\right)}$$

$$= \left(\overline{S_1 + S_0 + \bar{I}_0}\right) + \left(\overline{S_1 + \bar{S}_0 + \bar{I}_1}\right) + \left(\overline{\bar{S}_1 + S_0 + \bar{I}_2}\right) + \left(\overline{\bar{S}_1 + \bar{S}_0 + \bar{I}_3}\right)$$



4:1 Mux using only NOR gates.