Logique Séquentielle - fonction « mémoire »

1. Introduction

<u>Logique combinatoire</u>: Un système logique est dit combinatoire si à tout instant, le résultat logique en sortie ne dépend que de l'état de ses entrées. L'élément de base d'un système combinatoire est la porte logique.

<u>Logique séquentielle</u>: Un système est dit séquentiel si à une même combinaison des variables d'entrée peut correspondre plusieurs combinaisons différentes des variables de sortie.

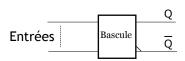
La combinaison des variables de sortie dépend des entrées mais également de l'état antérieur des variables de sortie ou d'un signal de synchronisation.

Autrement dit dans un système séquentiel, la sortie à un instant donné N dépend des entrées à l'instant N mais aussi des entrées et sorties aux instants précédents (instant N-1).

C'est ce que l'on appelle « l'effet MEMOIRE »

L'élément de base d'un système séquentiel est la bascule (bistable)

Fonction mémoire - la bascule :



Les sorties:

La sortie Q est la sortie « normale » de la bascule, tandis que la sortie \overline{Q} est la sortie complémentaire.

Remarque: lorsqu'on fait référence à l'état d'une bascule, on considère l'état de la sortie « normale » Q.

Changement d'état :

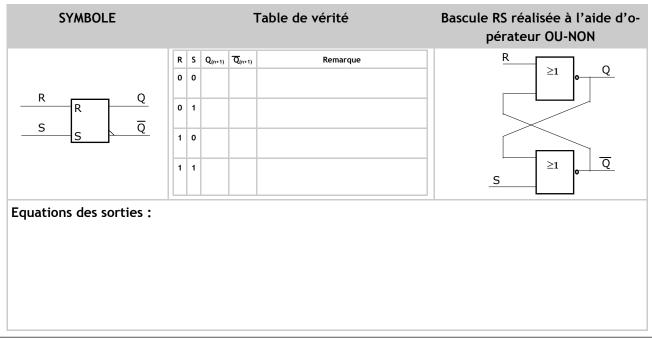
Les entrées sont utilisées pour commuter (« faire basculer ») les sorties. Une entrée a seulement besoin de l'excitation d'une impulsion pour changer l'état des sorties de la bascule.

Après la disparition de cette impulsion, les sorties conserve leur valeur.

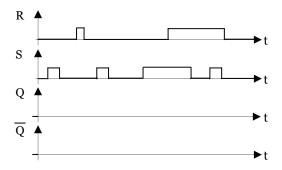
C'est cela qui fait de la bascule un dispositif de mémorisation.

2. Les bascules

2.1 La bascule R S



Exercice : Compléter les chronogrammes suivants (appliqués à une bascule RS) :

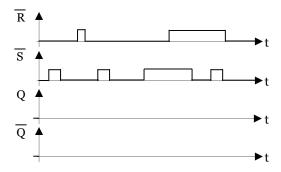


2.2 La bascule R S

Nb : La bascule \overline{R} \overline{S} est la sœur jumelle de la bascule RS.



Exercice : Compléter les chronogrammes suivants (appliqués à une bascule \overline{RS}) :



2.3 La bascule R S synchrone (bascule RSH ou RST)

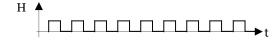
Un circuit numérique peut fonctionner de 2 façons :

- mode asynchrone : sa (ou ses) sortie(s) change(nt) d'état à tout moment quand une (ou plusieurs) entrées changent d'état.
- mode synchrone : le moment exact, où la sortie change d'état est commandé par un signal de synchronisation temporelle que l'on appelle couramment signal d'horloge (H ou C [clock])

Lorsque qu'un circuit fonctionne en mode synchrone, ses sorties ne changent d'état qu'aux instants de transitions du signal d'horloge. Ces transitions sont appelés des fronts montant ou front descendant.

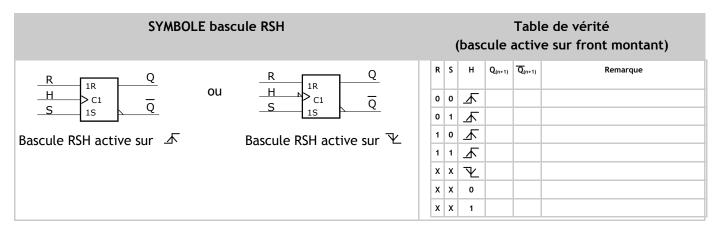
Intérêt: En distribuant ce signal d'horloge à l'ensemble des fonctions logiques réalisant un système, les sorties de ces fonctions changent d'état toutes en même temps lorsque le signal d'horloge effectue une transition.

Exemple de signal d'horloge:

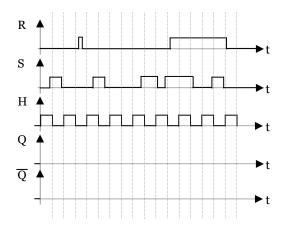


On appelle **front montant** l'instant t ou le signal d'horloge (H) passe de l'état bas à l'état haut. Dans une table de vérité le front montant est symbolisé par le signe suivant :

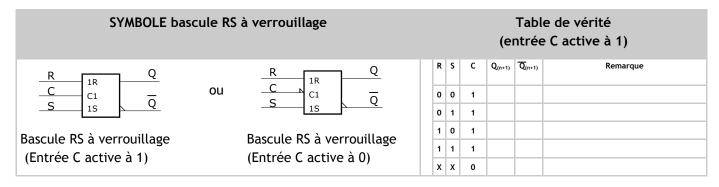
On appelle **front descendant** l'instant t ou le signal d'horloge (H) passe de l'état haut à l'état bas. Dans une table de vérité le front descendant est symbolisé par le signe suivant : \checkmark



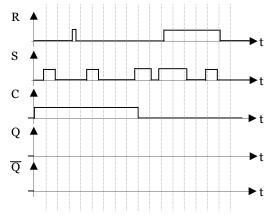
Exercice : Compléter les chronogrammes suivants (appliqués à une bascule RSH active sur front montant) :



2.4 La bascule R S à verrouillage (LATCH)



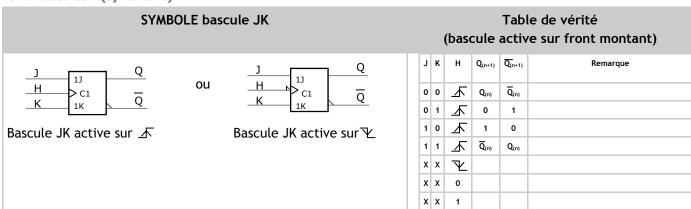
Exercice : Compléter les chronogrammes suivants (appliqués à une bascule RSC active sur niveau 1) :



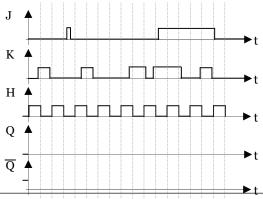
2.5 Exemple d'application des bascules RS

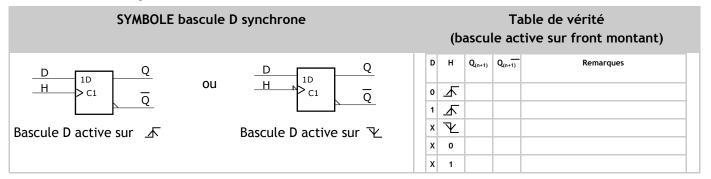
Système Anti-Rebond (voir TD).

2.6 La bascule JK (synchrone)

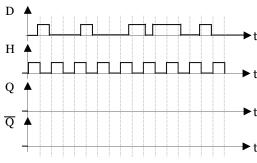


Exercice: Compléter les chronogrammes ci-contre (appliqués à une bascule JK active sur front montant):

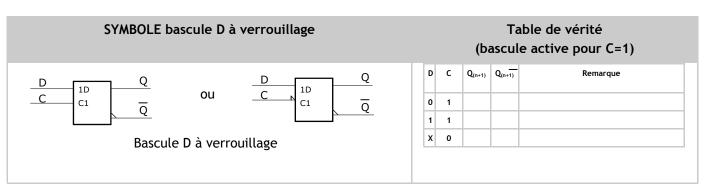




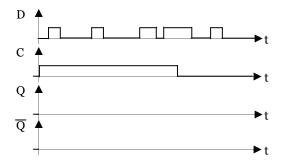
Exercice : Compléter les chronogrammes suivants (appliqués à une bascule D active sur front montant) :



2.7 La bascule D à verrouillage (LATCH)



Exercice: Compléter les chronogrammes suivants (appliqués à une bascule D, C actif à 1):



3. Caractéristiques communes aux bascules

3.1 mode de fonctionnement des entrées

Comme nous l'avons vu précédemment les entrées peuvent fonctionner dans un des deux modes de fonctionnement :

- mode synchrone : les entrées synchrone ne sont prises en compte que sur le front montant du signal d'horloge. Elles ont un fonctionnement synchrone par rapport au signal d'horloge.
- mode asynchrone : les entrées asynchrone (ou dites prioritaires) ont un effet immédiat sur l'état de la bascule.

Initialisation d'une bascule : Pour le fonctionnement d'un système, il est souvent nécessaire que les bascules soient initialisées, c'est à dire que leur sortie Q soit mise à « 1 » ou à « 0 » et ce indépendamment du signal d'horloge. D'où, deux entrées supplémentaires asynchrones, présentes sur pratiquement tous les circuits intégrés :

Preset : mise à 1 de la sortie Q (broche appelée aussi RAU ou SET) **Clear :** mise à 0 de la sortie Q. (broche appelée aussi RAZ ou CLR)

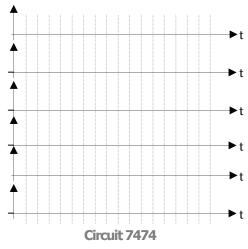
Ces deux entrées asynchrones sont désignées entrées d'initialisation ou de forçage.

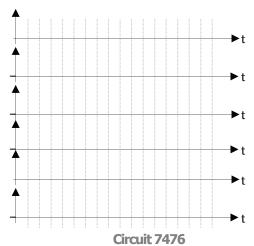
Remarque: La plupart des bascules ont au moins une entrée de type asynchrone (pour fixer la valeur des sorties à la mise sous tension). Dans certains montages, elles sont inutiles: on les maintient alors en permanence au niveau logique inactif.

Exercice 1 : établir les tables de vérité des fonctions logiques 7474 et 7476

SYMBOLE du circuit référence 7474	Table de vérité du circuit 7474
SYMBOLE du circuit référence 7476	Table de vérité du circuit 7476

Exercice 2: Tracer les chronogrammes de fonctionnement correspondants aux fonctions logiques 7474 et 7476 (voir exercice 1)





3.2 Temps de propagation

Comme tout circuit logique, on peut définir deux temps de propagation T_{PHL} et T_{PLH} (c.f TP sur la technologie des fonctions logiques). Ces temps de propagation affecte toutes les entrées des bascules (horloge, fonction SET et RESET, entrées asynchrones...)

Rappel: Le temps de propagation est le retard entre le moment où le signal est appliqué et le moment où ce dernier provoque un changement en sortie. Il est mesuré aux points à mi-hauteur du signaux (50 %).

Les retards de propagation affectent la réponse à toutes les entrées (horloge, entrée asynchrone). Ils peuvent varier entre quelques ns et quelques ms.

Exemple sur doc TI : Pour la bascule 74HC74, on définit Tp typ $\overline{PRE}/\overline{CLR} \rightarrow Q/\overline{Q} = 20$ ns

3.4 Largeur minimum de l'impulsion d'horloge

On définit :

 $t_{W \, clock}$: durée minimale pendant laquelle l'horloge doit demeurer à 1 avant de repasser à 0. exemple : $t_{W \, Clock \, High}$ = 20 ns

3.5 Durée minimum pendant laquelle une entrée asynchrone doit être active :

Si on veut effectivement forcer la bascule à 0 ou 1, il faut que l'impulsion sur l'entrée asynchrone dure suffisamment longtemps dans son état actif.

Exemple: $t_{W \text{ Preset Low}} = 25 \text{ ns}$; $t_{W \text{ Clear Low}} = 25 \text{ ns}$.

NB: - Ces entrées sont actives à l'état bas.

- Si on laisse PRESET plus de 25 ns à 0, on est sur que la sortie passera à 1 (sans ambiguïté).

Deux exigences de synchronisation doivent être respectées pour qu'une bascule synchrone réponde correctement à ses entrées de commande lorsque arrive un front déclencheur sur l'horloge.

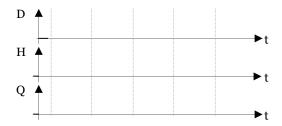
3.6 Temps de stabilisation (ou temps d'établissement min) : noté t_{SU} (Setup).

Il s'agit de l'intervalle qui précède immédiatement le front déclencheur du signal d'horloge, pendant lequel l'entrée de donnée doit être gardée au niveau approprié. Si on ne respecte pas ce temps, il n'est pas garanti que la bascule répondra correctement à l'arrivée du front. Les fabricants spécifient généralement la durée de stabilisation minimale admissible.

3.7 Temps de maintien : noté t_M ou T_H (Hold).

Il s'agit de l'intervalle qui suit immédiatement le front déclencheur du signal d'horloge pendant lequel l'entrée de donnée doit être gardée au niveau approprié. Si on ne respecte pas ce temps, la bascule ne sera pas déclenchée correctement. Les fabricants spécifient généralement la durée minimale acceptable. Généralement le temps de maintien est suffisamment court. La sortie d'une bascule passe donc dans l'état imposé par les niveaux logiques actifs sur ses entrées de commande synchrones juste avant la transition du signal d'horloge.

En résumé, l'entrée de commande doit être stable, c'est à dire inchangée, pendant une durée égale à : TS + TH.



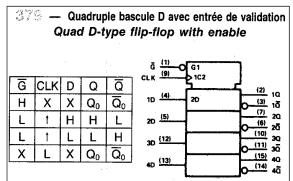
3.8 Fréquence maximale du signal d'horloge:

Fréquence la plus élevée que peut avoir le signal d'horloge et qui assure un déclenchement fiable de la bascule. La fréquence Fmax varie d'une bascule à l'autre et même entre bascules avec le même numéro de série. Elle est fonction du temps de transition.

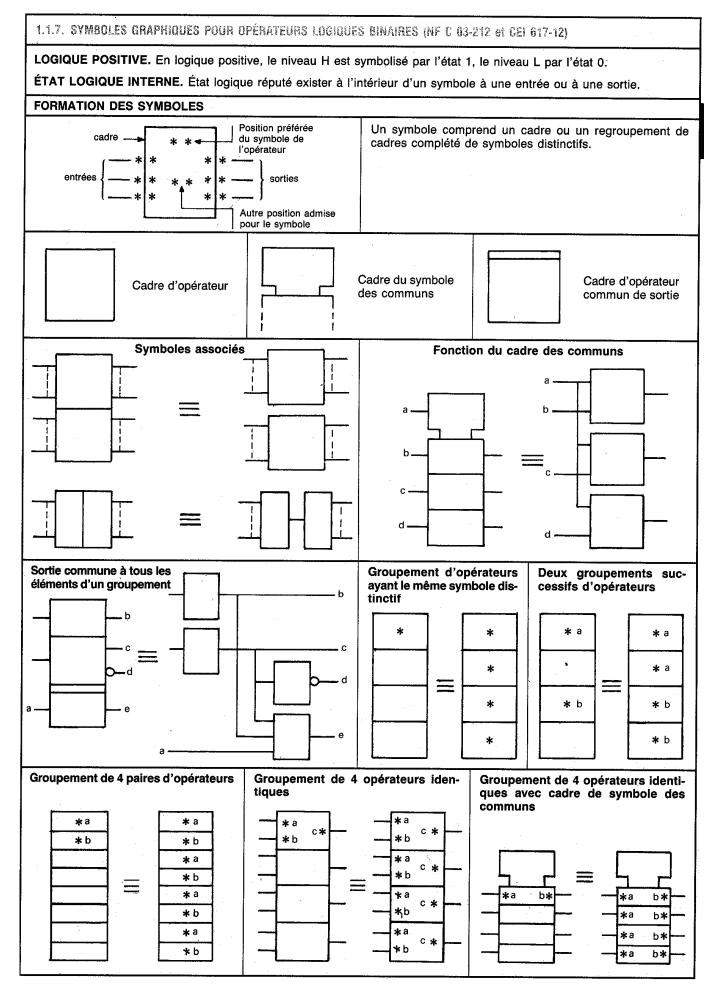
4. Symbolisation des opérateurs logiques - (Norme Européenne NF-C 03-212 et CEI 617-12)

Une norme Européenne (et Française) définit la façon de représenter la symbolique associée aux opérateurs logiques. C.F annexe 1 à ce cours.

Exemple : Circuit 74379 - Cadre des communs d'entrée : il est utilisé chaque fois qu'un circuit intégré a des entrées communes avec plus d'un élément de la puce.



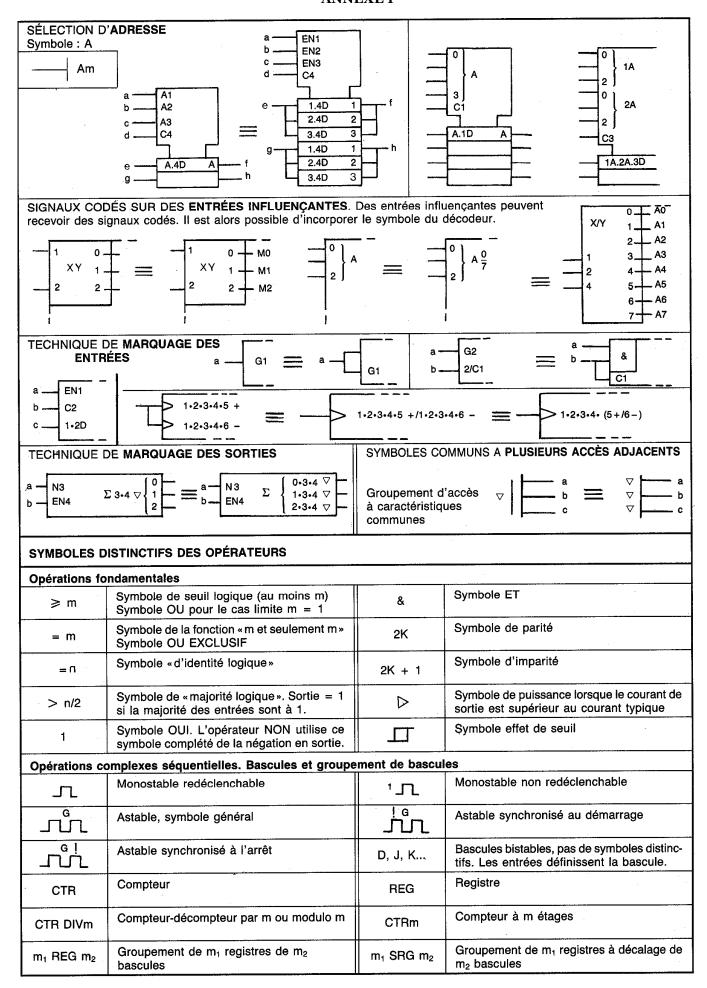
- **G1** : entrée qui lorsqu'elle est valide (ici état bas) va permettre la validation de toutes les entrées précédées de 1.
- 1C2 : horloge sur front montant. Elle influence toutes les entrées précédées de 2 (toutes les bascules D).
- 2D: entrée de bascule D (influencée par horloge 1C2).



ANNEXE 1

<u>-</u> d	Négation logique à l'entrée État interne 1 État externe 0		Entrée dynamique État interne = 1 sur front montant
þ—	Négation logique à la sortie État externe 0 État interne 1		État dynamique avec négation logique État interne = 1 sur front descendant
	Connexion interne	7	Symbole d'effet différé sur une sortie
D	Sortie amplifiée		Entrée à seuil Entrée avec hystérésis
	Sortie à circuit ouvert (symbole général)	\Diamond	Sortie à circuit ouvert de type H Par exemple NPN émetteur ouvert
	Sortie à collecteur ouvert (C.O.) NPN collecteur ouvert	∇	Sortie 3 états. État haute impédance Entrée de commande notée EN
E	Entrée d'expansion. A connecter à la sortie d'un circuit expanseur	E	Sortie d'un expanseur. A connecter à l'entrée d'un autre circuit
EN	Entrée de validation. L'état interne 0 de l'e Cette entrée est à effet prépondérant de dé		
D	Entrée D d'une bascule. L'état logique interne de cette entrée est mis en mémoire.	J	Entrée J d'une bascule
— к	Entrée K d'une bascule	—— Р	Entrée R. Entrée à état interne 1,0 mémo risé par l'opérateur
s	Entrée S. Entrée à état interne 1,1 mémorisé par l'opérateur	т т	Entrée T d'une bascule. Chaque fois que T = 1, changement d'état de la bascule.
——— m	Entrée de décalage d'un registre à droite. Décalage de m positions	+ m	Entrée de comptage. Incrémente de m chaque impulsion d'entrée.
— m	Entrée de décalage d'un registre à gau- che. Décalage de m positions	m	Entrée de décomptage. Décrémente de r à chaque impulsion d'entrée.
?	Entrée d'interrogation d'une mémoire associative	!	Sortie de comparaison d'une mémoir associative
— Р	Entrée opérande, entrée P figurée. A cette entrée est affecté un opérande.		Entrée PLUS GRAND QUE d'un compara teur numérique
 <	Entrée PLUS PETIT QUE d'un compara- teur numérique	<u>**</u>	Entrée d'ÉGALITÉ d'un comparateu numérique
cı	Entrée d'une retenue dans un opérateur monté en cascade	—— cg	Entrée de la retenue générée dans un opérateur
ж	Sortie de la retenue générée par un opé- rateur en vue d'un calcul anticipé	со	Sortie de la retenue d'un opérateur
CP	Sortie de la retenue propagée dans un opérateur	CT = m	Entrée imposant un contenu Si m = 0, utiliser R
T*	Sortie indiquant que l'opérateur a atteint la valeur indiquée		Entrée en mode fixe, en permanence l'état interne 1
	Accès bilatéral figuré sur le côté gauche. Peut figurer sur le côté droit.	"1"	Sortie de mode fixe en permanence à l'éta interne 1
**	Accès bilatéral avec notation de dépendance	**	Accès bilatéral figuré sur le côté droit ave notation de dépendance
	Entrée concernée par des signaux analo- giques (si risque de confusion)	#	Entrée concernée par des signaux numé riques (s'il y a risque de confusion)
-	Accès sans transmission d'information (Branchement extérieur d'un composant R,C)	m1 m2	Symbole de groupement numérique pou accès à plusieurs bits en parallèle
	Symboles de groupement de liaisons en entrée ou en sortie. Ils indiquent que plu- sieurs signaux sont nécessaires pour obte- nir une information logique.	*	m présentés dans l'ordre des poids crois sants peuvent être remplacés par les valeur décimales. L'astérisque peut représenter u nombre concernant une opération P,Q, so un chargement ou une notation d dépendance.

NOTATION DE DÉPENDANCE La notation de dépendance symbolise les relations entre accès, entrées et sorties, sans figurer le détail des opérateurs et interconnexions impliqués. Réservée aux symboles d'opérateurs complexes, la notation de dépendance ne doit pas être utilisée 0 en lieu et place des symboles d'opérateurs combinatoires. Les conventions régissant la notation de dépendance font appel aux notions d'accès influençants et 2 d'accès influencés. La notation de dépendance est réalisée en marquant : l'accès influençant par un symbole littéral suivi d'un numéro d'identification; 1D — chacun des accès qu'il influence par le même numéro d'identification (représenté par m dans ce chapitre). DÉPENDANCE : ET Symbole: G Gm G1 7 Gm DÉPENDANCE : OU Symbole: V Vm ≥1 ≥1 Vm DÉPENDANCE DE NÉGATION b Symbole: N Nm Nm DÉPENDANCE D'INTERCONNEXION Symbole: Z G1 Zm 2 Zm DÉPENDANCE DE COMMANDE Symbole: C C1 G1 S Cm 1C2 1C2 D 2D 20 Cm DÉPENDANCE DE MISE A 1 b С d Symbole: S С d S DÉPENDANCE DE 0 0 Sm 0 0 MISE A 0 0 0 1 1 0 1 1 Symbole: R R1 0 1 1 0 0 1 0 Rm 1 0 0 1 * inchangé DÉPENDANCE DE VALIDATION Symbole: EN L'effet de cette entrée sur les sorties qu'elle influence est le même que celui d'une entrée EN. L'effet **ENm** de cette entrée sur les entrées qu'elle influence est le même que celui d'une entrée G. SÉLECTION DE MODE Pour les opérateurs complexes, un M1 M Symbole: M tableau peut préciser le mode de fonc-C1 1C2 tionnement. Mn 2D 10 М fonction MO Bascule D statique Mn 0.}M Bascule D dynamique



ANNEXE 1

Opérations co	omplexes séquentielles. Mémoires		
MEM m ₁ ×m ₂	Mémoire de m ₁ section de m ₂ bit, en cas général	CAM	Mémoire vive associative adressable par son contenu
CIR	Mémoire vive à recirculation	EPROM	Mémoire effaçable et reprogrammable à lec- ture seule
EEPROM	Mémoire effaçable électriquement et repro- grammable à lecture seule	FIFO	Mémoire vive du type « premier entré premier sorti »
LIFO	Mémoire vive du type «dernier entré premier sorti»	PROM	Mémoire programmable à lecture seule
RAM	Mémoire vive à accès aléatoire	ROM	Mémoire à lecture seule ou mémoire morte
Opérations co	omplexes combinatoires. Multiplexeurs/dém	ultiplexeurs	
DMX	Démultiplexeur	MULDEX	Multiplexeur-démultiplexeur
мих	Multiplexeur	-	
Opérations co	omplexes combinatoires. Convertisseurs		
X/Y	Symbole général. Les symboles qui suivent précisent le type.	BCD	Décimal codé binaire
BIN	Binaire	CAR	Coordonnées cartésiennes
DPY	Afficheur	ECL	Niveau pour circuits logiques ECL
ЕХЗ	Excès de 3	EX3GRAY	Excès de 3 code GRAY
GRAY	Code GRAY	HEX	Code hexadécimal
HPRI	Codeur de priorité	MOS	Niveau pour circuits logiques MOS
POL	Coordonnées polaires	mSEG	Code à m segments
TTL	Niveau pour circuits logiques TTL	Λ	Analogique
DEC	Décimal	#	Numérique
Opérations co	emplexes combinatoires. Opérateurs mathé	natiques	
ALU	Unité arithmétique et logique	CPG	Générateur de retenue anticipée
P-Q	Soustracteur	Σ	Additionneur
π	Multiplicateur	P Q	Diviseur
Opérateurs à	retard		
t1 t2	t ₁ et t ₂ sont à remplacer par les retards intro	duits sur les fro	nts des impulsions.
OPÉRATEURS	LOGIQUES COMPLEXES - ACCÈS A PLUS	IEURS FONCTION	DNS
$ eg \Phi eg $	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		RD/\overline{W} $=$ D BUS
			D BUS ♥ = D BUS ♥

רומווכמומ	sélection adresse de colonne	validation du boîtier	entrée/sortie d'horloge	validation d'horloge	sélection du boîtier	prêt à émettre	demande de DMA acceptée	activation du bus de données	bus de donnees	detection de porteuse	acces direct de memoire	validation des données	demande de DMA	demande pour émettre retardée	poste de données prêt	terminal de données prêt	validation, utilisable comme suffixe	erreur	faute	arrêt	reconnaissance de maintien	maintien	demande de maintien	interruption	reconnaissance d'interruption	validation d'interruption	demande d'interruption	validation de mémoire	remise à zéro générale	memoire prête	interruption non masquable	absence de bit de parite	nombre de bits de stop	remise à zéro	récontion on course de la contraction de la cont	sélection d'adresse de rangée	lecture	lecture/écriture	données recues disponibles	validation données recues	prêt	erreur de trame réception	chevauchement de mots réception	erreur parité réception	selection de registre	mot d etat reception valide	debut de message reception	demaide pour emettre	horloge de réception de données	début	échantillonnage, utilisable comme suffixe	transmission en cours valide	tampon émission vide	fin de message émission	temportsation mot d'émission valido	commande du 3º état	début de message émission	sortie série émission	horloge d'émission des données	adresse memoire valide	adiesse peripirerique valide écriture	attente	validation écriture	horloge externe du microprocesseur
Similifier	column address select	chip enable	clock	clock enable	chip select	clear to send	UMA acknowledge	data bus enable	data bus	direct moment process	direct merilory access	data port enable	Divid request	delayed request to send	data set ready	data terminal ready	enable	error	fault	halt	hold acknowledge	plou	hold resquest	interrupt	interrupt acknowledge	Interrupt enable	Interrupt request	memory enable (HAM)	master reset	memory ready	non maskable interrupt	no parity bit	A peripheral (B.C)	reset	receiver active	row address select	read	read/write	receiver data available	received data enable	ready	receiver framing error	receiver over run	receiver parity error	register select	receiver status available	revelvel start of message	receiver serial (SID)	receiver clock	start	strobe		transmitter buffer empty	transmitter end of message	transmitter status available	three-state control	transmitter start of message	transmitter serial (SOD)	transmitter clock	valid menory address	write	wait signal	write enable	O, Xtal, extal clock
	CAS	CEN	OLK I	CLKEN	နှင့်	200	DACK		200	2 5			2 6		7 K	ı S	2	ERR	7	HAL	HLDA	HOLD	Ø !	- I	A I	N C	2 1		Z .	MAC -		000	0 P		PACT	BAS	B	RD/W	RDA	RDEN	RDY	HFE.	ROR	T 0	ָ פַּ	V C	RTS W	X	RXCLK	START	STB	TACT	E C		TSA AST	TSC	TSOM	×	Y Y CLK	VPA	*	WAIT	WEN.	7 Y
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