Corrigé de l'examen Architecture des Ordinateurs

Session Rattrapage

Exercice 1

1. Table de Verité

b_0	a_0	C	D	S_0
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Table de Karnaugh

CD \ a_0b_0	00	01	11	10
00				
01			1	1
11	1	1	1	1
10		1	1	

$S_0 = Cb_0 + Da_0 + CD$

Avec des portes NAND

$\overline{S_0} = S_0 = \overline{Cb_0 + Da_0 + CD} = \overline{Cb_0} \cdot \overline{Da_0} \cdot \overline{CD}$

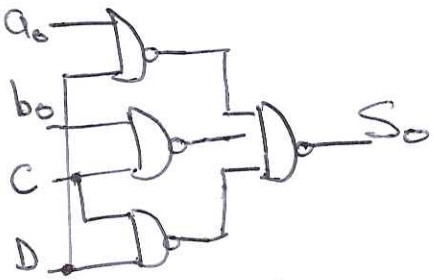


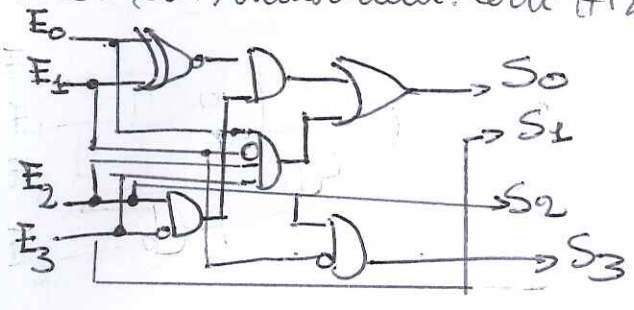
Schéma logique

Exercice 2

Déim	Code de Gray Non pondéré				Code Aiken			
					2	4	2	1
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	1	0	0	1	0
3	0	0	1	0	0	0	1	1
4	0	1	1	0	0	1	0	0
5	0	1	1	1	0	1	0	1
6	0	1	0	1	1	1	0	0
7	0	1	0	0	1	1	0	1
8	1	1	0	0	1	1	1	0
9	1	1	0	1	1	1	1	1
	E_3	E_2	E_1	E_0	S_3	S_2	S_1	S_0

Entrées du transcodeur : Code de Gray

Sorties du transcodeur : Code Aiken



Equations booléennes des sorties

$S_0 = \overline{E_3}E_2E_1E_0 + E_3\overline{E_2}\,\overline{E_1}\,\overline{E_0} + E_3E_2\overline{E_1}E_0$

$S_0 = \overline{E_3}E_2(\overline{E_1}\,\overline{E_0} + E_1E_0) + E_3E_2\overline{E_1}E_0$

$S_0 = \overline{E_3}E_2\overline{(E_1 \oplus E_0)} + E_3E_2\overline{E_1}E_0$

ou

$S_0 = E_2\overline{E_1}(\overline{E_3}\,\overline{E_0} + E_3E_0) + \overline{E_3}E_2E_1E_0$

$S_0 = E_2\overline{E_1}\overline{(E_0 \oplus E_3)} + \overline{E_3}E_2\overline{E_1}E_0$

$S_1 = \overline{E_3}$

$S_2 = \overline{E_2}$

$S_3 = \overline{E_3}E_2\overline{E_1}E_0 + \overline{E_3}E_2E_1\overline{E_0} + E_3\overline{E_2}\,\overline{E_1}\,\overline{E_0} + E_3\overline{E_2}\,\overline{E_1}E_0 + E_3E_2\overline{E_1}\,\overline{E_0}$

$= \overline{E_3}E_2\overline{E_1} + E_3\overline{E_2}\,\overline{E_1} = \overline{E_1}E_2$

$S_3 = \overline{E_1}E_2$