AGNUS AND BUDDY CARD
3 MB CHIP RAM CARD
FOR SMD2000

By Gazzmaniac

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DISCLAIMER:
This is an experimental hobbyist project which may not work. There are probably design flaws and faults. Constructors will require equipment including soldering and rework, test gear, oscilloscope, CPLD programmer, and advanced soldering, electronics, and troubleshooting skills.

If you choose to construct this project please assume there will be no support available to help you get it working. You are on your own. If you can't get it working or break your Amiga chipset or something else do not blame anyone but yourself. You were warned!

No person or organisation associated with this project accepts any liability or responsibility for damages or injury as a result of someone using this board.

You agree to these terms if you have the board fabricated or you obtain a fabricated board.

That said, remember it is a hobby and the whole point is to enjoy making it and to get satisfaction from having made a unique piece of hardware. Remember to have fun. If you start cracking the shits walk away and finish it another day.

NOTES

Read the readme file!

This is an Agnus board for the SMD2000. It replaces the standard Agnus boards for that project.

This board uses the 8375 Agnus from the A500+/A600 in a bank switching arrangement in order to increase the maximum addressable chip ram.

If you intend to use this card you will also need to build an SMD2000 motherboard and CPU card.

This design is an improvement on the first prototype design, which was built to prove the bank switching arrangement works, to verify the timing arrangements for accessing Amiga registers, and to facilitate writing the first CPLD source code. This specific design has not actually been made, however an almost identical one has, with the only difference being a minor rearrangement of the card to add RP302 & RP303, the pull up resistors on the control lines for each of the switchable RAM banks (in the working prototype these resistors were added by bodging in using TTH resistors). There is no reason why this design will not also work.

Refer to the Readme file for other notes and the Functional Description for a detailed explanation of how this contraption works.

REFERENCES

Agnus Specification Rev C; 20/7/1988
Denise Specification; 1988 (Amigawiki.de version)
Motorola MC68000 microprocessor user manual 9ed; 1993.
A500+ Service Manual; October 1991.
Amiga Hardware Reference Manual 3ed; 1991.
US Patent 4,777,621 (Amiga patent); 11/7/1988.
Paula Dissection, http://forum.6502.org/viewtopic.php?f=4&t=7681

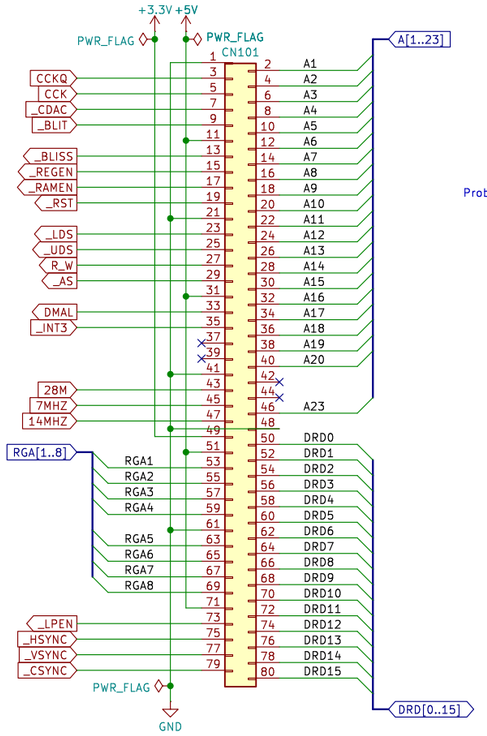
Symbols and footprints for most parts were downloaded from Mouser/Samacsys, and many were modified to make the schematics more readable. Samacsys parts do not require further attribution, however I am doing so anyhow.
Links to datasheets are in the symbol metadata.
Footprints and symbols for generic parts e.g. jumpers/headers use Kicad libraries.

VERSION CONTROL

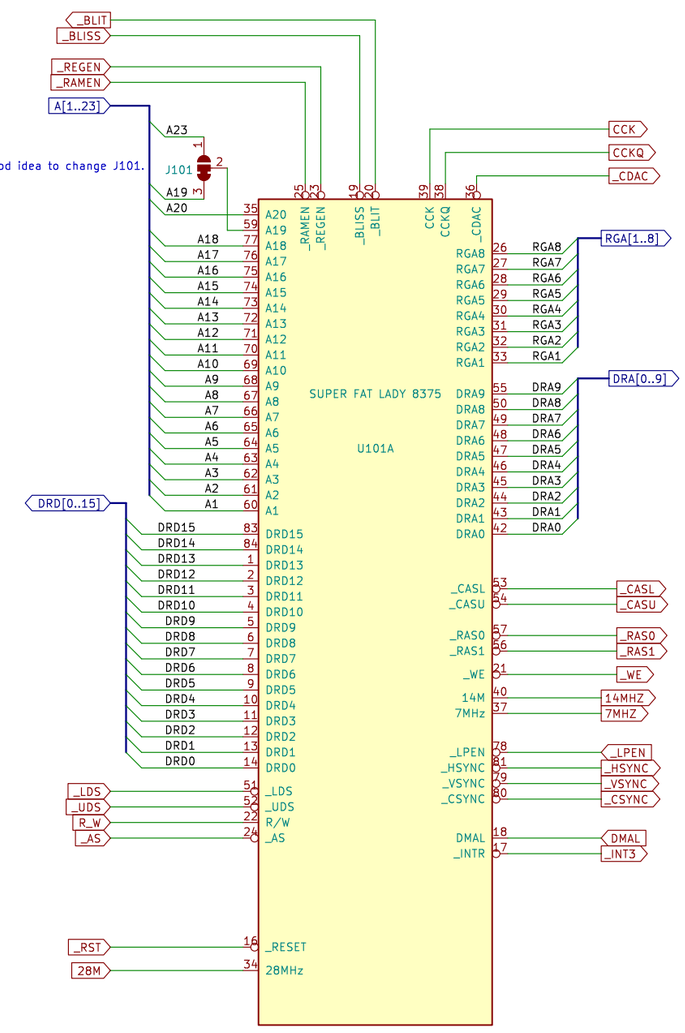
Rev	Description
0	For general release – added pullup resistors
A	Initial design for first prototype (internal)

Sheet: /
File: Bank Switching Agnus Card 8375.kicad_sch
Title: 3 MB BANK SWITCHING CHIP RAM CARD FOR SMD2000
Size: A3 | Date: 2025–06–09 | **Rev: 0**
KiCad E.D.A. 8.0.6 | Id: 1/4

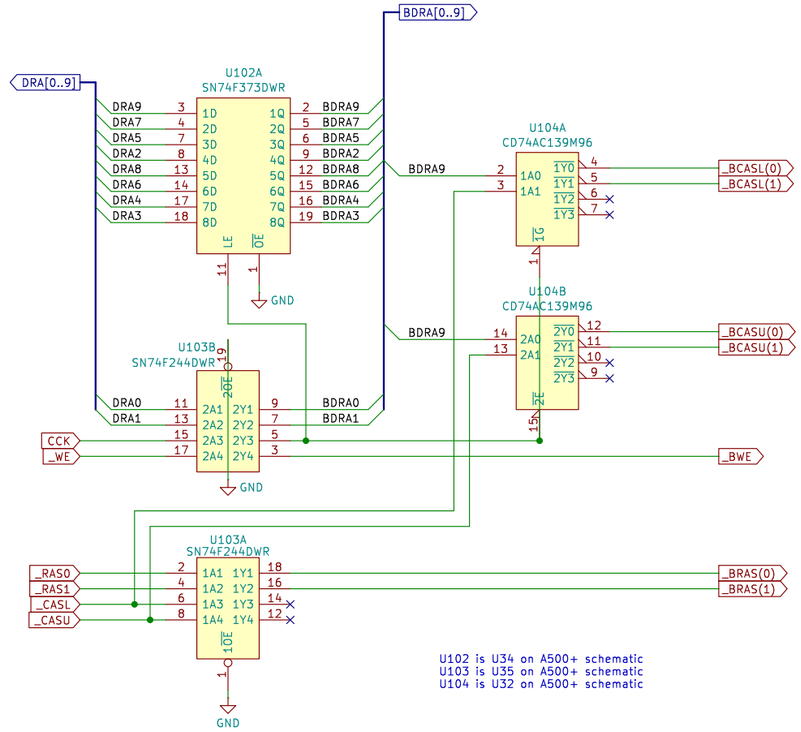
AGNUS CARD CONNECTOR



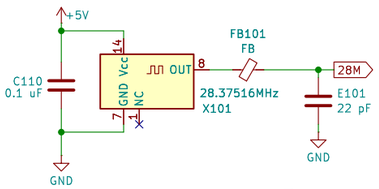
SUPER FAT LADY



RAM CONTROL LOGIC AND ADDRESS BUS BUFFERS



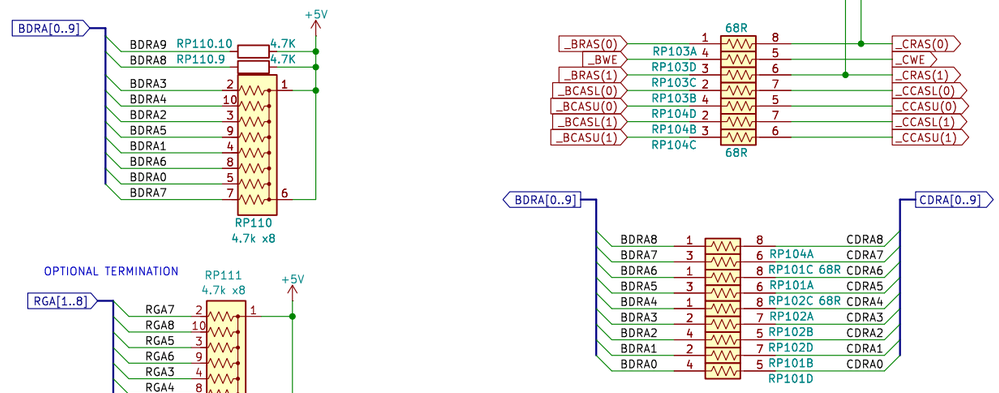
28 MHZ CLOCK



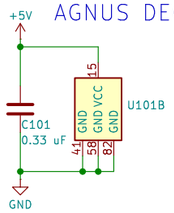
Removed XCLK option.

X101 is X1 on A500+/A2000 schematic
E101 is E666 on A500+ schematic

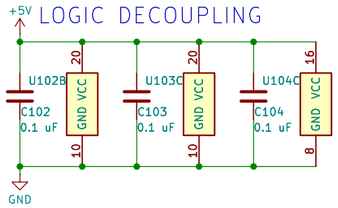
RESISTORS ETC



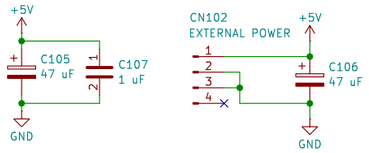
AGNUS DECOUPLING



LOGIC DECOUPLING

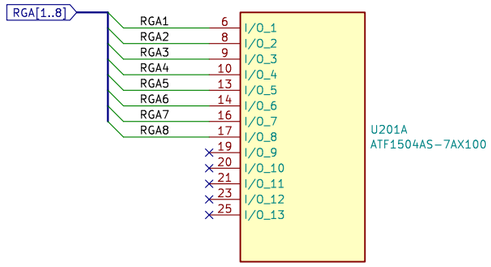


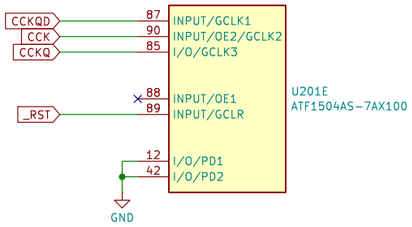
BOARD DECOUPLING

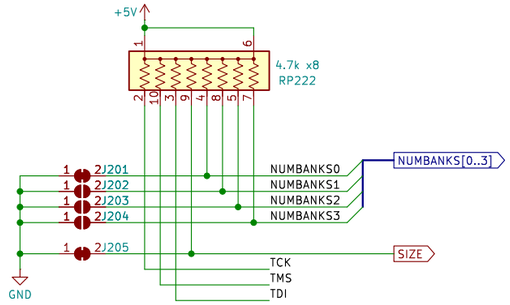


Sheet: /Agnus & Amiga Control Logic/		
File: Page 02 – Agnus.kicad_sch		
Title: 3 MB BANK SWITCHING CHIP RAM CARD FOR SMD2000		
Size: A3	Date: 2025-06-09	**Rev: 0**
KiCad E.D.A. 8.0.6		Id: 2/4

CPLD "BUDDY"



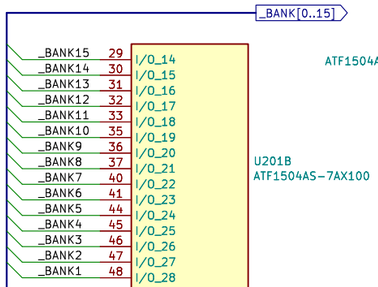


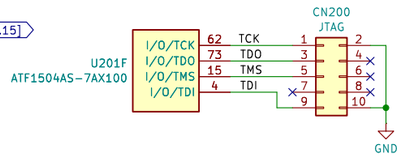


USE J201-J204 TO SPECIFY NUMBER OF BANKS
TAKE NUMBER OF BANKS AND SUBTRACT 1
REPRESENT THIS NUMBER IN BINARY:

NUM BANKS	J2011 (1s)	J202 (2s)	J203 (4s)	J204 (8s)
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1
10	1	0	0	1
11	0	1	0	1
12	1	1	0	1
13	0	0	1	1
14	1	0	1	1
15	0	1	1	1
16	1	1	1	1

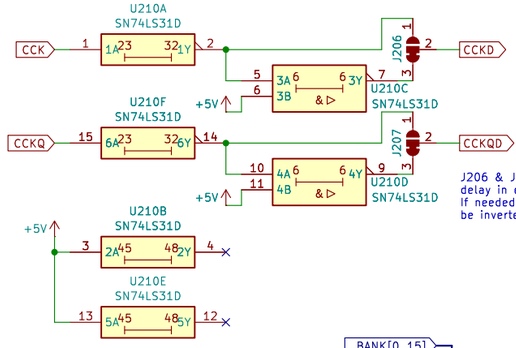
J205 SPECIFIES SIZE OF EXPANSION BANKS
OPEN=512k, CLOSED=1M





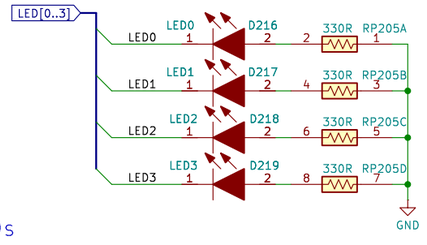
JTAG matches pinout of ByteBlaster
NOTE Pullup Resistors Elsewhere

CLOCK DELAYS

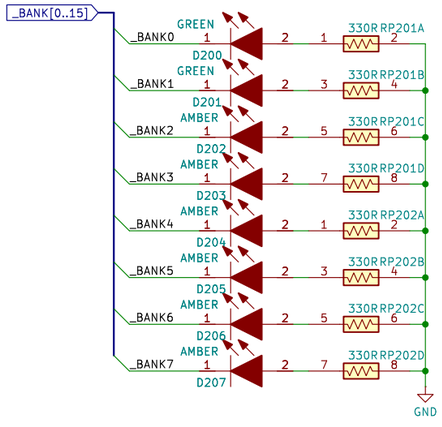


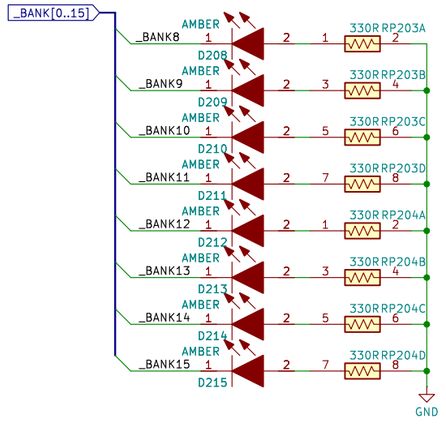
J206 & J207 are insurance for a long delay in elements 1 and 6.
If needed the CCKD/CCKQD clocks will be inverted and will need to change firmware.

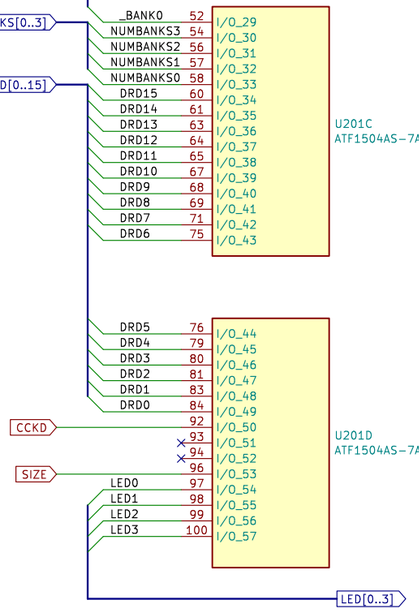
DEBUG LEDs

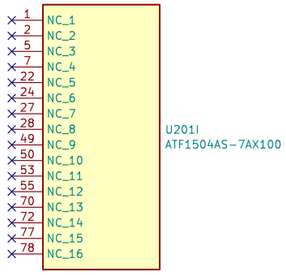


BANK LEDs

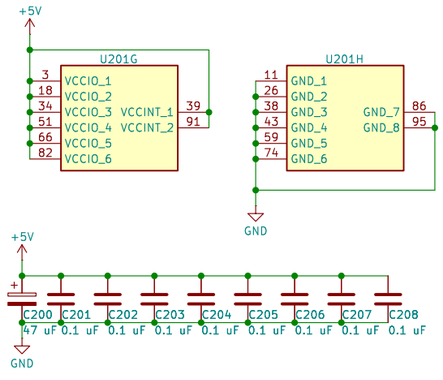




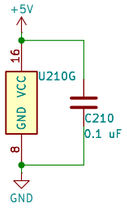




CPLD DECOUPLING



CLOCK DECOUPLING



Sheet: /Buddy & Expansion Logic/	
File: Page 03 - CPLD.kicad_sch	
Title: 3 MB BANK SWITCHING CHIP RAM CARD FOR SMD2000	
Size: A3	Date: 2025-06-09 **Rev: 0**
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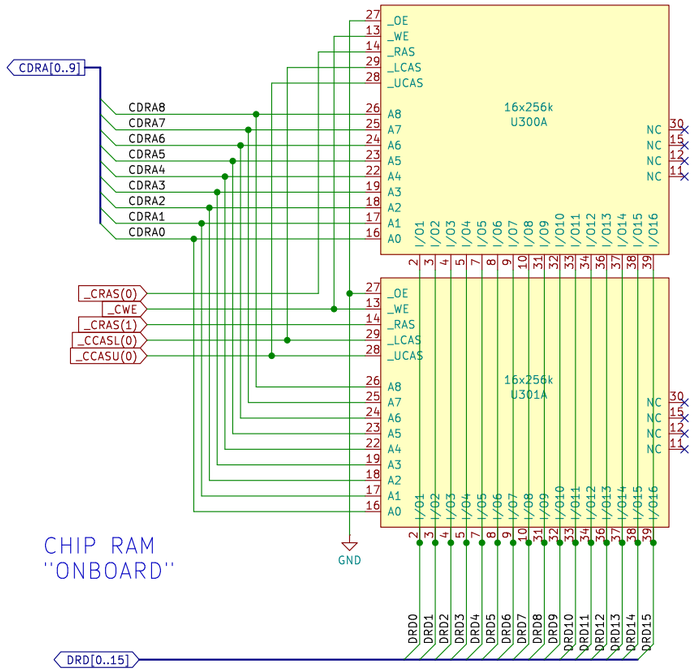
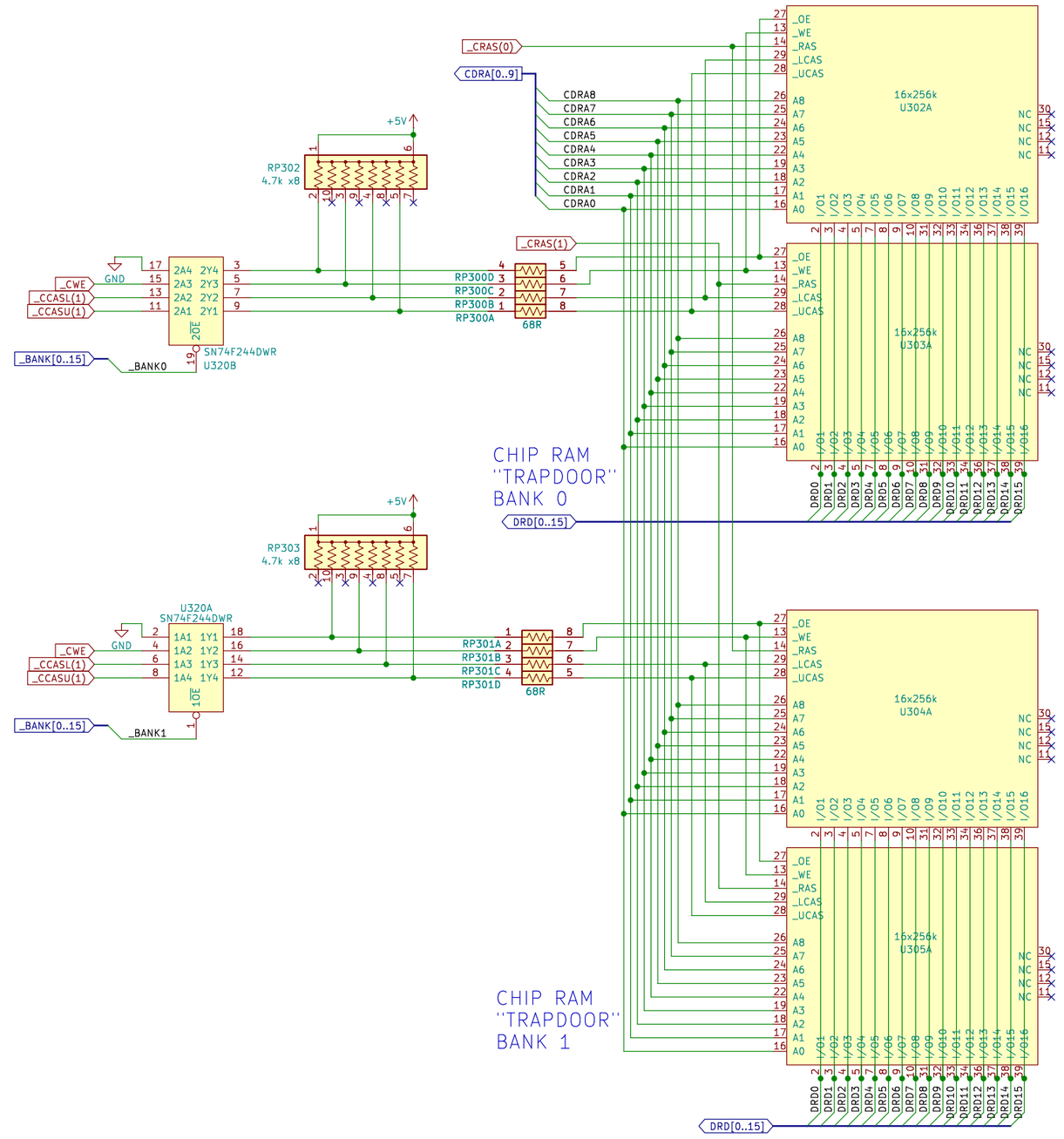
ALWAYS CONNECTED RAM



CHIP RAM "ONBOARD"

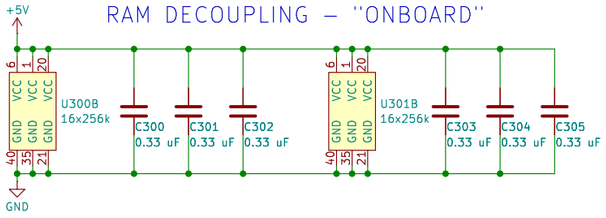
SELECTABLE RAM



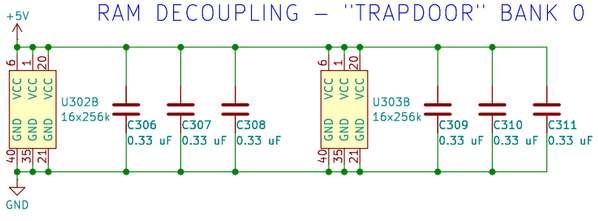
CHIP RAM "TRAPDOOR" BANK 0

CHIP RAM "TRAPDOOR" BANK 1

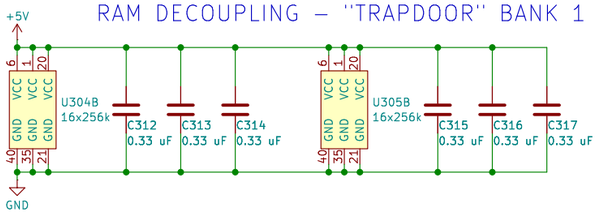
RAM DECOUPLING – "ONBOARD"



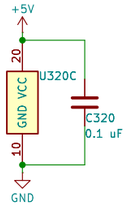
RAM DECOUPLING – "TRAPDOOR" BANK 0



RAM DECOUPLING – "TRAPDOOR" BANK 1



LOGIC DECOUPLING



Sheet: /RAM/		
File: Page 04 – RAM.kicad_sch		
Title: 3 MB BANK SWITCHING CHIP RAM CARD FOR SMD2000		
Size: A3	Date: 2025-06-09	**Rev: 0**
KiCad E.D.A. 8.0.6		Id: 4/4