Universitat Autònoma de Barcelona

Facultat d'Enginyeria
Grau en Enginyeria Informàtica
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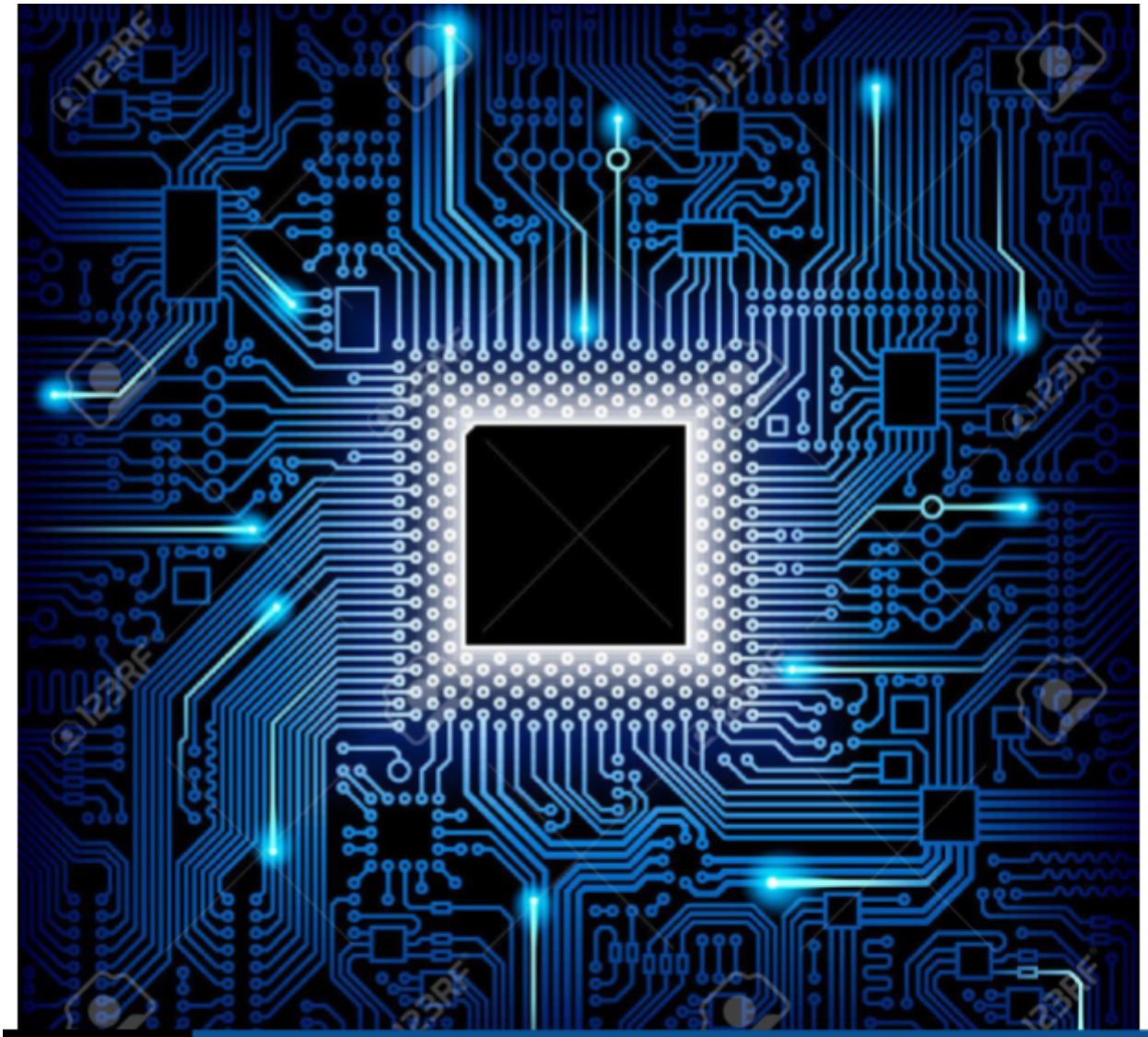

TREBALL DE FINAL DE GRAU

# AXI4 INTEGRATOR

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# Abstract

This project consists in the design of a tool which will be capable of interconnecting different components of a SoC (System-on-Chip) through their respective ports. This tool will be written in Python mostly but it will generate Verilog code as well in order to, later, connect the components. The components will be given in XML, using the protocol IP-XACT provided by Accellera. The user will be capable of editing the connections as well as making new ones.

# Context

The project comes from a larger work with the objective of making an app user-friendly capable of interconnecting modules with AXI4 similar to apps that already exists and are available in the market. These modules, though, use the royalty-free RISC-V architecture. The project is being developed for different parties including the Autonomous University of Barcelona (UAB) and National Microelectronics Center (IMB-CNM-CSIC).

# Objectives

The main objective of this project is to start building a Software which will be capable of programming different devices such as FPGA. This program plays a small part in the overall development. Its role has different parts:

- The program will be capable of reading an XML document and create the appropriate structures in order to store its information. That includes modules, with their different ports and parameters, and connections between them.
- It also needs to create new connections and edit the modules in any way the user desires.
- Finally, the connections need to be made using Verilog code. To do this task, the program will have to write this code in a file which later will be used to make the connections.

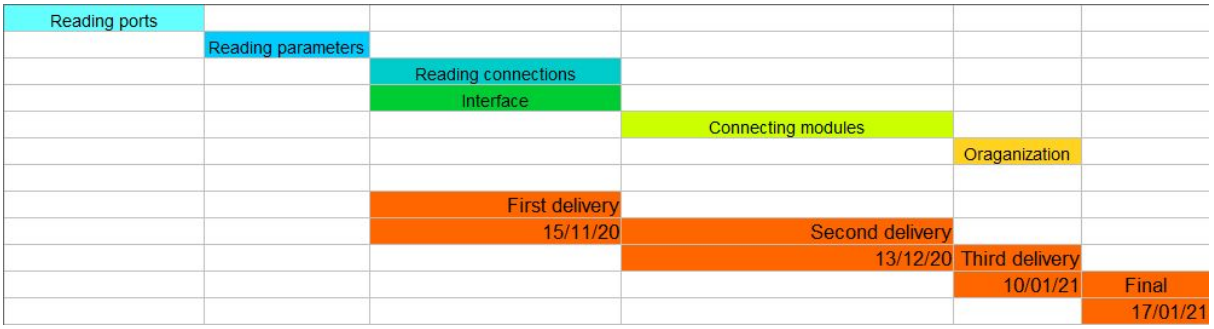
# Tasks

We can describe the project with the following tasks:

- First, we need to make a function capable of reading the modules written in XML using the IP-XACT protocol. Those modules may contain different amounts of ports, parameters and connections. The mentioned function will need to store each module with its ports and parameters as well as possible connections with other modules. So this first task can be divided into three different tasks at the same time:
    - Reading and storing of the ports
    - Reading and storing of the parameters.
    - Reading and storing of the connections.
- In second place, interaction with the user will be required so a simple interface in which the user can input the information he/she desires needs to be done. The interaction with the user will be done through the terminal. Overall it is a straightforward task so no much time will be spent in this.
- The third task will be connecting modules. Those modules will be connected both via Verilog (written in a file) and in the program (stored in the appropriate structures). This task requires the user to input the desired ports from the desired modules they wish to connect so an interface for that will be needed. Also a directory with the proper name will be created so that the project keeps an organized directory. It will be very time demanding
- Fourth and last, organizing the functions to make the code more readable as well as adding contingencies in the project so it doesn't crash whenever there's an error and instead notifies the user what the problem was.

# Schedule

The following image shows a time representation of the project as well as the different deliveries dates:




# Budget

The cost will remain in the Hardware that will be used since a royalty-free architecture will be used. In order to test the program, a 300€ FPGA will be needed to run it.

Also the human labor needs to be taken into account. 300 hours is the average time for a 12 CTS (credits) subject, using a 7€/hour as the salary (the average salary for a student in practice), this gives us a 2.100€ result. The teachers spend around 2 hours weekly for a total amount of 32 hours, with an average salary of 12.5€/hour adds to 400€ per teacher.

In total it will be around 3.200€. This price may differ depending on possible modifications in the schedule.

# Bibliography

IP-XACT User Guide:
https://www.accellera.org/images/downloads/standards/ip-xact/IP-XACT_User_Guide_2018-02-16.pdf

Tutorial Verilog:
http://www.iuma.ulpgc.es/~nunez/clases-FdC/verilog/Verilog%20Tutorial%20v1.pdf

XML - Wikipedia:
https://en.wikipedia.org/wiki/XML#:~:text=Extensible%20Markup%20Language%20(XML)%20is,free%20open%20standards%E2%80%94define%20XML.

AMBA® AXI™ and ACE™ Protocol Specification:
http://www.gstitt.ece.ufl.edu/courses/fall15/eel4720_5721/labs/refs/AXI4_specification.pdf

RISC-V:
https://en.wikipedia.org/wiki/RISC-V