Digital Multiplier in verilog

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I. Multiplier algorithms

In This report I want to explore different types of multipliers their advantages and disadvantages in terms of timing analysis, power consumption, and No of gates required. My entire results and code is open source and is available at github link here

II. Booth Multiplier

It is a multiplier algorithm for signed numbers. let A, B are inputs with both x bits then we use 3 numbers A, P, S 2*x+1 bits each. then we initialise A,S,P as follows

$A = \{A(xbits), x + 1zeros\}$

$S = \{-A(in2'scomplemetxbits), x + 1zeros\}$

$P = \{xzeros, B(xbits), 0(1bit)\}$

after that based on last 2 digits of P we repeat below process for x times (ignore any overflow in addition)

01: $P = (P + A) >>> 1$

10: $P = (P + S) >>> 1$

00: $P = (P) >>> 1$

11: $P = (P) >>> 1$

($>>>$ stands for arthematic shift)

III. Wallace Tree multiplier

It is a multiplier algorithm for signed numbers. First it computes all partial products and then it uses a selection of full and half adders to sum partial products in stages until two numbers are left. It uses Binary adder at end to compute final result.

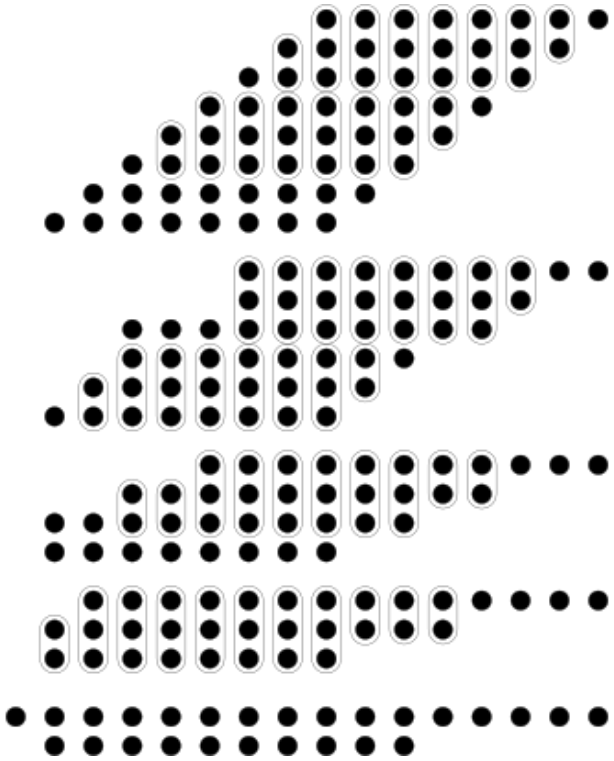

Fig 1: Wallace Tree visuvilization

As you can we Fig 1 shows 4 layes implemntation of wallace tree multiplier for input of size 8 bits.

IV. Results

After implementing code in vivado and taking other constrains in favour of hardware for zynq developement board we can go as lo as 10 ns for wallace pipelined and 10.5 ns for booth sequential model. Note that wallace pipelined multiplier takes 6 clock cycles to give result while sequential booth multiplier requires 9 clock cycles. No of LUTs utilised roughly doubled for wallace than compared to booth. For Wallace pipelined multiplier Flip Flop utilization is roughly 2.5 times the utilization of booth.

Bases on these results we can see that Booth sequential model uses far less gates and regesters as it removes the repeated hardware by using sequencial controller but takes more time to arrive at results (9 clock cycles) while pipelined wallace multiplier takes more gates but less time (6 clock cycles) as No of gates are less for booth we can expect less power utilization.

Note: This conclusions are for sequential Booth multiplier and pipelined version of wallace. These may change for combinatinal or other implementations and this minimum frequency and LUT utilization are done in vivado implementation software.This was not actually implemented

on actual FPGA and might differ significantly if you decided to use CMOS implementation instead of using FPGA.

V. References

Wikipedia - Booth Multiplier

Wikipedia - Wallace Tree