11 GHz Band 4×4 MIMO-OFDM Broadband Experimental System for 5 Gbps Super High Bit-Rate Mobile Communications

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***Abstract*— Super high bit-rate mobile communications have been investigated to achieve more than 10 Gbps bit-rate. This paper studies an experimental system that can achieve 5 Gbps throughput by using 11 GHz band radio frequency (RF) circuits and 4×4 MIMO-OFDM with 400 MHz wide bandwidth, of which feasibility is verified. The experimental system consists of (i) 11 GHz band RF circuits, (ii) FPGA boards with 800 MHz sampling DAC or ADC, and (iii) CPU boards that perform MIMO-OFDM transmission and reception processing in offline mode. The RF circuits employ a direct conversion method. Since IQ imbalance and phase noise in the RF circuits degrade transmission performance, this paper compensates for them by digital signal processing. The experimental system evaluates the transmission performance in 5 Gbps 4×4 MIMO-OFDM employing turbo detection, and it is shown that performance degradation of the experimental system to the simulation results can be limited to less than 1 dB by the compensation method for imperfection of the RF circuits. In addition, it is clarified that the turbo detection with two iterations can improve 6.0 dB at SNR to achieve 5 Gbps throughput.**

I. Introduction

Sophisticated mobile terminals such as smartphone are rapidly growing a demand for high bit-rate transmission, and the fourth-generation mobile communication systems target the maximum bit-rate of 1 Gbps [1]. In demonstration experiments to verify the higher bit-rate, 12×12 MIMO transmission with signal bandwidth of 100 MHz has achieved 5 Gbps [2], and a multiuser (MU) MIMO experiment that increases the number of antennas to 16 has been performed [3].

In order to realize the even higher bit-rate, super high bit-rate mobile communications attaining 30 Gbps bit-rate have been investigated, which is accomplished by 24×24 MIMO with the signal bandwidth of 400 MHz [4]. For verifying the super high bit-rate mobile communications by experiments, both baseband (BB) circuits that can support the wide bandwidth of 400 MHz and high-precision radio frequency (RF) circuits that can configure 24×24 MIMO should be developed. A basic hardware unit for its implementation corresponds to the 5 Gbps 4×4 MIMO, and totally, 24×24 MIMO is composed of six units. In order to verify the feasibility, 4×4 MIMO-OFDM BB experimental system with 400 MHz wide bandwidth has been developed [5].

This paper studies a 11 GHz band 4×4 MIMO-OFDM RF/BB experimental system by combining 11 GHz band RF circuits with the BB experimental system. The RF/BB experimental system consists of (i) 11 GHz band RF circuits, (ii) FPGA boards with 800 MHz sampling digital-to-analog converter (DAC) or analog-to-digital converter (ADC), and (iii) CPU boards that perform MIMO-OFDM transmission and reception processing in offline mode. The RF circuits employ a direct conversion method. Since IQ imbalance and phase noise in the RF circuits degrade transmission performance, this paper compensates for them by digital signal processing. Moreover, the turbo detection, which exploits bit log-likelihood ratio from the decoder output, is employed as MIMO signal detection, and reduces SNR to achieve 5 Gbps.

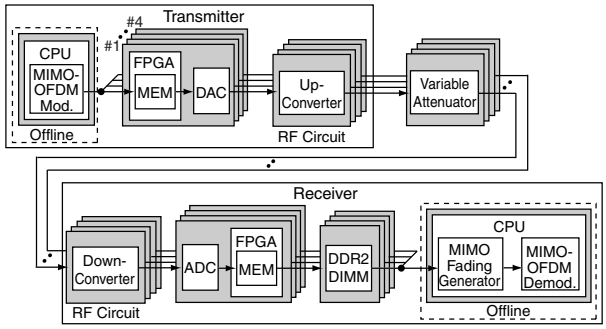

Fig. 1. 11 GHz band 4×4 MIMO-OFDM experimental system

TABLE I
SPECIFICATIONS OF 4 × 4 MIMO-OFDM

No. of transmit and receive antennas	4
Carrier frequency	11 GHz
RF output level per antenna	10 dBm
RF circuit architecture	direct-conversion
Occupied bandwidth	400 MHz
Sampling frequency	800 MHz
Subcarrier spacing	195 kHz
OFDM symbol duration	6.1 μs (GI: 1.0 μs)
Frame length	220 μs
No. of OFDM symbols in frame	preamble: 5, data: 31
Maximum bit-rate	5.1 Gbps (64QAM, $R = 3/4$)

II. 4×4 MIMO-OFDM Experimental System

A. Basic Configuration

A basic structure of the 11 GHz band 4×4 MIMO-OFDM experimental system is shown in Fig. 1, and basic specifications of the experimental system are listed in Table I. The MIMO-OFDM transmitter consists of a CPU board that performs the MIMO-OFDM transmission processing, FPGA boards with 800 MHz sampling DAC, and 11 GHz band RF transmitter circuit. The MIMO-OFDM transmitted signal which CPU generates in the offline mode is transferred and stored into the memory (MEM) inside FPGA, and then DAC repeatedly outputs the digital signal from the FPGA as an analog BB signal in real-time. The RF transmitter circuit up-converts the analog BB signal to carrier frequency of 11 GHz. The modulated signal is input into the RF receiver circuit through the variable attenuator.

The MIMO-OFDM receiver is composed of the RF receiver circuit, the FPGA boards with 800 MHz sampling ADC, memory boards with DDR2 DIMM, and the CPU board. The

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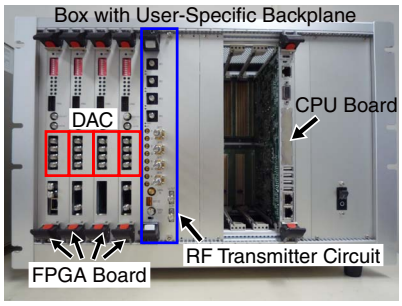


Fig. 2. MIMO-OFDM transmitter box

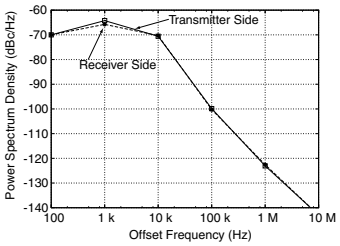


Fig. 3. Measured phase noise

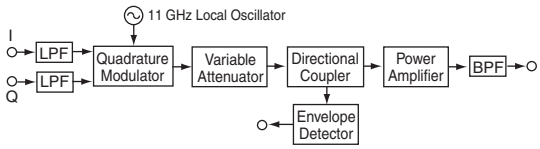


Fig. 4. 11 GHz band up-converter in RF transmitter circuit

input signal of the RF receiver circuit is down-converted to the BB signal. The sampled signals by ADC are transferred and stored into DDR2 DIMM via MEM inside FPGA in real-time. The CPU board periodically reads the sampled signals from DDR2 DIMM, and performs the MIMO-OFDM reception processing in the offline mode. In the experimental system, multipath fading channel and noise are generated and added into the sampled received signal inside the receiver because the radio station license is under application procedure. Carrier frequency of 11 GHz is dependent on the radio station license.

As shown in Table I, guard interval (GI) was set to 1.0 μs so as to deal with the multipath delay up to 1.0 μs. Subcarrier spacing was 195 kHz, and thus the OFDM symbol duration was 6.1 μs. One frame consists of 36 OFDM symbols, and with 64QAM and coding rate $R = 3/4$, the maximum bit-rate achieves 5.1 Gbps by taking into account the transmission efficiency. In the following sections, detailed hardware of the RF/BB MIMO-OFDM transmitter and receiver are introduced, and then the transmission/reception processing and compensation methods for the IQ imbalance are described.

B. RF/BB MIMO-OFDM Transmitter

Fig. 2 shows a MIMO-OFDM transmitter box including the BB and RF transmitter circuits. The BB transmitter circuit consists of four FPGA boards and the CPU board that are inserted into the compact PCI box, and each FPGA board mounts two FPGA chips of Xilinx Viterx-5 SX240T [6]. In addition, two-channel DAC circuit is attached on each FPGA board to output the I and Q components of the BB signal for each transmit antenna. Texas Instruments (TI) DAC DAC5682Z is employed in the DAC circuit, and it operates with 16-bit resolution and sampling frequency of 800 MHz

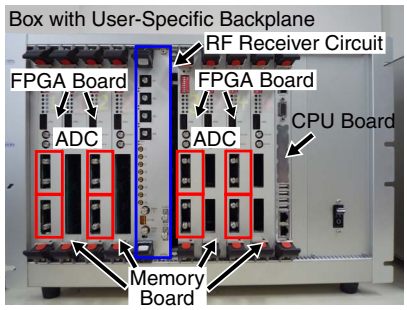


Fig. 5. MIMO-OFDM receiver box

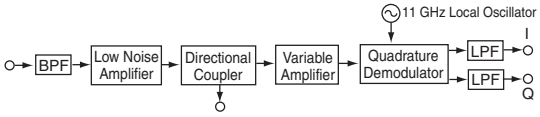


Fig. 6. 11 GHz band down-converter in RF receiver circuit

(up to 1 GHz). The BB transmitter circuit employs the cascade connection of the clock signal which is input into each FPGA board, and the phases of the clock signals in all the FPGA boards are different each other. Hence, time lag occurs in the four signal waveforms which DAC outputs. In addition, there exists the characteristic difference between the analog circuits of DAC. Thus, the BB calibration for them is performed [5].

The RF transmitter circuit is a compact PCI board, and consists of 11 GHz local oscillator and four up-converters for four transmit antennas. The local oscillator synchronizes the 10 MHz reference signal from the internal crystal oscillator or the external supply by using phase-locked loop, and it can output the local oscillator signal from the external terminal, which is exploited to establish phase-noise-free situation. Measured power spectrum density of the phase noise in the 11 GHz local oscillator signal is depicted in Fig. 3. The phase noise level is large enough to degrade the transmission performance at the frequency of less than 100 kHz. However, the frequency range is narrower than the subcarrier spacing of 195 kHz, and thus the phase noise compensation for the common phase error (CPE), which is the mean of the phase noise during one OFDM symbol and which induces the common phase rotation on all the subcarriers in frequency domain, is required.

Fig. 4 shows a block diagram of the up-converter. The direct conversion method modulates I and Q components of the BB signal into the 11 GHz RF signal, and the passband frequency of low-pass filter (LPF) is from DC to 250 MHz. The CPU board can control the gain of the power amplifier from -3 dB to 17 dB in 1 dB step. Then, the RF output level is changed from -10 dBm to 10 dBm.

C. RF/BB MIMO-OFDM Receiver

A MIMO-OFDM receiver box including the BB and RF receiver circuits is shown in Fig. 5. The BB receiver circuit consists of four FPGA boards with the ADC circuits, four memory boards with 8 GB DDR2 DIMM, and the CPU board. Two ADC circuits are attached on each FPGA board, and TI ADC ADS5474 with 14-bit resolution and sampling frequency of 400 MHz is employed. For two-times-oversampling the bandwidth of 400 MHz, 800 MHz sampling ADC is realized by parallel 400 MHz sampling ADCs using

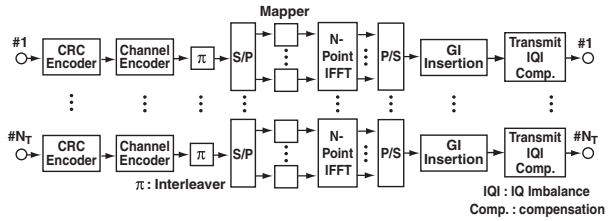


Fig. 7. MIMO-OFDM transmission processing

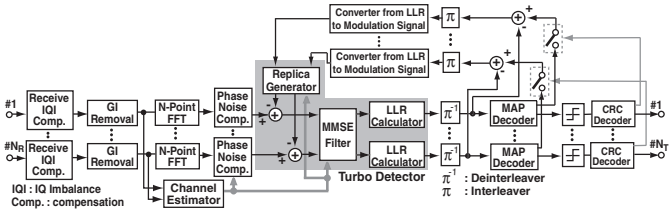


Fig. 8. MIMO-OFDM reception processing

the reverse-phase clock. The characteristic difference between the analog circuits of the two ADCs is compensated by the BB calibration. The ADC circuit can realize the high-precision interleaved ADC by exploiting a delay chip (ON Semiconductor MC10EP195) that can delay the clock signal in the 10 ps step. By changing the control registers inside FPGA, the CPU board can control the BB circuit via the PCI bus by the software.

The RF receiver circuit is also a compact PCI board, and consists of the 11 GHz local oscillator and four down-converters. The structure of the local oscillator on the receiver side is the same as that on the transmitter side, and the performance is also the same as shown in Fig. 3. Fig. 6 depicts a block diagram of the down-converter which also employs the direct conversion method. It can extract the I and Q components of the BB signal of -7 dBm from the RF input signal whose signal level is -60 dBm to -40 dBm by changing the gain of 53 dB to 33 dB.

III. Transmission and Reception Processing

A. MIMO-OFDM Transmission and Reception Processing

Fig. 7 shows the MIMO-OFDM transmission processing with N_T transmit antennas. It first adds the cyclic redundancy check (CRC) code to information bits of each OFDM symbol to detect a decision error, and then it encodes the information bits by using the convolutional code. After interleaving the coded bits, it maps them into a modulation signal at each subcarrier. Next, N-point IFFT transforms the modulation signals into the time-domain signals, and then GI is inserted. Finally, IQ imbalance compensation for the RF transmitter circuit is performed. The transmit IQ imbalance compensation is described in section III-B. Note that a preamble is time-multiplexed at the head of the frame [5], and same pilot signals for the N_T streams are inserted into the pilot subcarriers during the data OFDM symbols.

The MIMO-OFDM reception processing with N_R receive antennas is shown in Fig. 8. It first performs receive IQI compensation that is described in section III-C. Next, it carries out the channel estimation by using the preamble, and the received signals which N-point FFT transforms into the frequency-domain signals are processed by the phase noise compensation. The phase noise compensation estimates CPE by using the pilot signals, and removes CPE by dividing the post-FFT signals by the estimated CPE [7]. After that, the turbo detector extracts the N_T streams from the compensated received signals. In an initial processing of the turbo detection, it operates as the MMSE detection because it cannot obtain bit log-likelihood ratios (LLRs) which the MAP decoders output. After deinterleaving the bit LLRs which the turbo detector calculates, the MAP decoder yields (coded) bit LLR and LLR of the information bit for each stream. If the CRC decoder detects any decision errors from the information bits, the initial processing is shifted to an iterative processing. Otherwise, the reception processing ends.

In the iterative processing, the turbo detector generates received signal replicas of all the streams from the bit LLRs of the MAP decoder outputs. Next, it cancels the other streams from the received signals, and then combines the desired signal components and suppresses a residual cancellation error by using a MMSE-based linear filter [5]. After deinterleaving the bit LLRs which the turbo detector calculates from the output of the MMSE filter, the MAP decoding for each stream is performed again. The reception processing repeats the iterative processing until the maximum number of iterations or CRC does not detect any decision errors.

B. Transmit IQ Imbalance Compensation

Since the IQ imbalance in the RF transmitter and receiver circuits severely degrades the transmission performance in 5 Gbps 4×4 MIMO-OFDM, the IQ imbalance compensation was introduced into the experimental system. First, let us model the IQ imbalance in the RF transmitter circuit mathematically. Let $s_i(t)$ and $s_q(t)$ denote I and Q components of the BB input signal to the quadrature modulator, and a BB input signal vector $\mathbf{s}(t)$ is defined as $\mathbf{s}(t) = [s_i(t)\ s_q(t)]^{\mathrm{T}}$ where the superscript $^{\mathrm{T}}$ denotes transposition. In addition, a modulated signal vector distorted by the IQ imbalance is defined as $\tilde{\mathbf{s}}(t) = [\tilde{s}_i(t)\ \tilde{s}_q(t)]^{\mathrm{T}}$, and $\tilde{\mathbf{s}}(t)$ is given by

$$\tilde{\mathbf{s}}(t) = \mathbf{A}_t \left[\mathbf{s}(t) + \mathbf{b}_t\right] \ , \tag{1}$$

$$\mathbf{A}_t = \begin{bmatrix} 1 & -(1+\kappa_t)\sin\Delta\phi_t \\ 0 & (1+\kappa_t)\cos\Delta\phi_t \end{bmatrix}, \ \mathbf{b}_t = \begin{bmatrix} \Delta i_t \\ \Delta q_t \end{bmatrix} \ , \tag{2}$$

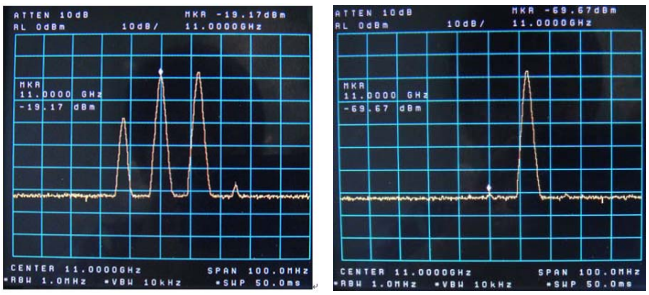
where κ_t is an amplitude error of the Q component against the I component, $\Delta\phi_t$ is a phase error in the $\pi/2$ phase shifter, Δi_t and Δq_t are DC offsets of the I and Q components [8].

Let $\hat{\kappa}_t$, $\Delta\hat{\phi}_t$, $\Delta\hat{i}_t$, and $\Delta\hat{q}_t$ denote estimated parameters of the IQ imbalance, respectively, and the IQ imbalance can be compensated by giving an inverse function of the IQ imbalance in (1) to a desired BB signal vector $\hat{\mathbf{s}}(t)$. Then, a predistorted BB signal vector $\mathbf{s}_d(t)$ for the IQ imbalance compensation is given by

$$\mathbf{s}_d(t) = \hat{\mathbf{A}}_t^{-1}\ \hat{\mathbf{s}}(t) - \hat{\mathbf{b}}_t \ , \tag{3}$$

where $\hat{\mathbf{A}}_t$ and $\hat{\mathbf{b}}_t$ are estimates of $\mathbf{A}_t$ and $\mathbf{b}_t$, respectively. By substituting $\mathbf{s}_d(t)$ into $\mathbf{s}(t)$ in (1), $\tilde{\mathbf{s}}(t)$ can approach asymptotically to $\hat{\mathbf{s}}(t)$.

This paper employs a simple parameter estimation method that measures a spectrum of the modulated signal by using the spectrum analyzer and that recursively updates the estimated



(a) Spectrum before compensation (b) Spectrum after compensation

Fig. 9. Effect of IQ imbalance compensation

TABLE II

ESTIMATED TRANSMIT IQ IMBALANCE

RF CH	$\hat{\kappa}_t$	$\Delta\hat{\phi}_t$ (deg)	$\Delta\hat{i}_t$	$\Delta\hat{q}_t$
1	-0.013	-10.71	0.639	0.389
2	-0.014	-10.37	0.618	0.368
3	-0.014	-10.71	0.644	0.301
4	-0.010	-10.37	0.610	0.377

parameters so as to reduce the levels of the carrier leakage and the image leakage by perturbation method. Fig. 9 (a) shows a spectrum of 12.5 MHz complex sinusoidal wave before the IQ imbalance compensation, and the carrier leakage at 11 GHz and the image leakage at 10.9875 GHz occur. On the other hand, as shown in Fig. 9 (b), the carrier leakage and the image leakage can be removed by adjusting $\hat{\mathbf{b}}_t$ and $\hat{\kappa}_t$, $\Delta\hat{\phi}_t$ in $\hat{\mathbf{A}}_t$, respectively. The estimated IQ imbalance parameters are summarized in Table II. It is found that the phase error and the DC offset are relatively large.

C. Receive IQ Imbalance Compensation

The RF received signal vector, which is represented in the lowpass equivalent model, is defined as $\mathbf{r}(t) = [r_i(t)\ r_q(t)]^{\mathrm{T}}$, and the BB signal vector, which the quadrature demodulator outputs, $\tilde{\mathbf{r}}(t) = [\tilde{r}_i(t)\ \tilde{r}_q(t)]^{\mathrm{T}}$ is expressed as

$$\tilde{\mathbf{r}}(t) = \mathbf{A}_r\,\mathbf{r}(t) + \mathbf{b}_r\ , \tag{4}$$

$$\mathbf{A}_r = \begin{bmatrix} 1 & 0 \\ -(1+\kappa_r)\sin\Delta\phi_r & (1+\kappa_r)\cos\Delta\phi_r \end{bmatrix}\ , \tag{5}$$

$$\mathbf{b}_r = [\Delta i_r\ \Delta q_r]^{\mathrm{T}}\ , \tag{6}$$

where κ_r and $\Delta\phi_r$ are the amplitude error and the phase error in the quadrature demodulator, and Δi_r and Δq_r are DC offsets of the I and Q components [8].

Similar to the transmitter side, the receive IQ imbalance compensation provides the inverse function of the IQ imbalance in (4). A compensated BB signal vector $\hat{\mathbf{r}}(t) = [\hat{r}_i(t)\ \hat{r}_q(t)]^{\mathrm{T}}$ can be given by

$$\hat{\mathbf{r}}(t) = \hat{\mathbf{A}}_r^{-1}\left[\tilde{\mathbf{r}}(t) - \hat{\mathbf{b}}_r\right]\ , \tag{7}$$

where $\hat{\mathbf{A}}_r$ and $\hat{\mathbf{b}}_r$ are estimates of $\mathbf{A}_r$ and $\mathbf{b}_r$, respectively.

After the transmit IQ imbalance is compensated, the receive IQ imbalance parameters are estimated. It is assumed that $r_i(t)$ and $r_q(t)$ are zero-mean, variance σ_r^2, and uncorrelated. Then, $\hat{\mathbf{b}}_r$ can be estimated by calculating ensemble average of $\tilde{\mathbf{r}}(t)$ in (4), that is, $\mathrm{E}[\tilde{\mathbf{r}}(t)] = \hat{\mathbf{b}}_r$, where $\mathrm{E}[\ ]$ denotes the ensemble average. In addition, by calculating a covariance matrix of $\tilde{\mathbf{r}}(t)$, $\hat{\kappa}_r$ and $\Delta\hat{\phi}_r$ can be estimated as [8]

$$\hat{\kappa}_r = \sqrt{\frac{\mathrm{E}\left[(\tilde{r}_q(t) - \Delta\hat{q}_r)^2\right]}{\mathrm{E}\left[(\tilde{r}_i(t) - \Delta\hat{i}_r)^2\right]}} - 1\ , \tag{8}$$

$$\Delta\hat{\phi}_r = -\sin^{-1}\left\{\frac{\mathrm{E}\left[(\tilde{r}_i(t) - \Delta\hat{i}_r)(\tilde{r}_q(t) - \Delta\hat{q}_r)\right]}{\sqrt{\mathrm{E}\left[(\tilde{r}_i(t) - \Delta\hat{i}_r)^2\right]\mathrm{E}\left[(\tilde{r}_q(t) - \Delta\hat{q}_r)^2\right]}}\right\}. \tag{9}$$

The estimated parameters of the receive IQ imbalance are summarized in Table III, and the receive IQ imbalance is smaller than the transmit IQ imbalance.

TABLE III

ESTIMATED RECEIVE IQ IMBALANCE

RF CH	$\hat{\kappa}_r$	$\Delta\hat{\phi}_r$ (deg)	$\Delta\hat{i}_r$	$\Delta\hat{q}_r$
1	0.025	-2.03	0.228	-0.037
2	0.002	-2.26	0.423	-0.165
3	-0.002	-2.36	0.052	-0.026
4	0.016	-1.50	-0.401	0.015

TABLE IV

EXPERIMENTAL CONDITIONS

No. of FFT points	4096
No. of subcarriers	data: 2012, pilot: 32
Modulation scheme	64QAM
Channel coding	convolutional code ($R = 3/4$)
Interleaver	block (12072-bit)
MAP decoding	Max-Log-MAP algorithm
Maximum no. of iterations	2
Channel model	40-path Rayleigh fading with exponential decay
Maximum delay	0.78 μs
Power ratio of first to last path	20 dB
Maximum Doppler freq.	0 Hz

IV. EXPERIMENTAL EVALUATION

A. Experimental Conditions

In order to verify the 4×4 MIMO-OFDM RF/BB experimental system, laboratory experiments of 5 Gbps transmission were conducted. The gains of the transmit power amplifier and the receive power amplifier were set to 17 dB and 33 dB, respectively. The attenuation value in the variable attenuator was fixed to 40 dB. In order to remove an effect of the carrier frequency offset, 10 MHz reference signal was shared on the transmitter and receiver sides. Other additional experimental conditions are listed in Table IV. The number of FFT points was 4096, and the numbers of data subcarriers and pilot subcarriers were 2014 and 32, respectively. The modulation scheme was 64QAM, and the convolutional code with $R = 3/4$ was employed for channel coding. The maximum bit-rate becomes 5.1 Gbps. The maximum number of iterations in the turbo detection was two. CPU on the receiver side generates 40-path fading channel with the exponential decay and noise. The MIMO channel was assumed to be spatially uncorrelated.

B. Measured EVM

First, in order to verify both the transmit/receive IQ imbalance compensation and the phase noise compensation, error vector magnitude (EVM) was measured in four SISO-OFDM channels where there were not the multipath fading and the noise. Table V summarizes the measured EVMs.

TABLE V
MEASURED EVM IN FOUR SISO-OFDM CHANNELS

CH	BB	RF/BB				
	no-IQI	IQI	Tx IQIC	Tx & Rx IQIC		
	no-PN	no-PN			PN	CPEC
1	0.97 %	7.06 %	2.99 %	2.59 %	6.56 %	3.59 %
2	1.73 %	8.49 %	2.59 %	2.54 %	6.77 %	3.54 %
3	1.07 %	9.35 %	2.91 %	2.63 %	7.09 %	4.52 %
4	1.04 %	7.05 %	3.37 %	2.36 %	6.81 %	3.18 %
Ave	1.20 %	7.99 %	2.97 %	2.53 %	6.81 %	3.71 %

For comparison, EVM measured in the BB experimental system was also added. The BB experimental system causes no IQ imbalance (no-IQI) and no phase noise (no-PN), and can achieve 1.2 % in the average (Ave) EVM among four channels by the high-precision BB calibration. The RF/BB experimental system with no-PN causes the EVM degradation due to IQI, which decreases the average EVM to almost 8 %. On the other hand, the transmit (Tx) and receive (Rx) IQI compensation (IQIC) can alleviate the degradation to the average EVM of 2.5 %. In addition, when the influence of the phase noise was added to the above situation (without sharing the local oscillator signal), the average EVM was 6.8 % while the CPE compensation (CPEC) can reduce it to 3.7 %. Therefore, it can be seen that the RF/BB experimental system requires both IQIC and CPEC to reduce the measured EVM to the sufficiently low level.

C. Measured Transmission Performances

Next, block error rate (BLER) performances were measured by the RF/BB experimental system where both IQIC and CPEC were performed. One OFDM symbol was treated as one block, and the channel coding was performed by one block unit. Fig. 10 shows the measured BLER performances. For comparison, both computer simulation results and the BB experimental results are also plotted. When the RF/BB experimental system does not employ CPEC, the measured BLER significantly degrades. On the other hand, the turbo detection with CPEC can drastically improve BLER by increasing the number of iterations, and the measured BLER in the RF/BB experimental system can limit SNR degradation from the simulation results at BLER $= 10^{-2}$ to 1 dB.

In addition, throughput performances that are calculated from the BLER performances are examined in Fig. 11. It is found that the turbo detection with two iterations can achieve the throughput of 5 Gbps at SNR = 19.0 dB even in the RF/BB experiment, and that it can reduce the received SNR to achieve 5 Gbps by 6.0 dB in comparison with the MMSE detector in the initial processing.

V. CONCLUSIONS

This paper has studied the 11 GHz band 4×4 MIMO-OFDM RF/BB experimental system realizing the 5 Gbps bit-rate with 400 MHz bandwidth. The experimental system consists of (i) 11 GHz band RF circuits, (ii) FPGA boards with 800 MHz sampling DAC or ADC, and (iii) CPU boards that perform MIMO-OFDM transmission and reception processing in offline mode. Since IQ imbalance and phase noise in the RF circuits severely degrade 5 Gbps transmission performance, the IQ imbalance and the phase noise compensations by the digital signal processing have been applied to the RF/BB experimental system, which reduces the average EVM to the sufficiently low level and which enables the experimental system to achieve the 5 Gbps bit-rate. Moreover, the experimental results have demonstrated that the turbo detection with two iterations can improve 6.0 dB at the received SNR to achieve 5 Gbps even in the RF/BB experiment system with the large IQ imbalance and phase noise.

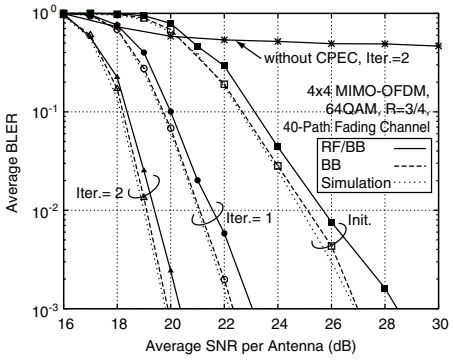


Fig. 10. Average BLER performance

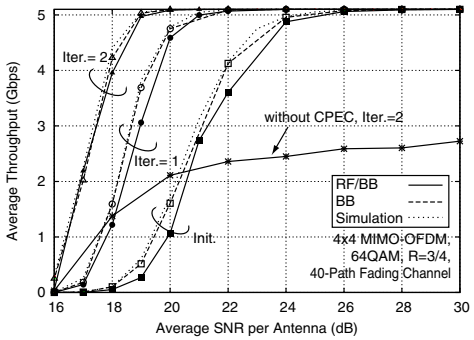


Fig. 11. Throughput performance

ACKNOWLEDGEMENT

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