Realization of DBF-OFDM Transceiver for Vehicular Communication Using FPGA Chip

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***Abstract*—Following the Dedicated Short Range Communications (DSRC) vehicular communications IEEE802.11p physical layer standards, this paper implements the OFDM baseband processing modules on the FPGA platform. The digital beam-forming (DBF) smart antenna technology is applied for Orthogonal Frequency Division Multiplexing (OFDM) transceiver to identify the cars on the highway and to improve the bit error rate (BER) performance in applications of DSRC vehicular communication transceivers on the vehicle position system (VPS)-based electronic toll collection (ETC) system. Three-element array antenna is chosen in order to satisfy the FPGA chip's constraint of processing 108 bits input data per time clock.**

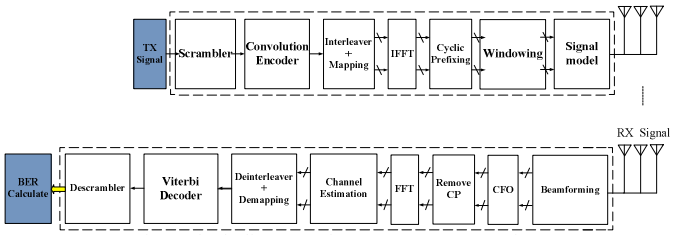
The experimental results demonstrate that three-element DBF-OFDM is superior to SISO-OFDM about 4dB gain in signal to noise ratio (SNR). Both the DBF-OFDM and SISO-OFDM operated in 13*n*s delay spread fading channel have better performance than 26*n*s delay spread fading channel when the BER is 10^{-5}. The performance for both the DBF-OFDM and SISO-OFDM systems operated in 60km/h user speed is better than 120km/h user speed. The FPGA hardware resource utilizations of the DBF-OFDM and SISO-OFDM systems are also compared.

I. INTRODUCTION

Recently, the vehicle position system (VPS)-based electronic toll collection (ETC) system [1] is going to be deployed on the highway in Taiwan. Most VPS-based ETC systems have included the communication link between the mobile station (MS) and mobile switching monitoring center (MSMC), which provides transmission of the vehicle position measured from the GPS receiver; transmission of an user ID number used to identify the vehicle to ETC system; transmission and updating of the charging data stored in the on-board unit (OBU); transmission of the system status message; integration with other intelligent transportation system (ITS) services [2][3]. With proper planning, the dedicated short range communications (DSRC) system overlaid on the ETC virtual gantry (VG) region can fulfill the subscriber's demand for mobile data transmission in the service area. The VGs distribute at the highway entrance, highway exit and in the highway. The DSRC system, which is one of the key technologies for ITS [3], provides wireless communications over a line-of-sight distance of less than 1 km between the roadside units (RSU) and mostly high-speed MS units but occasionally between MSs on two high-speed vehicles.

An array antennas mounted on base stations (BSs) of mobile radio systems plays an important role in fulfilling the increased demand for channels [4]. Beam former steers beams on the wanted signals and nulls toward interferences to increase carrier to interference ratio, which leads to an increase of channel capacity because multi-user interference can be reduced by beam-space filtering [5]. In this paper, a three-element digital beam-forming (DBF) is applied to a Orthogonal Frequency Division Multiplexing (OFDM) transceiver to identify the cars on the highway and to improve the bit error rate (BER) performance. The DBF-OFDM is realized using a field programmable gate array (FPGA) for the DSRC system.

II. DBF-OFDM[3][4]



Fig,1 Block diagram of DBF-OFDM transceiver

The block diagram of the DBF-OFDM transceiver is shown in Fig. 1 in which the subsystems in the dotted box are implemented with FPGA chip. For the transmitter, after processing the scrambler, convolution encoder and interleave, followed by mapping to BPSK or QAM constellation points, the transmitting data stream is divided into several parallel bit streams. An OFDM signal is constructed using an inverse fast Fourier transform (IFFT). The cyclic prefixes (CP), which are generated with the copies of the last parts of the OFDM symbol, are pre-pended to the front of each OFDM symbol. The cyclic prefixing output symbol is multiplied by windowing function and processed by signal module to generate the output OFDM pulse.

First, the received OFDM pulse is processed by DBF module in the receiver. After removing the CP, the received signal is demodulated by FFT module. Suppose that the guard interval is longer than the length of channel impulse response, that is, there is no inter-symbol interference between OFDM symbols. The accurate channel frequency response is estimated to compensate the frequency and phase errors caused by the fading channels. Then, the received OFDM symbol is processed by de-constellation, de-mapping, channel decoding and de- scrambler.

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III. DBF PRINCIPLE

For a linear uniform array of N isotropic elements, The diagram of a linear uniform array of N isotropic elements [6] is shown in Fig. 2, where the inter-element spacing is d, and the incident angle of a far field source is θ_0(radian). The antenna directivity is expressed as follows: [7]

$$D = \frac{p(\theta,\phi)_{\max}}{\frac{1}{4\pi}\int_0^{2\pi}\int_0^{\pi} p(\theta,\phi)\sin\theta d\theta d\phi} \tag{1}$$

, where $p(\theta,\phi)$ is the antenna pattern. When θ is a fixed direction, the directivity can be simplified as:

$$D = \frac{p(\phi)_{\max}}{\frac{1}{2\pi}\int_0^{2\pi} p(\phi)d\phi} \tag{2}$$

The antenna gain is defined as $G = \eta D$, where the value of η is between 0 and 1.

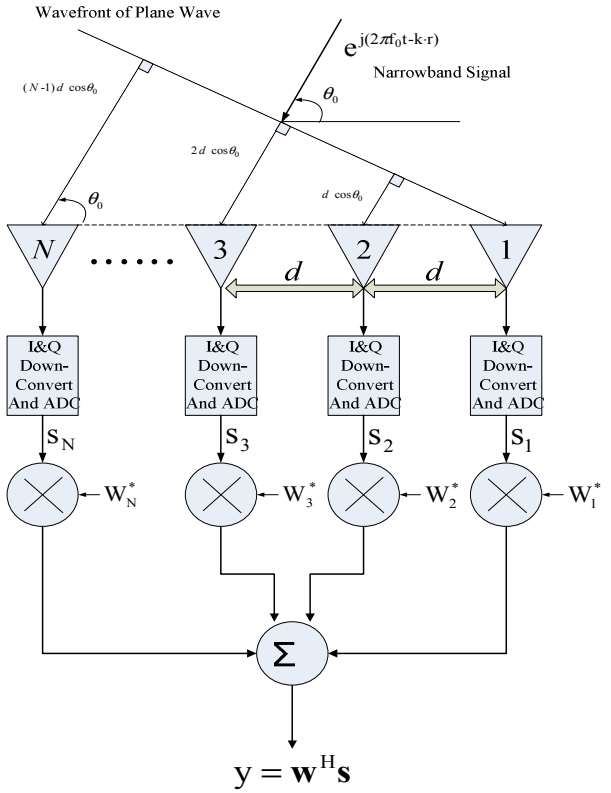


Fig.2 The linear array antenna diagram

The complex envelope at the n_{th} antenna element is

$$s_n = e^{j\ 2\pi\ (n-1)\frac{d}{\lambda}\cos\theta_0},\ n\ =\ 1,\ \ldots,\ N \tag{3}$$

, where λ is the wavelength of the received signal. The DBF output is a scalar.

$$y = \sum_{n=1}^{N} w_n^* s_n\ =\ \mathbf{w}^H\mathbf{s} \tag{4}$$

, where the symbol $(\cdot)^*$ denotes the complex conjugate and symbol $(\cdot)^H$ denotes the transpose complex conjugate or Hermitian transpose. At the same time, it is defined that $\mathbf{s}\in C^N$, $\mathbf{w}\in C^N$, where C^N denotes an N-dimensional complex vector. Therefore, the pointing vector $\mathbf{s}(\theta_0)$ and the weighting matrix $\mathbf{w}$ are expressed as

$$\mathbf{s}(\theta_0)\triangleq\begin{bmatrix} s_1 \\ s_2 \\ s_3 \\ \vdots \\ s_N \end{bmatrix} = \begin{bmatrix} e^{j0} \\ e^{j2\pi\frac{d}{\lambda}\cos\theta_0} \\ e^{j2\pi(2)\frac{d}{\lambda}\cos\theta_0} \\ \vdots \\ e^{j2\pi(N-1)\frac{d}{\lambda}\cos\theta_0} \end{bmatrix} \tag{5}$$

$$\mathbf{w} = \begin{bmatrix} w_1 \\ w_2 \\ w_3 \\ \vdots \\ w_N \end{bmatrix} \tag{6}$$

Under the constraint of $\|\mathbf{w}\|^2 = \text{constant} < \infty$, the maximum response output is

$$\max_{\{w\}}|y|^2 = \max_{\{w\}}|\mathbf{w}^H\mathbf{s}|^2 \tag{7}$$

$$|\mathbf{w}^H\mathbf{s}|^2 \le \|\mathbf{w}\|^2\|\mathbf{s}\|^2 \tag{8}$$

Then the relationship between $\mathbf{w}$ and $\mathbf{s}$ is

$$\mathbf{w} = \kappa\cdot\mathbf{s} \tag{9}$$

, where κ is a scalar. The DBF output is

$$y = \mathbf{w}^H x\ =\ \kappa\sum_{n=1}^{N} x_n e^{-j2\pi(n-1)\frac{d}{\lambda}\cos\theta_0} \tag{10}$$

If $\kappa = 1$, then the output response of the n_{th} array branch is

$$x_n\ =\ e^{j2\pi(n-1)\frac{d}{\lambda}\cos\theta}\ ,\ n\ =\ 1\ ,\ \ldots\ ,\ N \tag{11}$$

For instance, if $d = \lambda/2$, $N = 3$, $\theta_0 = 0°$, and let θ vary in $0^\circ \sim +180^\circ$, the antenna pattern is equivalent to $|y|^2$ versus θ. After the phase compensation, three independent signals that are obtained from three adjacent elements are combined to generate an antenna pattern of -10dB side lobe level and 4.59 dB antenna gain. The antenna pattern is shown in dotted curve of Fig. 3.

The Chebyshev weighting is used to reduce the side lobe level. Let the Chebyshev polynomial

$$\begin{aligned} T_m(u) &= \cos(m\cos^{-1}u) \qquad |u|\le 1 \\ &= \cosh(m\cosh^{-1}u) \qquad |u|\ge 1 \end{aligned} \tag{12}$$

equal to the desired side lobe level 20log$b$ (dB), that is,

$$T_{2M-1}(u_0) = b \tag{13}$$

The Chebyshev weighting for even ($2M$) array element is

$$I_n = \sum_{p=n}^{M}(-1)^{M-p}\frac{2M-1}{2(M+p-1)}C_{2p-1}^{M+p-1}C_{p-n}^{2p-1}u_0^{\,2p-1} \tag{14}$$

The Chebyshev weighting for odd ($2M$+1) array element is

$$I_n = \sum_{p=n}^{M}(-1)^{M-p}\frac{M}{M+p}C_{2p}^{M+p}C_{p-n}^{2p}u_0^{\,2p} \tag{15}$$

When the 20dB Chebyshev weighting is applied to DBF, the side lobe level of antenna pattern is reduced to -20dB but the antenna gain is also reduced to 3.86dB. The antenna pattern is shown in solid curve of Fig. 3.

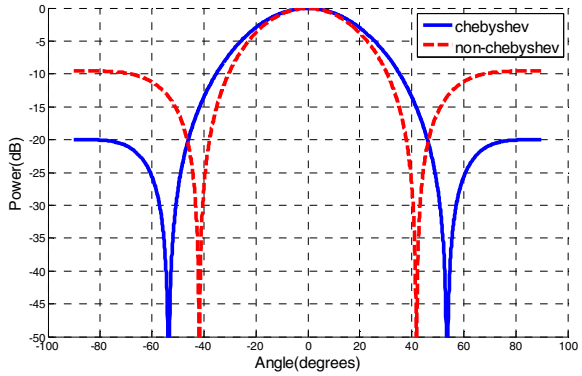
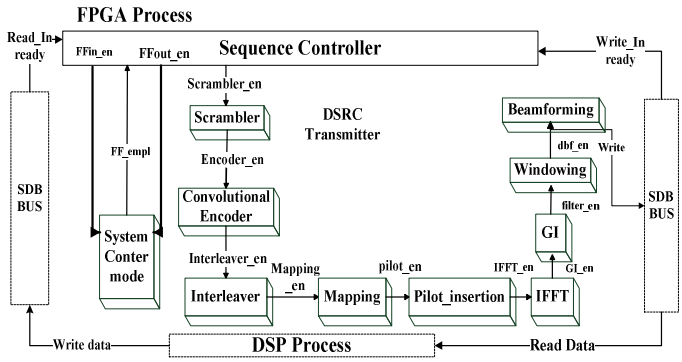


Fig. 3 20-dB Chebyshev Antenna pattern (solid curve)

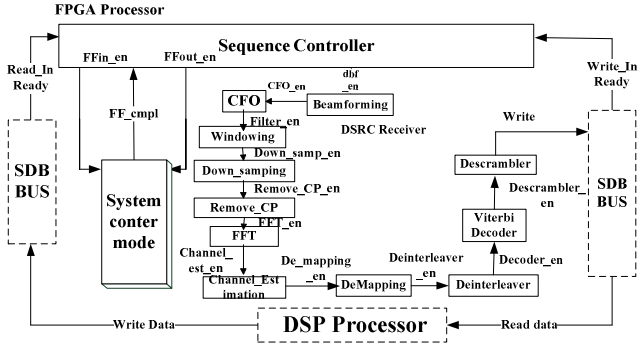
IV. IMPLEMENTATIONS

The DBF-OFDM transceiver is realized with Virtex II xc2v8000-ff1152-4 FPGA chip [8], 3L Diamond[9] and TMS320C6713 DSP processor [10]. Due to the maximum data transmission per time clock of the FPGA chip is 128 bits, the DBF module can only process the received signals generated from three element array antenna. Because each processed signal received from an antenna branch contains 36 bits.

A. Transceiver Hardware



(a)



(b)

Fig. 4 Flow structure of DBF-OFDM transceiver (a) transmitter, (b) receiver

Figure 4 shows the processing structure of DBF-OFDM transceiver. The processing time of each module must be less than the symbol interval of 8μsec in order to satisfy the requirement of real-time DSRC communications. The SISO-OFDM can be implemented with the same modules as the DBF-OFDM.

B. Beamforming Module

Three received signals are input to beamforming module, which generates the DBF output using formula (4). Figure 5 shows the hardware structure of the beamforming module, which constitutes of array response sub-module, Chebychev window sub-module and Combiner sub-module. The coordinate rotation digital computer (CORDIC) rotation module [11] is employed to compute $\cos\theta_0$ in the array response module. The three received signals are multiplied by Chebychev weighting and array response in the Combiner sub-module to generate the DBF output.

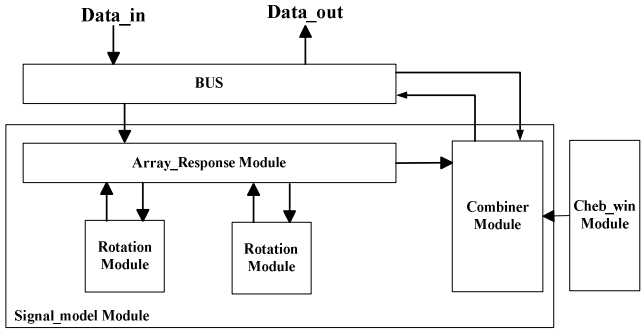


Fig. 5 Hardware structure of Beamforming module

C. Software Design

The circuit modules of the DBF-OFDM transceiver, as shown in Fig. 4, process the data bit-by-bit. The required processing time for each module is one time clock. The pipeline period is a packet length. The sequence controller is designed to control the data processing flow and to enable the FPGA modules. After the processing is completed, the FPGA processing modules are reset and they will send the output enable signals to the sequence controller.

D. Resource Utilization

There are 96 18x18 multipliers and 28672 LUTs in the Xilinx Virtex II xc2v8000-ff1152-4 FPGA chip with the clock rate of 30MHz. The hardware resource utilizations of circuit modules of the DBF-OFDM transceiver are listed in Table 1 and 2 for transmitter and receiver, respectively. For the transmitter, the IFFT, up sampling, and windowing take more hardware resources. For the receiver, CFO, FFT, Channel estimation and Viterbi decoder take more hardware resources.

TABLE I
THE HARDWARE RESOURCE UTILIZATIONS OF TRANSMITTER

module	Slice Flip Flops(93184)	4 input LUTs(93184)
Scambler	13	12
Convolution	13	14
Interleaver	138	196
Mapping	9	14
Pilot_insertion	812	1602
IFFT	8180	8197
Guard_interval	2121	2519
Preamble	30	64
Up_sampling	2621	4147
Windowing	1612	2336
DBF	426	1918

TABLE II
THE HARDWARE RESOURCE UTILIZATIONS OF RECEIVER

module	Slice Flip Flop(93184)	4 input LUTs(93184)
DBF	454	1920
Windowing	1612	2336
CFO	4992	10139
Down_Sampling	278	177
Remove_CP	2121	2518
FFT	6051	7254
Channel est.	3539	12093
Demapping	30	30
Deinterlever	355	789
Decoder	4079	6533

V. CHANNEL MODELS

A. Rayleigh Fading Cannel

The envelope of the *i*th path can be set as a Rician distribution function, which is described in terms of K-factor k_i. If k_i=0 then the probability density function (pdf) of envelope tends to a Rayleigh distribution.

$$P_r(r)=\begin{cases}\frac{r}{\sigma^2}\exp(-\frac{r^2}{2\sigma^2}), & r\ge 0\\ 0 & \text{, otherwise}\end{cases} \quad (16)$$

The pdf of phase is

$$P_\theta(\theta)=\frac{1}{2\pi},\ -\pi<\theta<\pi \quad (17)$$

Jakes spectrum is used as the path spectrum in the fading channel [12].

$$S(f)=\begin{cases}\frac{1}{\sqrt{1-\left(\frac{f}{f_d}\right)^2}} & |f|<0.999f_d\\ 0 & \text{otherwise}\end{cases} \quad (18)$$

, where f_d is the maximum Doppler shift related with the maximum user speed v_m.

$$f_d=v_m f_c/c \quad (19)$$

, where f_c is the carrier frequency and c is the light velocity (3×10^8m/s).

B. DSRC Fading Channel

It is noted that the relative vehicle speed defined in the DSRC specification is 280 km/hr. The rounded spectrum is employed in DSRC channel and defined as

$$S_i(f)=\begin{cases}g\sqrt{1-\left(\frac{f-f_{o_i}}{f_{d_i}}\right)^2} & |f-f_{o_i}|<0.999f_{d_i}\\ 0 & \text{otherwise}\end{cases} \quad (20)$$

, where f_{d_i} is the maximum Doppler shift for the path and f_{o_i} is the Doppler offset. The spectrum is truncated to $0.999f_{d_i}$ in order to avoid singularities.

From the measured Doppler shift $f_{d_i}^{'}$ and offset frequencies $f_{o_i}^{'}$ listed in [13], the measured Doppler shift and offset frequencies for each of twelve paths were both scaled by the input relative vehicle speed v.

$$f_{d_i}=f_{d_i}'\frac{v}{280km/hr},\ i=1,2,...,12 \quad (21)$$

$$f_{o_i}=f_{o_i}'\frac{v}{280km/hr},\ i=1,2,...,12 \quad (22)$$

, where v is the relative vehicle speed between transmitter and receiver.

VI. EXPERIMENTS

A. Test architecture

The test architecture of the DBF-OFDM transceiver is shown in Fig. 6. The users can input the system parameters including data transmission rate, channel condition, vehicle speed and transmitted data type. The DSRC system based on the OFDM technique can provide multiple data rate services. The data transmission rate determines the modulation type (BPSK, QPSK, 16QAM and 64QAM) and channel coding rate (1/2, 2/3 and 3/4) of the transceiver. Each transmitted packet contains 100 OFDM symbols.

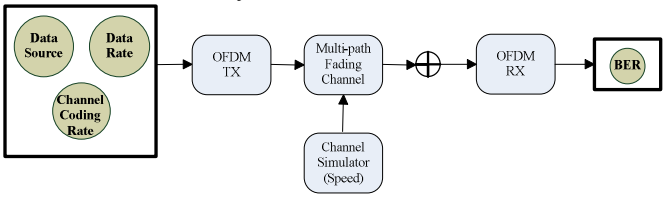
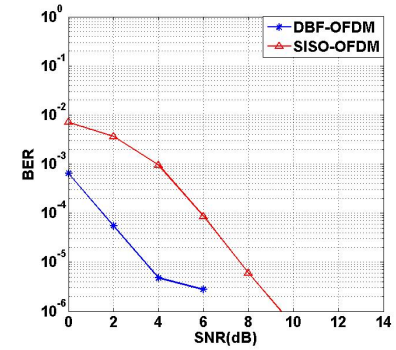


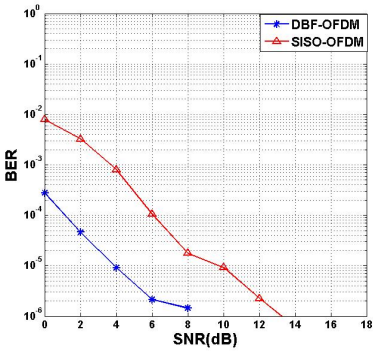
Fig.6 Test configuration

B. Function demonstrations

Two-ray Rayleigh fading channel is chosen to test the BER performance of the DBF-OFDM and SISO-OFDM transceiver. Figure 7(a) shows the BER performance of OFDM transceiver using 16 QAM and 18 Mbps data rate. The user speed is 12km/h and delay spread is 13 *n*s. Figure 7(b) shows the BER performance of OFDM transceiver using 16 QAM and 18 Mbps data rate. The user speed is 120km/h and delay spread is 26 *n*s. Figure 8(a) shows the BER performance of OFDM transceiver using 16 QAM and 18 Mbps data rate. The user speed is 60km/h and delay spread is 26 *n*s. Figure 8(b) shows the BER performance of OFDM transceiver using 16 QAM and 18 Mbps data rate. The user speed is 120km/h and delay spread is 26 *n*s. The test results show that the DBF-OFDM is superior to SISO-OFDM in signal to noise ratio (SNR) gain of about 4 dB. The BER performance for both the DBF-OFDM and SISO-OFDM systems operated in 13 *n*s delay spread is better than 26 *n*s delay spread. The BER performance for both the DBF-OFDM and SISO-OFDM systems operated in 60km/h user speed is better than 120km/h user speed.

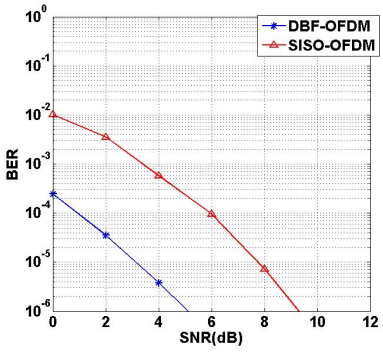


(a)

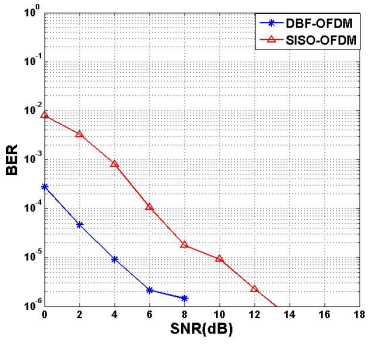


(b)

Fig.7 OFDM BER (a)120km/h, delay spread =13*n*s; (b)120km/h, delay spread =26*n*s



(a)



(b)

Fig.8 OFDM BER (a)60km/h, delay spread =26*n*s; (b)120km/h, delay spread =26*n*s

VII. Conclusions

In this paper, the FPGA chip is applied to the design of a DBF-OFDM transceiver, which leads to an increase of channel capacity, identifies the cars on the highway and improves the BER performance for VPS-ETC applications. The air interface specification of the DSRC system is chosen as an example to compare the BER performance between the DBF-OFDM and SISO-OFDM transceivers. The test results demonstrate that the DBF can greatly improve the BER performance of the DSRC system. In addition, the FPGA hardware resource utilizations of the DSRC system using the DBF will not be increased too much.

Acknowledgment

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