A New Loop-delay Estimation Algorithm for Amplifier Predistortion System

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Abstract—**Predistortion technology is an adaptive, low cost and potential linearization method. Proper loop-delay estimation and compensation are important preconditions for ensuring the predistorter working well. But traditional loop-delay estimation algorithms are vulnerable to the amplifier's memory and nonlinear distortion. In this paper, based on the relationship between the system loop-delay and the amplitude of predistorter error output, we propose a new loop-delay estimation algorithm which improves the algorithm estimation accuracy in memory nonlinear distortion. Simulation results show that the NMSE after the predistortion is very close to the ideal one and a good power spectral density (PSD) performance is achieved. The new algorithm realizes the predistorter and the loop-delay estimation working simultaneously that maintains the reliability and continuity of signal transmission.**

Keywords-Predistorter, Loop-delay estimation, LMS algorithm, Nonlinearity.

I. INTRODUCTION

In recent years, for pursuing a better use of the limited spectrum resource, modern transmission system tends to adapt the non-constant envelope modulation which has higher spectrum utilization efficiency compared with constant envelope modulation. However, the former is more vulnerable to the amplifier nonlinear effect. Therefore, in order to improve the system efficiency, power amplifier (PA) linearization technology is necessary.

Predistortion technology has become one of the most potential linearization technologies because of its outstanding advantages including maintaining original signal spectrum distribution, low cost and adaptive capability. In typical predistortion systems, the predistorter compares the input signal with the feedback signal (Fig. 1), and ensure that the error between this two signals is minimum. However, the loop-delay which exists in practical hardware platform inhibits the convergence of the adaptive algorithm. Therefore the estimation of the loop-delay and a suitable compensation must be made to ensure that the predistortion system could compare the input and feedback signal correctly. The traditional loop-delay estimation algorithms are based on the correlation of the input and output signals of HPA or the spectrum analysis of the delayed signal to estimate the loop-delay.

In [1], Y.Nagata et al. proposed an adaptive loop-delay estimate algorithm. But in this iteration algorithm, the influence of PA nonlinear distortion on the baseband signal was quite significant, which disrupted the accuracy and stability of the loop-delay estimation.

Another estimate algorithm presented by Wright and Durtler [2,3] adopted the fast Fourier transform (FFT). But the computational complexity is large and the processing time is too long. Moreover, due to the application of mark cycle τ , the algorithm is related with system format and the applied range is limited.

In [4], J. Sala et al. proposed a new estimation algorithm using Time-Delay Spectrum (TDS) which improved the reliability and reduced the computing complexity to some extent. However, this estimation only processed the integer times loop-delay and the computational complexity is still high due to the fourth-order cross-correlation.

In [5] Kim and Lee adopted 64 times oversampling rate of the symbol rate to improve the estimation accuracy. But it is impractical in wide-band predistorter.

In [6], by investigating the correlation properties of the input and output signal, AI Bo et al. proposed a universal loop-delay estimate algorithm which was not system format related. In [7], Shigang Tang et al. proposed an adaptive loop-delay estimation algorithm which was suitable for PA nonlinear distortion. However, their studies were mainly in the background of non-memory nonlinear distortion PA models. The feasibility and accuracy of these algorithms in PA memory nonlinear distortion conditions were not involved.

In this paper, aiming at the disadvantages mentioned above, we propose a new algorithm based on analyzing the relationship between the system loop-delay and the predistorter output error amplitude. It is independent of the signal format and is suitable for memory nonlinear distortion. The simulation results show the new algorithm reduces the influence of the loop-delay error on the performance effectively as well as maintains the reliability and continuity of signal transmission

The rest of this paper is organized as follows. In Section II, the relationship between the system loop-delay and the amplitude of predistorter output error are investigated and the system format-free loop-delay estimate algorithm is proposed. The new algorithm realizes the synchronous work of the predistorter and the system loop-delay estimation. In Section III, simulations are presented to evaluate the performance of the new algorithm. Conclusions are given in Section IV.

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II. LOOP-DELAY ESTIMATE ALGORITHM

A. Predistorter Algorithm

In this paper, we select the adaptive predistorter based on look-up table algorithm. The system is constructed by predistortion module and loop-delay correction module (Fig. 1). The operation principle of this predistorter can be described briefly as follow:

1) Memory-Polynomial Predistorter:

The Volterra series is a widely used model to process the PA memory nonlinear distortions. Memory polynomial is one of its common simplified models, which can be expressed as:

$$v_d(n)=\sum_{k=1}^{K}\sum_{q=0}^{Q}a_{kq}v_a(n-q)\left|v_a(n-q)\right|^{k-1} \tag{1}$$

where K is the nonlinear order and Q is the memory depth of the amplifier. a_{kq} is the memory polynomial coefficient. Because the even order intermodulation frequency can be removed by the filter, we only take the odd order nonlinear distortion into account. Hence, expression (1) can be simplified as follow:

$$v_d(n)=\sum_{\substack{k=1\\ Odd}}^{K}\sum_{q=0}^{Q}a_{kq}v_a(n-q)\left|v_a(n-q)\right|^{k-1} \tag{2}$$

where, we supposed $K=5$, $Q=5$. Based on adaptive LMS algorithm, we deduce the memory polynomial update iteration formula as:

$$a_{(k,q)_{p+1}}=a_{(k,q)_p}+\mu\cdot v_a^{*}(n-q)\cdot\left|v_a(n-q)\right|^{k-1}\cdot e(n) \tag{3}$$

where $e(n)=v_m(n)-v_d(n)$, p represents the p-th iteration.

2) Memory-Polynomial Look-up Table Predistorter:

Equation (2) illuminates the memory polynomial predistortor's input/output relationship. For analysis convenience, we rewrite (2) into

$$\begin{aligned}v_d(n)&=\sum_{q=0}^{Q}v_a(n-q)\sum_{\substack{k=1\\ Odd}}^{K}a_{kq}\left|v_a(n-q)\right|^{(k-1)}\\&=\sum_{q=0}^{Q}v_a(n-q)\cdot w_q(v_a(n-q))\end{aligned} \tag{4}$$

where $w_q(v_a(n-q))=\sum_{\substack{k=1\\ Odd}}^{k}a_{kq}\left|v_a(n-q)\right|^{(k-1)}$, when both the input signal amplitudes $\left|v_a(n-q)\right|$ and "q" are fixed value, $\sum_{\substack{k=1\\ Odd}}^{k}a_{kq}\left|v_a(n-q)\right|^{(k-1)}$ becomes a constant. Therefore, (4) can be made into a look-up table (LUT) form, its adaptive updating adopts the adaptive-updating recursive formulas as follow [8]:

$$e(n)=v_m(n)-W_p\cdot V_a^{T}(n) \tag{5}$$

$$W_{p+1}(n)=W_p(n)+\mu\cdot V_a^{*}\cdot e(n) \tag{6}$$

where, $V_a(n)=[v_a(n),v_a(n-1),\cdots,v_a(n-M+1)]$, $W_p(n)=[w_{0,p}(\left|v_a(n)\right|),w_{1,p}(\left|v_a(n-1)\right|),w_{2,p}(\left|v_a(n-2)\right|),\cdots,w_{M-1,p}(\left|v_a(n-M+1)\right|)]$, μ is iteration step-size, $e(n)$ is the error signal between the amplifier input and the predistorter output (with loop-delay). In this paper, the entries of LUT are 64. This predistortion process does not need to solve polynomial coefficients. Therefore, compared with memory polynomial algorithm, it has lower computation complexity and better predistortion performance.

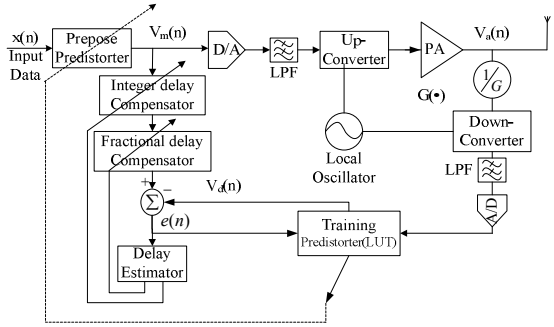


Figure 1. System block diagram

B. The relationship between the system loop-delay and the amplitude of predistorter output error:

By analyzing the relationship between the system loop-delay and the amplitude of predistorter error output, we can conclude: when the loop-delay error gets smaller, the amplitude of predistorter output error becomes smaller as well(Fig. 2), conversely the amplitude of predistorter output error become larger when the loop-delay error gets larger (Fig. 2). So we propose a new loop-delay estimate algorithm which can work with the predistortion algorithm simultaneously. The new algorithm dismisses traditional correlation calculations and linear iterations. Therefore, it is robust to the PA memory distortion and applies to both PA memory and non-memory nonlinear distortion conditions.

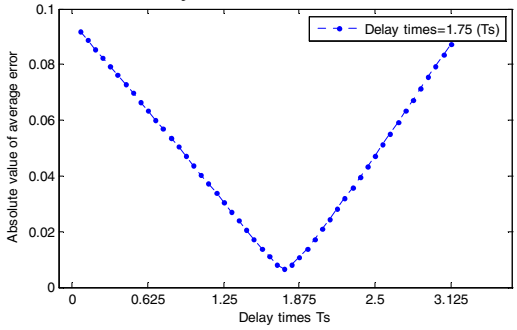


Figure 2. System loop-delay and amplitude of predistorter error output diagram (Loop-delay= 1.75 Ts).

C. Loop-delay Estimation algorithms

Loop-delay algorithm can be divided into two parts: integer loop-delay and fraction loop-delay.

1) Integer loop-delay algorithm:

When each predistortion process is finished, the system can get predistortion error from (5) , then substitute it into (7) and (8) yields the integer loop-delay estimation:

$$d_n = d_{n-1} + K \cdot e \tag{7}$$

$$Delay = \mathrm{int}(|d_n|) \tag{8}$$

where n is the number of predistortion iterations, d_n presents the estimated integer loop-delay value, K is iteration compensation (in this paper, K=1). In (8), int( ) is defined as to round $|d_n|$ to the nearest integer. From (7) and (8), the algorithm can estimate the integer loop-delay and begin the next predistortion computing with new delay compensation value. After several iterations, the final integer delay estimate is acquired. The convergence performance is shown in Fig. 3: after the join operation of about 1000 points, the new algorithm can converge at integer estimate d_k=3T_s point (T_s is the sampling period).

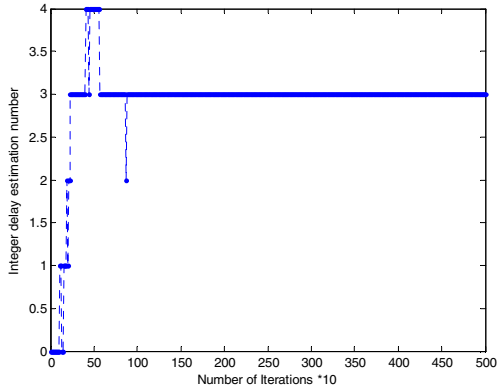


Figure 3. Integer loop-delay convergence diagram.

2) Fraction loop-delay algorithm:

When the integer loop-delay estimation and compensation are finished, the system turns to the fraction loop-delay estimation.

Firstly, the estimation algorithm sets initial LUT to zero and determines the iteration direction. According to (5) and (9),the predistorter calculates output error average amplitude of loop-delay=0.1 and loop-delay=-0.1. The smaller value $|\bar{e}_{dir}|_{delay}$ is selected as the iteration direction defined as direction A (the reverse iteration direction is defined as B). We set M=1000 for calculation accuracy.

$$|\bar{e}_{dir}|_{delay} = \sum_{n=1}^{M} |e(n)|_{delay} \Big/ M \tag{9}$$

Secondly, in order to make the fraction loop-delay estimation approach to the reality loop-delay, the LUT are initialized again and the algorithm makes progressive interpolation towards to direction A by step $\Delta = 0.1$Ts based on (10) and compensates the loop-delay by interpolation filter. After each loop-delay step compensation, the algorithm calculated new average amplitude of the predistorter error based on (11) with the new loop-delay step value.

If $|\bar{e}(k)| - |\bar{e}(k-1)| \le 0$, the algorithm will repeat the former step and keep the iteration direction to approach the reality loop-delay continuously. Once $|\bar{e}(k)| - |\bar{e}(k-1)| > 0$ which indicates the excessive delay compensation, the algorithm will adjust the iteration step: $\Delta = 0.1$*Ts/2 according to (10) and make reverse direction B iteration. After several iterations, the fraction loop-delay is estimated and corresponding compensation is made to eliminate the system loop-delay.

$$delay(k+1) = \begin{cases} delay(k) + \Delta \cdot 0.1Ts & (|\bar{e}(k)| - |\bar{e}(k-1)| \le 0) \\ delay(k) - \Delta \cdot 0.1Ts/2 & (|\bar{e}(k)| - |\bar{e}(k-1)| > 0) \end{cases} \tag{10}$$

$$|\bar{e}(k)| = \sum_{n=(k-1)\cdot M+1}^{k\cdot M} |e(n)|_{delay(k)} \Big/ M \tag{11}$$

where $\Delta = sign[|\bar{e}_{dir}|_{delay=-0.1Ts} - |\bar{e}_{dir}|_{delay=0.1Ts}]$, $delay(1)=0$, k =1,2…n/M, $|\bar{e}(0)| = +\infty$. We remark that the estimated fraction loop-delay amplitude is similar to that of the reality but it has opposite sign due to the usage of interpolator inverse compensation.

The fraction loop-delay compensation is realized by using a 4-tap piecewise-parabolic interpolation filter which can sum all the positive and negative fraction loop-delays to generate a positive fraction loop-delay compensation value.

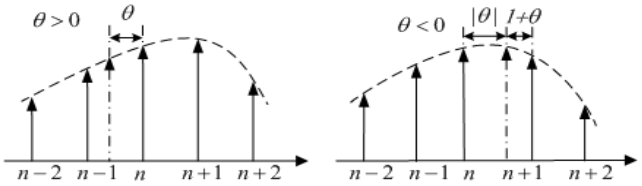


Figure 4. Positive and negative fraction loop-delays.

The widely used 4-tap piecewise-parabolic interpolator is

$$y_{in}(n) = \begin{cases} \sum_{i=-2}^{1} a_i(\theta) x_{in}(n+i) & (\theta>0) \\ \sum_{i=-2}^{1} a_i(1+\theta) x_{in}(n+1+i) & (\theta<0) \end{cases} \tag{12}$$

where x_{in} denotes the real part of complex form input signal $x_d(n)$, y_{in} denotes the delay signal generated by x_{in} passing the interpolation filter. $a_i(\theta)$ can be described as follow:

$$\begin{cases} a_1(\theta) = \alpha\theta^2 - \alpha\theta \\ a_0(\theta) = -\alpha\theta^2 + (\alpha-1)\theta + 1 \\ a_{-1}(\theta) = -\alpha\theta^2 + (\alpha+1)\theta \\ a_{-2}(\theta) = \alpha\theta^2 - \alpha\theta \end{cases} \tag{13}$$

where α is the default coefficient which is $\alpha = 0.25$ in this paper. θ is the fraction loop-delay estimate. Because the amplitude variation in adjacent sampling points are very small, so we can get the approximate expression[9]-[11]:

$$x_{in}(n+1) - x_{in}(n) \approx x_{in}(n-1) - x_{in}(n-2) \tag{14}$$

By substituting (13) and (14) into (12), we have

$$y_{in}(n)=\begin{cases}\theta\cdot(x_{in}(n-1)-x_{in}(n))+x_{in}(n)\\(1+\theta)\cdot(x_{in}(n)-x_{in}(n+1))+x_{in}(n+1)\end{cases} \quad (15)$$

III. SIMULATION RESULTS

To evaluate the proposed new algorithm, a simulation is constructed using 16QAM-modulated baseband signal with 8 times up-sampled, a raised-cosine pulse with a 0.25 roll-off factor and an odd-order-only memory polynomial mode as the amplifier. The amplifier mode can be described as below:

$$y(n)=\sum_{\substack{p=1\\p_{odd}}}^{P}\sum_{q=0}^{Q}a_{pq}x(n-q)\left|x(n-q)\right|^{p-1} \quad (16)$$

where, P is the polynomial odd-order and Q is the amplifier memory depth. In this paper, we set P=5, Q=2 and the coefficients are [12]:

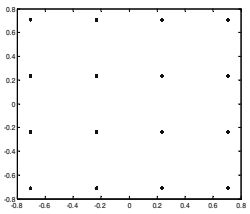
$$\begin{aligned}&a_{10}=1.0513+0.0904j && a_{30}=-0.0542-0.2900j\\&a_{50}=-0.9657-0.7028j && a_{11}=-0.0680-0.0023j\\&a_{31}=0.2234+0.2317j && a_{51}=-0.2451-0.3735j\\&a_{12}=0.0289-0.0054j && a_{32}=-0.0621-0.0932j\\&a_{52}=0.1229+0.1508j\end{aligned} \quad (17)$$

and the NMSE value of the recursive algorithm is defined as:

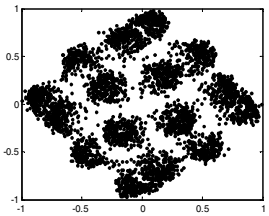
$$NMSE(dB)=10\log_{10}\left[\frac{\sum_{n=1}^{M}|v_m(n)-v_a(n)|^2}{\sum_{n=1}^{M}|v_m(n)|^2}\right] \quad (18)$$

A. Constellation

Fig. 5 (a) shows the constellations of original signal. Fig. 5 (b) is the output signal without predistortion. We can see that the distortion is obvious when original signal goes through the amplifier without predistortion. Fig. 5 (c) shows the output signal with predistortion and the loop-delay =1.75 Tsample(Ts). We can see though the output signal amplitude expansion caused by PA nonlinearity is corrected by predistortion, the expansion caused by loop-delay error still exists and deteriorate the system performance. Fig. 5 (d) is output signal with both predistortion and loop-delay compensation. The figure shows when the predistorter work with loop-delay estimation algorithm simultaneously, both the amplitude distortion and the phase distortion of the output signal constellation are corrected and the constellation are closer to the original signal constellation. Thus, the new algorithm has made excellent loop-delay compensation.



(a)



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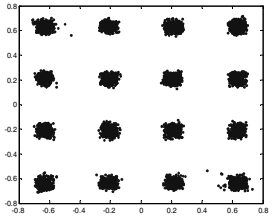
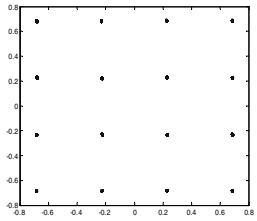


(c)



(d)

Figure 5. (a) original signal constellation (b) constellation without predistortion (c) constellation with predistortion, loop-delay=1.75 Tsample (d) constellation with both predistortion and loop-delay compensation

B. Power Spectral Density Improvement

Fig. 6 illustrates the signal out-of-band power spectral density(PSD). We can observe that even when the output signal is processed by predistorter, the spectral regrowth phenomenon caused by loop-delay is still obvious in Fig. 6 (a) and (b). Fig.6(c) shows the HPA output signal PSD figure without predistorter processing and the loop-delay influenced. Fig.6 (d) shows that the memory-polynomial LUT Predistorter algorithm has certain ability to correct loop-delay, if the loop-delay error is smaller than 0.1Ts. Fig. 6 (e) represents the signal out-of-band power spectral density figure of HPA with both predistortion and loop-delay compensation, compared with Fig. 6(a) and (b), this new algorithm can reduce the signal out-of-band spectral regrowth by 25dB.

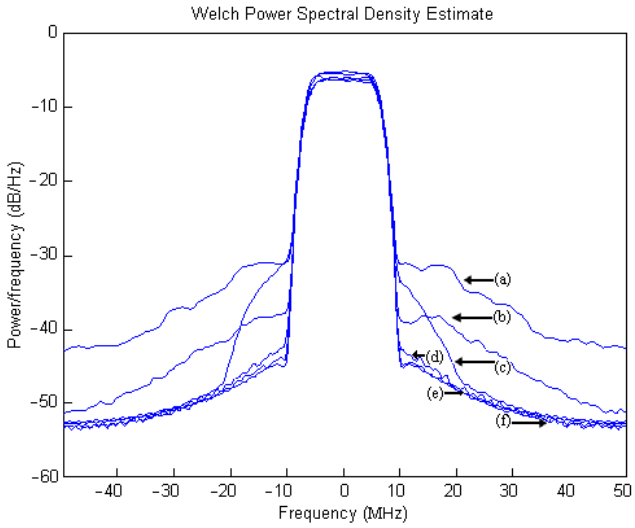


Figure 6. Signal out-of-band power spectral density of HPA output (a) with predistortion, loop-delay =3.15 Ts (b) with predistortion, loop-delay =1.75 Ts (c) without predistortion, loop-delay =0 Ts (d) with predistortion, loop-delay =0.1 Ts (e) with predistortion and loop-delay compansation (f) ideal PSD.

C. Convergence Performanc

In practical application, the characteristics of HPA will drift because of the variance of the environmental temperature and transmission channel. Therefore, adaptive algorithm is needed to track this kind of drift. Fig. 7 shows NMSE curves of predistortion algorithm with loop-

delay=3.15, 1.75 and 0.1 respectively. In Fig. 7 loop-delay=3.15 and 1.15 conditions, the predistorter is influenced by loop-delay severely, the performance is decreased by nearly -20 to -30dB. The small loop-delay (delay=0.1) can also influence the predistorter, the performance is decreased by 3dB. When the loop-delay (e.g. 1.75Ts) is well corrected, the improved NMSE performance is consistent with ideal conditions (Fig. 7 w/o loop-delay). Therefore, the proposed loop-delay estimate algorithm has good NMSE performance and can maintain the integrality and continuity of signal transmission.

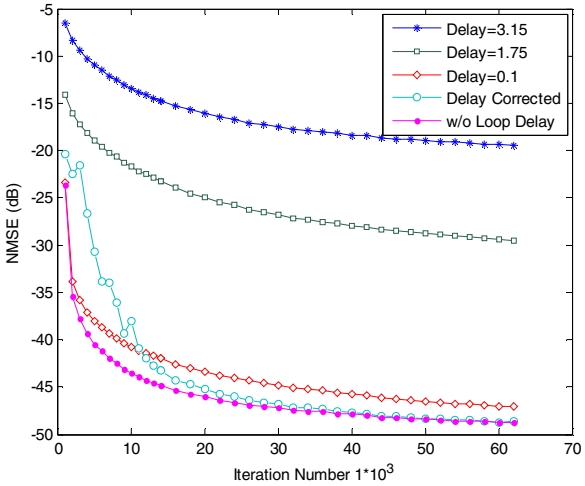


Figure 7. NMSE curve of predistortion algorithm with different loop-delay conditions.

IV. CONCLUSION

Loop-delay estimation is critical for ensuring the efficiency of predistortion system. However, when HPA memory nonlinear distortion exists, the accuracy of predistorter loop-delay estimation algorithm decreased. In this paper, a new algorithm is proposed. By analyzing the relationship between the system loop-delay and the amplitude of predistorter output error. The new algorithm changes traditional loop-delay judging standard and realizes the predistorter and the system loop-delay estimation working simultaneously. This optimization reduces the influence of the loop-delay error on the performance of predistorter effectively as well as maintains the reliability and continuity of signal transmission, which has a high application value.

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