Resource Block Basis MMSE Beamforming for Interference Suppression in LTE Uplink

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***Abstract*—Mobile operators are facing rapid increase in data traffic recently, and so they have much interest in picocells and femtocells which can significantly improve network capacity. Deploying picocells and femtocells, however, can potentially cause inter-cell interference in case of co-channel operation. We have studied the interference suppression method using array antenna system for the 3GPP Long Term Evolution (LTE) uplink based on Minimum Mean Square Error (MMSE) beamforming. This paper proposes a new method to calculate the MMSE weight in a Resource Block (RB) basis. The proposed method has an advantage that the calculation does not require information on either resource allocation of interfering mobile stations or scheduling algorithm processed in the upper layer. An additional advantage of this RB-basis method is parallelization and scalability for symmetric multi-core processing, which is one of potential technologies for software defined radio (SDR) implementation. We have successfully implemented the proposed method on System-on-Chip consisting of multi-core DSP (Digital Signal Processor) and ARM microprocessors and verified that it successfully suppresses interference in real time.**

***Index Terms*—antenna array, interference suppression, timing offset estimation, Evolved UTRA, Long Term Evolution, femtocell, picocell, Multi-Core DSP, software defined radio**

I. INTRODUCTION

Long Term Evolution (LTE) was recently standardized by the 3rd Generation Partnership Project (3GPP) as the successor of the Universal Mobile Telecommunication System (UMTS). The Evolved UMTS Terrestrial Radio Access (E-UTRA), which is the radio access system in the LTE, uses the maximum channel bandwidth of 20MHz and supports a peak data rate of up to 300Mbps and 75Mbps in downlink and uplink, respectively. Orthogonal Frequency Division Multiple Access (OFDMA) and Single-Carrier Frequency Division Multiple Access (SC-FDMA) are employed in downlink and uplink for LTE, respectively [1].

Recently, operators are facing enormous traffic demand by explosive growth of smartphones. To overcome this challenge, heterogeneous network (HetNet) has been discussed in the 3GPP, which is a network consisting of different types of cells such as macrocells, picocells and femtocells, and it can significantly increase the network capacity. While HetNet offers the significant advantages, co-channel operation between macrocell and picocell/femtocell can cause severe inter-cell interferences. Fig. 1 shows the interference from macrocell Mobile Station (MS) to femtocell Base Station (BS). The solution to the interference is also under discussion in the 3GPP, by the name of HetNet inter-cell interference coordination (HetNet ICIC), and it coordinates the resource allocation between cells in frequency domain to avoid the interference. However, the coordination inevitably causes a degradation of data rates for users.

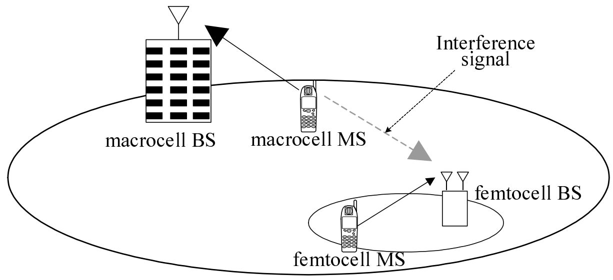

Fig. 1. Interference from macrocell MS to femtocell BS

To solve this problem, we have studied an interference suppression technique for base station in uplink using array antenna system based on MMSE beamforming. Unlike HetNet ICIC, this approach addresses the uplink interference issue in space domain, and thus, does neither cause a degradation of data rates in uplink nor require any communications between cells.

In SC-FDMA or OFDMA system, the optimum MMSE weight varies by time and frequency because resources for both communicating and interfering MSs vary by time and frequency. This paper presents a method to calculate the MMSE array weight by basic time-frequency resource available for data transmission which is called Resource Block (RB) in LTE. The proposed method does not require information on either resource allocation for the interfering MSs or scheduling algorithm processed in medium access control (MAC) layer because it is assured that resources for the communicating and the interfering MSs do not vary within an RB. Moreover, its implementation is done for only physical (PHY) layer and any message between MAC and PHY layers is not required for this method.

There almost always exists an offset between ideal and actual Fast Fourier Transform (FFT) symbol timing in SC-FDMA or OFDM system. The MMSE weight is incorrectly calculated due to phase rotation introduced by the timing offset, and it needs to be compensated. Unfortunately, the

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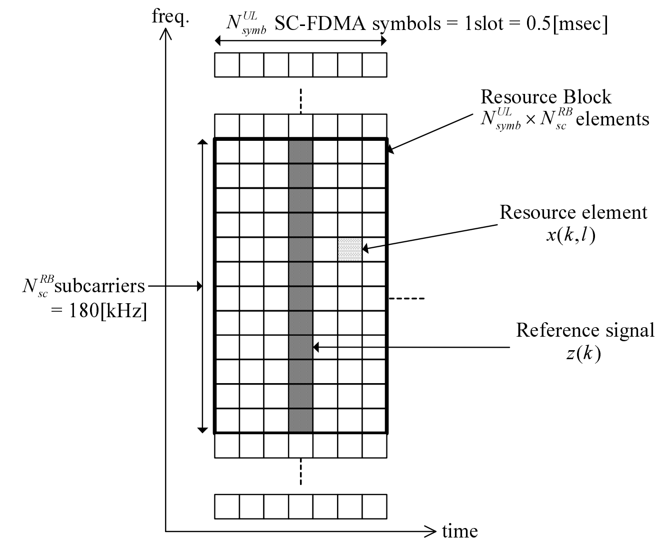

Fig. 2. Resource Block for PUSCH

number of available data points in an RB is limited and insufficient for conventional method to compensate the timing offset. This paper also introduces a new iterative timing offset compensation method based on alternating projection [2] to enable effective interference suppression in the RB-basis strategy in the presence of the timing offset.

We evaluated the feasibility and the performance of the proposed method using Mindspeed Transcede®4000 SoC platform consisting of multi-core DSPs. To achieve real-time processing, we modified task scheduling on the platform based on the results of some validation. Experimental results show that the proposed algorithm successfully suppresses interference without Transmission-Time-Interval (TTI) violation.

II. Resource Block Basis MMSE Array Processing for LTE Uplink

A. RB-basis Processing

As mentioned in the introduction, LTE uplink transmission is based on SC-FDMA. Thus the resources for uplink transmission are represented by a time-frequency resource grid in which each resource element corresponds to one SC-FDMA subcarrier. These resource elements are grouped into Resource Blocks (RBs) which consist of $N_{\mathrm{sc}}^{\mathrm{RB}}$ consecutive subcarriers in frequency domain and $N_{\mathrm{symb}}^{\mathrm{UL}}$ consecutive symbols in time domain [3]. In LTE uplink, $N_{\mathrm{sc}}^{\mathrm{RB}}$ is always twelve and $N_{\mathrm{symb}}^{\mathrm{UL}}$ is six or seven, which depends on Cyclic Prefix (CP) configuration. Fig. 2 shows the time-frequency grid in an RB for physical uplink shared channel (PUSCH) of the LTE uplink. When using MMSE based array processing for LTE uplink, we calculate an MMSE weight in an RB-basis because the interfering MS varies by RB. This "by-RB" strategy does not require the knowledge of resource allocation of either the interfering MSs or communicating MSs. Furthermore, it allows parallel processing and scalability for multi-core processing, and thus enables effective computation.

In the proposed approach, the frequency-domain signals are grouped into RBs after FFT operation, and MMSE array processing is performed. Then the output of the MMSE array processor using P antenna elements at the k-th subcarrier and the l-th symbol in an RB $y(k,l)$ is expressed as

$$y(k,l) = \boldsymbol{w}_{\mathrm{MMSE}}^{H}(k)\ \boldsymbol{x}(k,l), \tag{1}$$

where $\boldsymbol{x}(k,l)$ is the $(P \times 1)$ received resource element vector at the k-th subcarrier and the l-th symbol in the RB, $\boldsymbol{w}_{\mathrm{MMSE}}(k)$ is the MMSE weight vector at the k-th subcarrier of the RB, and $(\cdot)^H$ denotes the Hermitian operator. Here k and l are frequency and time indexes in an RB, respectively, where $0 \leq k < N_{\mathrm{sc}}^{\mathrm{RB}}$ and $0 \leq l < N_{\mathrm{symb}}^{\mathrm{UL}}$.

The MMSE weight at the k-th subcarrier is the solution to the following unconstrained non-linear optimization problem:

$$\boldsymbol{w}_{\mathrm{MMSE}}(k) = \arg\min_{\boldsymbol{w}(k)} E[|s(k) - \boldsymbol{w}^H(k)\boldsymbol{z}(k)|^2], \tag{2}$$

where $E[\cdot]$ is an expectation operator, $s(k)$ is the transmitted reference signal at the k-th subcarrier in the RB, and $\boldsymbol{z}(k)$ is the received reference signal at the k-th subcarrier in the reference symbol, which is given by $\boldsymbol{z}(k) = \boldsymbol{x}(k, N_{\mathrm{symb}}^{\mathrm{UL}} - 4)$ for PUSCH.

Note that $\boldsymbol{w}(k)$ is not frequency-invariant. Adaptive algorithms such as LMS and RLS are often used for variant system identification, but they are ineffective in the RB-basis processing because only twelve data points are available in an RB and they are absolutely insufficient to converge.

B. Weight Calculation

In practical situations, there almost always exists a timing offset between the ideal and actual FFT symbol timing because of coarse timing adjustment granularity, sampling clock error between the base station and the mobile stations, movement of the mobile stations, and attenuation or vanishment of path due to change of the channel condition. The timing offset introduces phase rotation in frequency domain. In an RB bandwidth, the frequency-variation of $\boldsymbol{w}(k)$ is caused by mainly this phase rotation, rather than multipath environment.

Here we apply some restriction for $\boldsymbol{w}(k)$ and rewrite Eq. (2) as

$$\boldsymbol{w}_{\mathrm{MMSE}}(k) = \arg\min_{\boldsymbol{w},\phi} E[|s(k) - \boldsymbol{w}^H e^{-j\phi k}\boldsymbol{z}(k)|^2], \tag{3}$$

where ϕ denotes magnitude of the phase rotation per subcarrier and is given by $\phi = 2\pi\Delta f \cdot \tau$ where Δf and τ denotes the subcarrier spacing and the timing offset of the MS assigned to the RB, respectively. In Eq. (3), the weight $\boldsymbol{w}(k)$ is factorized into frequency-invariant weight $\boldsymbol{w}$ and timing offset compensator $e^{-j\phi k}$. This restriction implies that channel condition within RB bandwidth ($= 180$[kHz]) is flat. Here, we propose a new method to calculate the MMSE weight based on alternating projection. The alternating projection is a simple technique for multidimensional minimization, which iteratively optimizes one factor at a time, fixing all the other factors. In the proposed method, the frequency-invariant weight $\boldsymbol{w}$ and the compensator $e^{-j\phi k}$ are optimized independently and iteratively. First, the frequency-invariant weight $\boldsymbol{w}$ is conventionally calculated as

$$\boldsymbol{w} = \boldsymbol{R}^{-1}\boldsymbol{r}, \tag{4}$$

where $\boldsymbol{R}$ $(P \times P)$ and $\boldsymbol{r}$ $(P \times 1)$ are the auto-correlation matrix of received reference signals and the cross-correlation vector between received and transmitted reference signals [4]. In Eq. (3), regarding ϕ as fixed value, then $\boldsymbol{R}$ and $\boldsymbol{r}$ are estimated using summations as

$$\boldsymbol{R} = \sum_{k=0}^{N_{\rm sc}^{\rm RB}-1} \boldsymbol{z}(k)\boldsymbol{z}^H(k) + \delta \boldsymbol{I}, \tag{5}$$

and

$$\boldsymbol{r} = \sum_{k=0}^{N_{\rm sc}^{\rm RB}-1} e^{-j\hat{\phi}k}\boldsymbol{z}(k)s^*(k), \tag{6}$$

where $(\cdot)^*$ denotes the conjugate operator, δ and $\boldsymbol{I}$ in Eq. (5) denote pseudo-noise power and identity matrix respectively. The pseudo-noise power is determined so as to avoid numerical instability of the matrix inverse. At the initial iteration, the estimation of rotation $e^{-j\hat{\phi}}$ in Eq. (6) is set to unity, otherwise, set to the estimate in the previous iteration.

After the frequency-invariant weight calculation, the timing offset estimation is carried out. Regarding $\boldsymbol{w}$ as fixed value, Eq. (3) is expressed as

$$\boldsymbol{w}_{\rm MMSE}(k) = \boldsymbol{w}\ e^{j\hat{\phi}k} \tag{7}$$

$$\hat{\phi} = \arg\min_{\phi} E[|1 - e^{-j\phi k}A(k)|^2], \tag{8}$$

where $A(k)$ is given by $A(k) = \boldsymbol{w}^H\boldsymbol{z}(k)/s(k)$. Obviously the above problem is a sinusoidal frequency estimation of $A(k)$. Several well-known methods such as MUSIC and ESPRIT[5] are often used for the estimation, but they require a complicated and expensive computation. Here we devise the following simple method using auto-correlation coefficients based on least squares:

$$\exp(j\hat{\phi}) = \boldsymbol{\rho}_x^+\boldsymbol{\rho}_y = \frac{\boldsymbol{\rho}_x^H\boldsymbol{\rho}_y}{\|\boldsymbol{\rho}_x\|^2}, \tag{9}$$

where $(\cdot)^+$ denotes the Moore-Penrose generalized inverse operator. Here $\boldsymbol{\rho}_x$ and $\boldsymbol{\rho}_y$ are defined as $\boldsymbol{\rho}_x = [\rho_0, \cdots, \rho_{M-1}]^T$ and $\boldsymbol{\rho}_y = [\rho_1, \cdots, \rho_M]^T$, where ρ_m $(m = 0, 1, \cdots, M)$ is auto-correlation of $A(k)$ and expressed as

$$\rho_m = \frac{1}{N_{\rm sc}^{\rm RB} - m} \sum_{k=0}^{N_{\rm sc}^{\rm RB}-m-1} A^H(k)A(k+m), \tag{10}$$

where $M < N_{\rm sc}^{\rm RB}$. We set $M = 4$ in our implementation because our simulation results show the larger values do not improve the estimation.

Fig. 3 shows the block diagrams of the proposed algorithm. In the proposed method, the weight calculation and timing offset estimation are iteratively performed. The estimation calculated in Eq. (9) is used as compensator in Eq. (6) at the next iteration. This algorithm suppresses the interference in the presence of timing offset with only twelve data points.

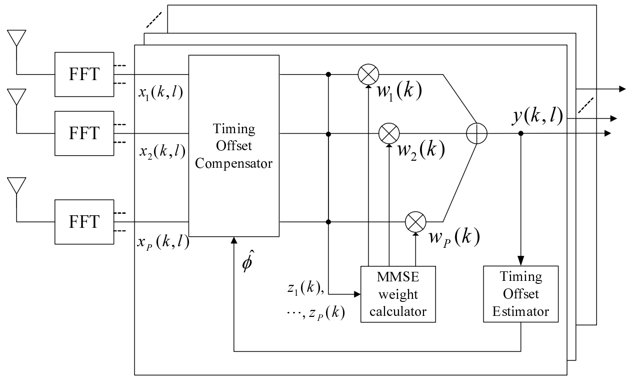

Fig. 3. MMSE array processor for LTE uplink

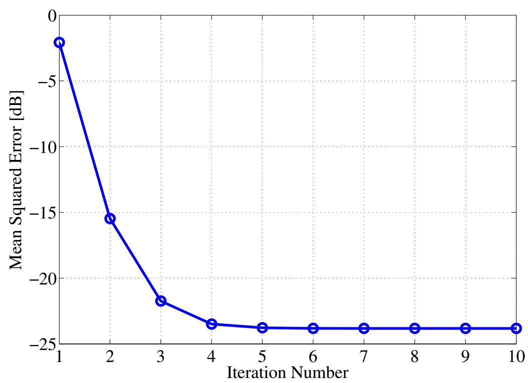

Fig. 4. Convergence of mean squared error between $y(k, N_{\rm symb}^{\rm UL} - 4)$ and $s(k)$ in the case of $P = 2$

Fig. 4 shows an example of the convergence of mean squared error between the reference signal $s(k)$ and the array output at the reference symbol $y(k, N_{\rm symb}^{\rm UL} - 4) = \boldsymbol{w}_{\rm MMSE}^H(k)\boldsymbol{z}(k)$ in the iterations, from a simulation in the case of timing offset of half a CP ($\simeq 2.3[\mu s]$). We see that the estimation error monotonically decreases with iterations and converges in five iterations. The additional advantage of the proposed algorithm is controllability of trade-off between estimation accuracy and computational effort. This controllability is suitable for software implementation, because available computational capability depends on processor's performance and load unlike hardware implementation. When processor has poor performance or its load is high, the number of iterations is limited to 1. In contrast, when we have rich processing performance or low load, then we can iterate several times.

III. Hardware Architecture

A. SoC Architecture

The Transcede®4000 chip of Mindspeed Technologies, Inc., which is one of the most promising baseband processors for the next generation wireless systems, consists of six ARM Cortex™-A9 microprocessors, ten CEVA-X1641™DSP cores, and other coprocessors such as FFT and FEC. The

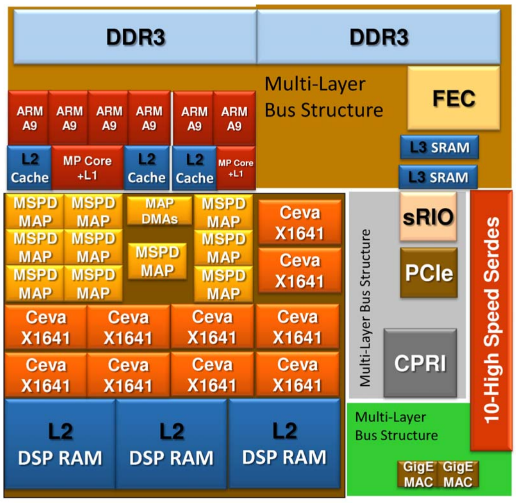

Fig. 5. Transcede®4000 architecture

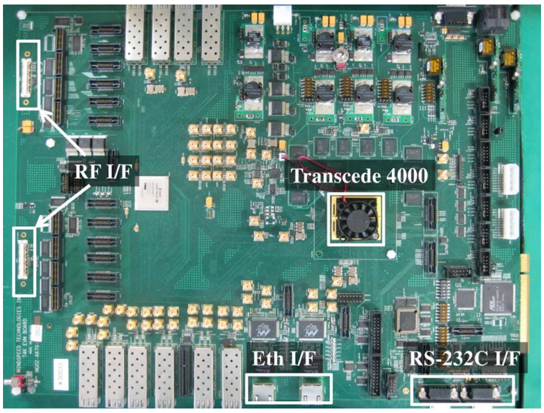

Fig. 6. Transcede®4000 Evaluation Board

architecture is shown in Fig. 5. Frequencies of the DSP and the ARM are set to 500MHz and 600MHz, respectively. CEVA-X1641™DSP has a mix of Very Long Instruction Word (VLIW) and Single Instruction Multiple Data (SIMD) architectures, and C programmability. Each DSP core has 96[KBytes] code memory and 128[KBytes] data memory as L1, and three 1[MByte] L2 DSP RAM memories reside in the chip. For the receiver (uplink), the incoming baseband I and Q signals from RF modules are stored in the L2 memories per subframe which is a transmission unit consisting of 2 slots in LTE. Then the data are first DMA-transferred to MAP processor in Fig. 5, FFT is performed, and the output is transferred back to the memory. In the same manner, the demodulation tasks following FFT are performed on DSPs in parallel. Each task is performed as the scheduler dispatches, which is run on one ARM core.

B. Evaluation Board

Fig. 6 shows Evaluation Board for the Transcede®4000. The board mounts serial ports and Ethernet ports. Host-PC controls the board via the serial ports, and the Ethernet is used for packet data transfer. The intermediate data in PHY layer such as constellation are probed via the ports. There are two independent RF interfaces in this board, and consequently the number of antennas P is 2 in the MMSE algorithm.

TABLE I
COMPARISON BETWEEN TASK GRANULARITIES

The number of used cores	1	8	8
The number of divided MMSE tasks	1	100	8
Processing time [μs]	1518	723	270

IV. SOFTWARE IMPLEMENTATION

For the implementation, we used LTE PHY stack provided by Mindspeed Technologies, Inc. and replaced its PUSCH demodulation task with our MMSE algorithm.

As mentioned in above section, the weight calculation is performed in RB-basis and in parallel. However, through experiments, it was found that DMA-transfer in RB-basis incurs nonnegligible overhead. Then we DMA-transfer the data per quarter of whole bandwidth of one slot in order to reduce the overhead, and that is, we divide whole processing into eight tasks per one subframe, because at maximum, eight DSPs are available in parallel. (Two of ten DSPs are always occupied by other tasks such as random access channel receiver.) The above also indicates the flexibility of the proposed method. We can freely change granularity of the calculation and construct the task structure according to chip architecture and performance. Table I shows the comparison of processing times between task granularities. For the purpose of reference, we show the case where all the processing is performed on single core in the first column. In this case, the processing time exceeds 1 millisecond TTI of LTE and real-time processing is unachievable. The second column shows the case where total 50×2 RBs in 2slots (= 1 subframe) are completely divided into 100 tasks and each task runs on one of eight cores, and the last column shows the case where we divide the total processing into eight tasks as state above. We see that owing to the overhead reduction, the case of 8 tasks requires much less time than the one of 100 tasks, and the optimization of granularity is successfully performed.

Total code size of the MMSE program is approximately 8[KBytes], and sufficiently small to be located in L1 code memory.

V. EVALUATION

We evaluated the MMSE algorithm using the environment depicted in Fig. 7. The signal generators, multichannel emulator, and RF board are connected via coaxial cables. Table II shows the evaluation specifications. The desired signal generator and the interference one transmit LTE uplink signal and AWGN signal, respectively. The ratio of carrier to interference power (CIR) is set to 3[dB] in the multichannel emulator. The emulator combines the signals with a fixed phase rotation to provide an arrival angular difference between desired and interference MSs. Error vector magnitude (EVM) and constellation diagram of the MMSE array output are

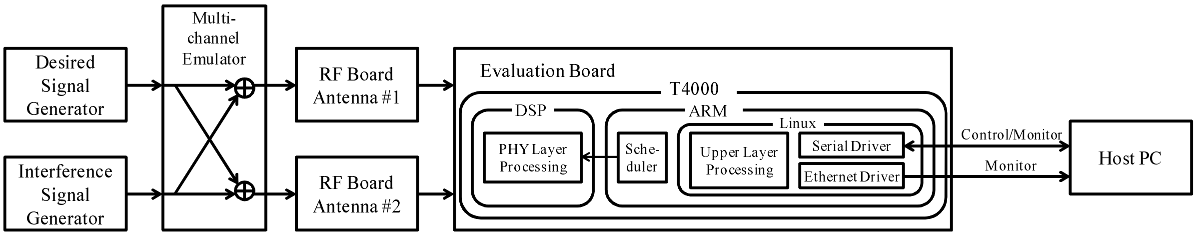

Fig. 7. Diagram of evaluation environment

TABLE II
SYSTEM PARAMETERS

Number of BS antennas ($=P$)	2
BS antenna element spacing	0.5 wavelength
Number of interfering MSs	1
Carrier frequency	2.1 [GHz] (E-UTRA Band1)
System bandwidth	10 [MHz]
Sampling frequency	15.36 [MHz]
CP configuration	Normal CP
Modulation	64QAM
Physical channel	PUSCH
Ratio of carrier to interference power	3 [dB]
Arrival angular difference between MSs	20 [deg]

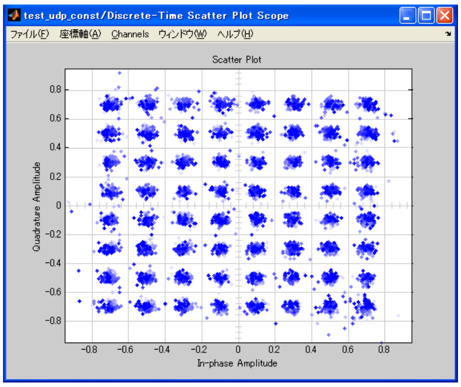

Fig. 8. Constellation diagram for MMSE array output

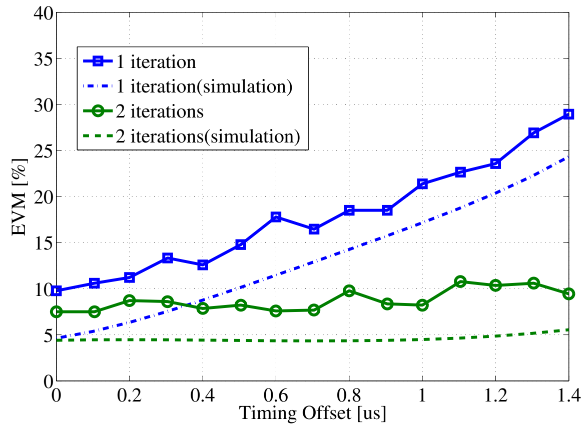

Fig. 9. Relationship between timing offset and EVM

monitored on the Host-PC. In the MMSE algorithm, the pseudo noise in Eq. (5) and the number of iterations are $\delta = (received\ power)/512$ and 1, respectively. We performed test using the above parameters, then we had EVM = 9.7[%]. Under the condition of CIR=3[dB], the theoretical EVM at receiver is approximately 50[%] when conventional maximum ratio combining (MRC) is used. Thus this experimental result represents that the proposed method outperforms the MRC in the presence of interference. The constellation diagram of the array output is also shown in Fig. 8. We see that the interference suppression is achieved under such severe interference. Through the evaluation, TTI violation was not observed, and therefore we conclude that the interference suppression works successfully and real-time processing is achieved. Next, to evaluate an effectiveness of the iteration, we intentionally delayed the start timing of the signal generator. Fig. 9 shows relationship between the timing offset and EVM in the cases of 1 and 2 iterations. We see that the iteration significantly improves the performance when the timing offset is large. We also see that there are biases from the simulation results in the both cases. It is thought to be due to the thermal noises added on the emulator and the RF boards.

VI. CONCLUSION

This paper presented an interference suppression method using an RB-basis MMSE beamforming for LTE uplink and its implementation on multi-core DSP. Through evaluation results, we have shown that the proposed method successfully suppresses interference in real time and is effective against timing offset. The proposed method also has significant advantages in terms of ease of implementation, effective computation on multi-core processor, and adaptive flexibility.

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