Direct Learning Predistorter with A New Loop Delay Compensation Algorithm

Zhengdai Li, Jingming Kuang and Nan Wu
Dept. of Electronic Engineering
Beijing Institute of Technology
Beijing, 100081, P. R. China

***Abstract*—Digital baseband predistortion technology can effectively reduce the system nonlinear distortion. However, the predistortion algorithms based on indirect structure are sensitive to measurement noise and the traditional loop-delay estimation algorithms are vulnerable to the amplifier's nonlinear distortion especially in the amplifier saturation region. In this paper, we first present an adaptive nonlinear predistorter based on direct learning structure and then propose a new loop-delay estimation algorithm which applies to PA nonlinear distortion conditions by analyzing the relationship between the system loop-delay misalignment and the amplitude of HPA model identification error output. Simulation results show that the power spectral density (PSD) after the predistortion is very close to that of the ideal signal and a good NMSE performance is achieved.**

Keywords-Loop delay estimation, Predistorter, RLS algorithm, Nonlinearity

I. INTRODUCTION

In communication system, High Power Amplifier (HPA) is usually set to work near the saturation point to improve the system amplifying efficiency. However, such case will lead to nonlinear distortions of signals. Over the past decade, research on memoryless nonlinear distortion of HPA has made great progress. Predistortion technology has become one of the most potential linearization technologies because of its outstanding advantages including maintaining original signal spectrum distribution, low cost and adaptive capability. In typical predistortion systems, the predistorter compares the input signal with the feedback signal, and ensure that the error between this two signals is minimum.

However the loop-delay existed in practical hardware platform inhibits the convergence of the adaptive algorithm. Therefore the estimation of the loop-delay and a suitable compensation must be made to ensure that the predistortion system could compare input and feedback signal correctly. The traditional loop-delay estimation algorithms are based on the correlation of the input and output signals of HPA or the spectrum analysis of the delayed signal to estimate the loop-delay. Y. Nagata et al. presented an adaptive loop-delay estimate algorithm in [1]. But this iteration algorithm was influenced by the PA nonlinear distortion obviously, which disrupted the accuracy and stability of the loop-delay estimation. Kim and Lee adopted 64 times oversampling scheme to improve the estimation accuracy [2]. But it is impractical in wide-band predistorter. The delay-locked loop (DLL) circuit method was proposed by Tang in [3]. The new method has shown fast estimation performance but it increased hardware complexity. When predistorter processes a higher rate interpolation under long time delay conditions, researchers tried to use a two-step time-delay estimation method to save resources and processing time [4]. However, large calculation quantity problem still exists in its fraction delay estimation part. Naskas proposed a new loop-delay estimation method which adopted special training sequence [5]. But it has application limited. Wright and Durtler presented a new estimate algorithm[6,7] which adopted the fast Fourier transform (FFT). However, the computational complexity is large and the processing time is too long. Moreover, due to the application of mark cycle , the algorithm is related with system format and the applied range is also limited. In [8] Li et al. proposed integer estimation algorithm based on correlation function and fraction estimation algorithm. They supposed that the feed back loop was a linear loop, thus the input signal was roughly the same as the delay signal ($x_{in} \approx x_{fb}$). However, these assumptions are disturbed by the PA nonlinear distortions and the fraction estimation algorithm based on Block-LMS method becomes impractical. Therefore, the fraction estimation was inaccurate.

On the other hand, most of the predistorters are designed in indirect learning architecture [9]-[11]. However, there are two main draw-backs that decrease the indirect learning model performance [12]. First, the measurement noisy of PA's output will make the adaptive algorithm converges to biased values. Second, the nonlinear filters cannot be swapped equivalently. The training data of indirect learning model are relative poor quality. Therefore, copying coefficients of post-distorter into predistorter does not guarantee a good pre-inverse model for the nonlinear device and the literatures show that direct learning architecture performs in general better than indirect learning model [13].

In this paper, aiming at the disadvantages of delay estimation methods and indirect learning model, we propose a direct learning architecture with a new delay estimation algorithm based on analyzing the relationship between the system loop-delay and the amplitude of the predistorter output error off-line during the HPA nonlinear model identification process. It is independent of the signal format and is suitable for nonlinear distortion. The simulation

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Corresponding Author: Nan Wu (wunan@bit.edu.cn).

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results show that the new algorithm reduces the loop-delay misalignment influence on the predistortion process and maintains the continuity of signal transmission.

The rest of this paper is organized as follows. In Section II, the relationship between the system loop-delay and the HPA identification output error amplitude are investigated and the system format-free loop-delay estimate algorithm is proposed. The new algorithm realizes the synchronous work of the HPA identification and the system loop-delay estimation. In Section III, simulations are presented to evaluate the performance of the new algorithm. Finally, conclusions are given in Section IV.

II. LOOP-DELAY ESTIMATE ALGORITHM

A. Predistorter and Model Identification Algorithm:

The system considered is constructed by polynomial predistorter, Identification module and loop-delay correction module (Fig. 1 and Fig2.). The polynomial is a widely used model to process the PA nonlinear distortions. which can be expressed as:

$$v_d(n) = \sum_{k=1}^{K} a_k x'(n)\left|x'(n)\right|^{k-1} \tag{1}$$

where K is the nonlinear order. a_k is the polynomial coefficient. $x'(n)$ is the compensated data that corrected by delay compensator from *x(n)*. Because the even order intermodulation frequency can be removed by the filter, we only take the odd order nonlinear distortion into account [9]. Hence, (1) can be simplified as follow,

$$v_d(n) = \sum_{\substack{k=1 \\ Odd}}^{K} a_k x'(n)\left|x'(n)\right|^{k-1} \tag{2}$$

where we supposed K=5.

The recursive least square (RLS) algorithm is a commonly used self-adapt algorithm. Its update purpose is to make the output signal and the desired signal match best in the sense of the least squares. Because of its fast convergence characteristics, the RLS algorithm is widely used in real-time system identification and fast equalization, etc [14]. In this paper, we use this algorithm to identify HPA model (Fig. 1) and update predistortion coefficients (Fig. 2).

The sum of weighted index error square is used as the cost function. In HPA identification process the cost function is expressed as

$$\begin{aligned} J(n) &= \sum_{i=0}^{n} \lambda^{n-i}\left|e(n)\right|^2 \\ &= \sum_{i=0}^{n} \lambda^{n-i}\left|v_a(n) - v_d(n)\right|^2 \\ &= \sum_{i=0}^{n} \lambda^{n-i}\left|v_a(n) - \mathbf{a}^H(n-1)\mathbf{u}(n)\right|^2, \end{aligned} \tag{3}$$

where the weighting factor $0<\lambda<1$ is called forgetting factor. $\mathbf{a}$ is composed by a_k, k is odd numbers and $\mathbf{u}$ is the column vector composed by x'(n) which is expressed as

$$\mathbf{u}(n) = [x'(n)\,|\,x'(n)|^0\; x'(n)\,|\,x'(n)|^2 \ldots x'(n)\,|\,x'(n)|^{k-1}]^T \tag{4}$$

The key steps of RLS algorithm are as follow:

- Initialization: $\mathbf{a}(0) = \mathbf{0}, \mathbf{P}(0) = \delta^{-1}\mathbf{I}$, in which δ is a very small value;
- Update the gain vector:

$$\mathbf{k}(n) = \frac{\mathbf{P}(n-1)\mathbf{u}(n)}{\lambda + \mathbf{u}^H(n)\mathbf{P}(n-1)\mathbf{u}(n)} \tag{5}$$

- Predistorter coefficient update:

$$\mathbf{a}(n) = \mathbf{a}(n-1) + \mathbf{k}(n)\left[\mathbf{v}_a(n) - \mathbf{a}^H(n-1)\mathbf{u}(n)\right]^* \tag{6}$$

- The inverse matrix update:

$$\mathbf{P}(n) = \frac{1}{\lambda}\left[\mathbf{P}(n-1) - \mathbf{k}(n)\mathbf{u}^H(n)\mathbf{P}(n-1)\right] \tag{7}$$

We employ HPA model recognition based on RLS algorithm and proposed a new loop-delay compensation algorithm (illustrated in Fig.1), which can identify the amplifier nonlinear model and compensate the system loop delay at the same time.

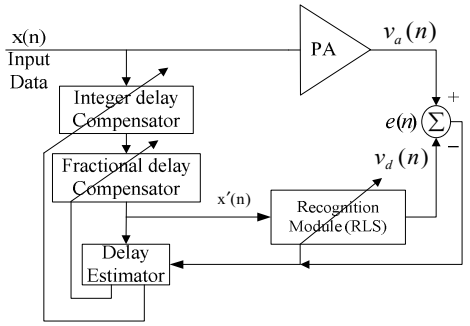

Fig. 1. The block diagram of HPA identification module

When the HPA nonlinear distortion model is identified correctly, the recognized model will be used to train the predistorter based on direct learning structure off-line and the cost function is changed to

$$J(n) = \sum_{i=0}^{n} \lambda^{n-i}\left|x(n) - v_a'(n)/G\right|^2 \tag{8}$$

The direct predistorter module coefficient is obtained after the convergence of the algorithm. Finally, the off-line training coefficient is updated to the on-line predistortion module that can achieve a new round of predistortion compensation processing.

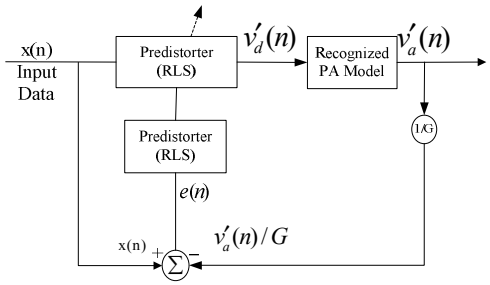

Fig. 2. The block diagram of predistorter based on direct learning structure.

Because the proposed predistortion algorithm based on direct learning structure compensates loop delay only in HPA model identification process and training predistortion coefficients off-line. The new algorithm enhances the predistortion algorithm performance compared with the indirect learning structure. Moreover, compared with traditional direct learning, the proposed predistortion algorithm with the new loop-delay estimation method can reduces the signal transmission interference caused by on-line predistortion training and maintains the integrality and continuity of signal transmission continuously.

B. *The relationship between the system loop-delay and the amplitude of HPA model identification error:*

By analyzing the relationship between the system loop-delay and the amplitude of HPA model identification error output, we can conclude: when the loop-delay misalignment gets smaller, the amplitude of HPA model identification output error becomes smaller as well, conversely the amplitude of HPA identification module output error become larger when the loop-delay misalignment gets larger. So we propose a new loop-delay estimation algorithm which can work with the HPA model identification algorithm simultaneously. The new algorithm dismisses traditional correlation calculations. Therefore, it is robust to by the PA nonlinear distortion and can estimate value stability and accuracy.

C. *Loop-delay Estimation algorithms*

Loop-delay algorithm can be divided into two parts: integer loop-delay and fraction loop-delay.

1) Integer loop-delay algorithm:

When each HPA model identification process (with loop-delay) is finished, the system can get and save instantaneous identification error $e(n)$ from (3). After M (M=100) identification iterations, we substitute the identification errors into (9) to calculate the mean error amplitude $\overline{e}_{\mathrm{mod}}(k)$. Then, substitute $\overline{e}_{\mathrm{mod}}(k)$ in integer loop-delay algorithm. After several iterations, the integer delay estimate can be obtained. The expressions of iteration are (10) and (11):

$$\overline{e}_{\mathrm{mod}}(k)=\sum_{n=(k-1)\cdot M+1}^{k\cdot M}\left|e(n)_{d_k}\right|\Big/M \tag{9}$$

$$d_{k+1}=d_k+sign\left[\overline{e}_{\mathrm{mod}}(k)-\overline{e}_{\mathrm{mod}}(k-1)\right]\cdot K\cdot\overline{e}_{\mathrm{mod}}(k) \tag{10}$$

$$\mathrm{Delay}=\mathrm{int}(\left|d_k\right|) \tag{11}$$

where $\mathrm{d_k}$ presents the estimated integer delay value , $\mathrm{d_1}=0$, $\overline{e}_{\mathrm{mod}}(0)=+\infty$, $k=1,2,3\ldots n/M$, n is the number of identification iterations, K is iteration coefficient (in this paper, K=5). In (11), $\mathrm{int}(\cdot)$ is defined as the operation of finding the nearest integer of $\left|d_k\right|$. From (9) - (11), the algorithm can estimate the integer loop-delay value and adjust compensation and then the next HPA model identification algorithm computing begins. After several iterations, the final integer delay estimate is obtained.

2) Fraction loop-delay algorithm:

The fraction loop-delay estimation is similar to the integer loop-delay estimation:

$$f_k=f_{k-1}+sign\left[\overline{e}_{\mathrm{mod}}(k)-\overline{e}_{\mathrm{mod}}(k-1)\right]\cdot K\cdot\overline{e}_{\mathrm{mod}}(k) \tag{12}$$

$$fraction=\mathrm{int}(\left|f_k\right|*100)/100 \tag{13}$$

When the fraction delay value f_k is estimated, the new algorithm treat the fraction delay with quantify precision to two fraction places. After several iterations, the algorithm converge at the actual fraction delay estimate value, the loop-delay estimation algorithm judges whether the estimation should stop according to the NMSE value.

When the process entering the fraction loop-delay estimation and compensation computation section, the loop-delay has been reduced to the part in interval [$-T_s/2$,$T_s/2$]. The fraction loop-delay compensation is realized by using a 4-tap piecewise-parabolic interpolation filter which can sum all the positive and negative fractional loop-delays to generate a positive fraction loop-delay compensation value .

The widely used 4-tap piecewise-parabolic interpolator is

$$y_{in}(n)=\begin{cases}\sum_{i=-2}^{1}a_i(\theta)x_{in}(n+i) & (\theta>0)\\ \sum_{i=-2}^{1}a_i(1+\theta)x_{in}(n+1+i) & (\theta<0)\end{cases} \tag{14}$$

where x_{in} denotes the real part of complex form input signal, y_{in} denotes the delay signal generated by x_{in} passing the interpolation filter. $a_i(\theta)$ can be described as follow:

$$\begin{cases}a_1(\theta)=\alpha\theta^2-\alpha\theta,\\ a_0(\theta)=-\alpha\theta^2+(\alpha-1)\theta+1,\\ a_{-1}(\theta)=-\alpha\theta^2+(\alpha+1)\theta,\\ a_{-2}(\theta)=\alpha\theta^2-\alpha\theta,\end{cases} \tag{15}$$

where α is the default coefficient, which is $\alpha=0.25$ in this paper. θ is the fraction loop-delay estimate. Because the amplitude variation in adjacent sampling points is very small, we can get the approximate expression:

$$x_{in}(n+1)-x_{in}(n)\approx x_{in}(n-1)-x_{in}(n-2) \tag{16}$$

By substituting (15) and (16) into (14),we have:

$$y_{in}(n)=\begin{cases}\theta\cdot(x_{in}(n-1)-x_{in}(n))+x_{in}(n)\\ (1+\theta)\cdot(x_{in}(n)-x_{in}(n+1))+x_{in}(n+1)\end{cases} \tag{17}$$

The result of interpolation filter with the proposed loop delay estimation method is shown in Fig. 3 it is seem that both the integer and fraction loop delay are well compensated [8].

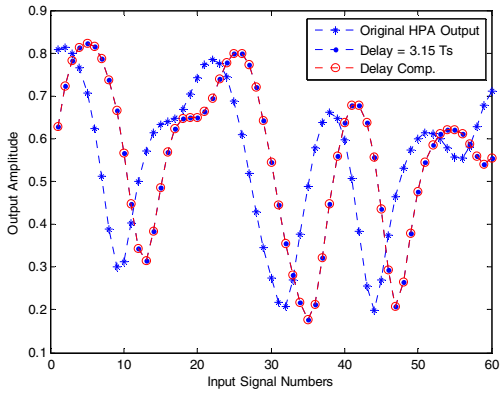

Fig. 3. Output signal of loop-delay interpolation compensator

III. SIMULATION RESULTS

In this paper, we select 16QAM-modulated baseband signal with 8 times up-sample and use Saleh model as the amplifier, in which the amplifier coefficients are: α_ρ =2, β_ρ =1, $\alpha_\theta = \pi/3$, β_θ =1. The NMSE value of the recursive algorithm is defined as:

$$NMSE(dB) = 10\log_{10}\left[\frac{\sum_{n=1}^{M}|x(n)-v_a(n)|^2}{\sum_{n=1}^{M}|x(n)|^2}\right] \qquad (18)$$

A. Performance of loop delay estimation algorithm:

The convergence performance is shown in Fig. 4: after about 4000 points iteration, the join operation of the new predistortion algorithm can estimate loop delay and converge at *delay* = -1.36 *Ts* (*Ts* is the sampling period).

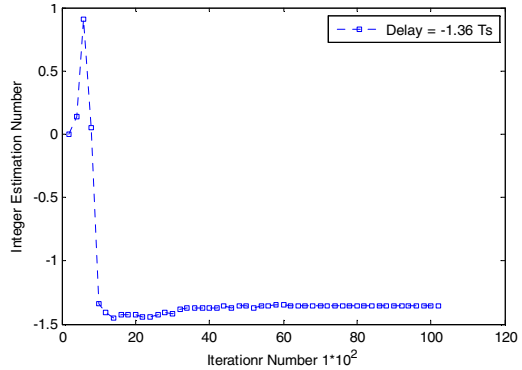

Fig. 4. Delay estimate convergence curve

B. Constellation

Fig. 5 (a) is the output signal with nonlinear distortion. It shows that severe distortion occurs when original signal goes through the amplifier without predistortion. Fig. 5 (b) shows the output signal with predistortion compensation but with 0.1 *Ts* loop delay influence. We can see that though the output signal amplitude expansion caused by PA nonlinearity is corrected, the expansion caused by loop-delay error still exists and deteriorates the system performance. Fig. 5(c) shows output signal with both predistortion and loop delay compensation. It shows that by proposed predistorter with the new loop-delay estimation method, both the amplitude distortion and the phase distortion of the output signal constellation are corrected effectively and this constellation is very close to the original signal constellation. Thus, the new algorithm has made excellent linearization effect.

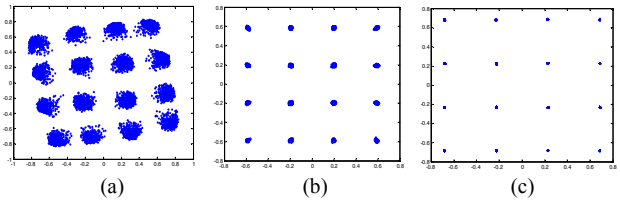

Fig. 5. (a) without loop-delay but with nonlinear distortion (b)with predistortion compensation but with loop-delay=0.1 Ts influence, (c) with both predistortion and delay compensation

C. Power Spectral Density Improvement

Fig. 6 illustrates the signal out-of-band power spectral density (PSD) figures:

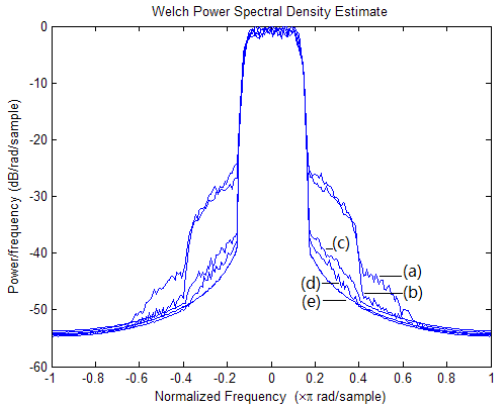

Fig. 6. Signal out-of-band power spectral density of HPA output. (a) Delay 3.15 w/ predsitortion; (b) Delay=0 w/o predistortion (c) Delay 0.1 w/ predistortion ,(d) Delay Correction w/ Preditortion; (e)ideal PSD

From the figure, we can observe that even when the output signal is processed by predistorter, the spectral regrowth phenomenon caused by the loop-delay (Fig. 6(a)) is still obvious. Even when the loop-delay is merely 0.1 Ts (Fig. 6 (c)) the loop-delay influence still can not be ignored. Fig. 6 (d) represents the signal out-of-band power spectral density figure of HPA with both predistortion and loop-delay compensation, compared with Fig. 6(a) and (b) the signal regrowth phenomenon decreases and the curve shape is closer to the ideal PSD figure (Fig. 6(e)). Compared to the predistortion compensation with 3.15 *Ts* loop delay influence, the new algorithm can improve signal out-of-band power spectral density by -20dB.

D. Convergence Performance

In practical application, the characteristics of HPA will drift because of the variance of transmission channel and environment temperature. Therefore, adaptive algorithm is needed to track this kind of drift. Fig. 7 shows NMSE curves of HPA model identification module with loop-delay=3.15,

1.15, 0.35 and 0.1 *Ts*, respectively. In Fig. 7 with delay=3.15 to 0.35, the identification module is influenced by loop-delay severely, the performance is decreased by nearly -40 to -55dB and even small loop-delay (loop-delay=0.1) influence can decrease the model identification performance by 30 dB. In Fig 7. We can see that when the loop delay is corrected by proposed algorithm, the improved NMSE performance is nearly -60dB (Fig. 7 legend "Delay Corrected"). Therefore, the new loop-delay estimate algorithm has good NMSE performance of HPA model identification.

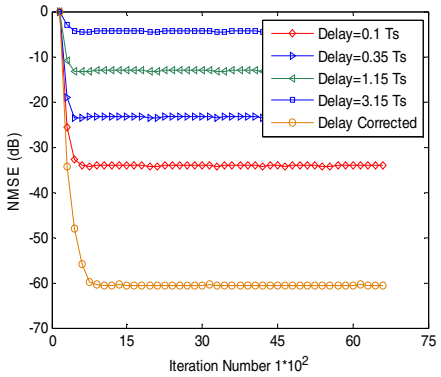

Fig. 7. NMSE peformance of HPA model identification.

Fig. 8 shows the NMSE performance of direct and indirect learning predistortion structure. By comparing the NMSE curves, we can see the predistorter based on direct learning structure can only converge at -40 dB when the loop delay is 0.5 *Ts*. In the indirect learning structure predistortion system, the performance of the postposition predistorter can converge to -51 dB. After the postposition predistorter coefficient is copied to the preposition module, the algorithm performance will drop and can only converge to -49 dB. Therefore, the nonlinear filters cannot be swapped equivalently. The proposed predistortion algorithm can converge to -59 dB. Compared with the traditional indirect learning structure, the algorithm is about 8 dB NMSE performance improved and compared with the predistorter with loop delay influence, the well delay compensated predistorter can promote performance about 19 dB. Meanwhile, in the newly proposed predistortion algorithm, the HPA model identification, delay compensation and predistortion operation are completed off-line. Therefore, the new predistortion algorithm can maintain signal transmission integrally and continuously.

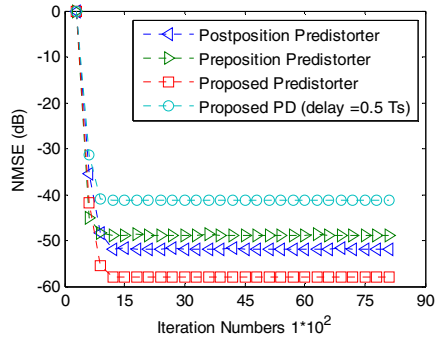

Fig. 8. NMSE performance of different predistortion structure.

IV. CONCLUSION

In this paper, we proposed direct learning predistorter with a new loop delay estimation algorithm based on the relationship between the system loop-delay and the amplitude of HPA model identification output error. This new algorithm changes the traditional loop-delay judging standard and realizes the model identification and the system loop-delay estimation working simultaneously. Simulation results show that the new algorithm can reduce loop-delay influence and realizes the predistortion and the loop-delay estimation off-line which maintains the reliability and continuity of signal transmission. Therefore, this algorithm achieves an ideal predistortion and loop delay compensation effect.

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