MIMO Hardware Simulator: Digital Block Design for 802.11ac Applications with TGn Channel Model Test

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***Abstract*—This paper presents new frequency domain and time domain architectures for the digital block of a hardware simulator of MIMO propagation channels. This simulator can be used for 802.11ac applications. The hardware simulator facilitates the test and validation cycles by replicating channel artifacts in a controllable and repeatable laboratory environment, thus making it possible to ensure the same test conditions in order to compare the performance of various equipments. After the description of the general characteristics of the hardware simulator, the new architectures of the digital block are presented and designed on a Xilinx Virtex-IV FPGA. Their accuracy and latency are analyzed. TGn channel model E tests are given in details. Lastly, results for all TGn channel models are presented.**

Keywords-Hardware simulator; radio channel; MIMO; FPGA; TGn channel model

I. INTRODUCTION

Multiple-Input Multiple-Output (MIMO) systems make use of antenna arrays simultaneously at both transmitter and receiver to improve the channel capacity and the system performance. Because the transmitted electromagnetic waves interact with the propagation environment (indoor/outdoor), it is necessary to take into account the main propagation parameters for the design of the future communication systems.

Hardware simulators of mobile radio channel are very useful for the test and verification of wireless communication systems. These simulators are standalone units that provide the fading signal in the form of analog or digital samples [1], [2].

The current communication standards indicate a clear trend in industry toward supporting MIMO functionality. A support for higher order of antenna arrays will be required to enable higher channel capacity and system performance. In fact, several studies published recently present systems that reach a MIMO order of 8×8 and higher [3]. This is made possible by advances at all levels of the communication platform as, for example, the monolithic integration of antennas [4] and the design of the simulator platforms.

With the continuous increase of field programmable gate array (FPGA) capacity, entire baseband systems can be efficiently mapped onto faster FPGAs for more efficient prototyping, testing and verification. As shown in [5], the FPGAs provide the greatest flexibility in algorithm design and visibility of resource utilization. Also, they are ideal for rapid prototyping and research use such as testbed [6].

The simulator is reconfigurable with standards bandwidth not exceeding 100 MHz, which is the maximum for FPGA Virtex IV. However, in order to exceed 100 MHz bandwidth, more performing FPGA as Virtex VI can be used [7]. The simulator is configured with the Long Term Evolution System (LTE) and Wireless Local Area Networks (WLAN) 802.11ac standards. The channel models used by the simulator can be obtained from standard channel models, as the TGn 802.11n [8], or from real measurements conducted with the MIMO channel sounder designed and realized at IETR [9]. Different architectures of antenna arrays can be used for outdoor and indoor measurements [10].

At IETR, several architectures of the digital block of a hardware simulator have been studied, in both time and frequency domains [11], [12]. Moreover, [13] presents a new method based on determining the parameters of a channel simulator by fitting the space time-frequency cross-correlation matrix of the simulation model to the estimated matrix of a real-world channel. This solution can be considered only as heuristic method because it shows that the error obtained can be important. Typically, wireless channels are commonly simulated using finite impulse response (FIR) filters, as in [12], [14] and [15]. Nowadays, different approaches have been widely used in filtering, such as distributed arithmetic (DA) and canonical signed digits (CSDs). However, for a hardware implementation, it is easier to use the FFT (Fast Fourier Transform) module to obtain an algebraic product. Thus, frequency architectures are presented, as in [12] and [14].

The previous considered frequency architectures in [12] operate correctly only for signals with a number of samples not exceeding the size of the FFT. However, in this paper, a new frequency domain architecture avoiding this limitation, and a new time domain architecture are both tested with TGn channel models, and a description in detail is given for TGn Model E.

The rest of this paper is organized as follows. Section II presents the new frequency and time domain architectures of the digital block. Section III shows the hardware implementation of the digital block for each architecture. Moreover, the accuracy of these two architectures is analyzed. Lastly, Section IV presents some concluding remarks.

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II. HARDWARE SIMULATOR: PRINCIPLE, ARCHITECTURE AND OPERATION

The simulator must reproduce the behavior of a MIMO propagation channel. The design of the RF blocks for UMTS (Universal Mobile Telecommunications System) was completed during a previous project [12]. It is able to accept input signals between -50 and 33 dBm. The objectives of PALMYRE II* project concern the channel models and their hardware implementation into the MIMO simulator.

The bandwidth is between 1.5 MHz and 20 MHz for LTE, and 80 MHz or 160 MHz for 802.11ac. However, The FPGA Virtex IV does not support bandwidths larger than 100 MHz. TGn channel models cover all scenarios for WLAN applications, and the duration of the impulse responses does not exceed 1.05 µs for all TGn channel models. Thus, in this paper, tests are made with 802.11ac standard with a considered bandwidth of 80 MHz.

A. Channel Model

TGn channel models [8] have a set of 6 profiles, labeled A to F, which cover all the scenarios. Each model has a number of clusters. For example, model E, which is used for outdoor to indoor environment, has four clusters. Each cluster corresponds to specific tap delays, which overlaps each other in certain cases. Table I summaries the relative power of the impulse responses for TGn channel model E by taking the LOS (Line-Of-Sight) impulse response as reference [8]. The relative powers of all impulse responses for all TGn channel models are presented in [8]. According to the standard and the bandwidth, the sampling frequency is $f_s = 180$ MHz and $T_s = 1/f_s$.

TABLE I. RELATIVE POWER OF THE IMPULSE RESPONSE FOR MODEL E

Tap index	Excess delay [nT_s]	Relative Power [dB]	Tap index	Excess delay [s]	Relative Power [dB]
1(Ref)	0	-2.6	**10**	41T_s	-5.5
2	2T_s	-3.0	**11**	50T_s	-7.6
3	4T_s	-3.5	**12**	59T_s	-9.8
4	5T_s	-3.9	**13**	68T_s	-12.0
5	9T_s	-0.06	**14**	77T_s	-14.2
6	14T_s	-1.2	**15**	88T_s	-15.3
7	20T_s	-2.5	**16**	101T_s	-18.3
8	25T_s	-3.8	**17**	115T_s	-20.7
9	32T_s	-3.3	**18**	131T_s	-24.6

The relative power of the first tap is different than zero because the impulse response is in NLON (Non-Line-Of-Sight). Fig. 1 presents the impulse response of TGn model E.

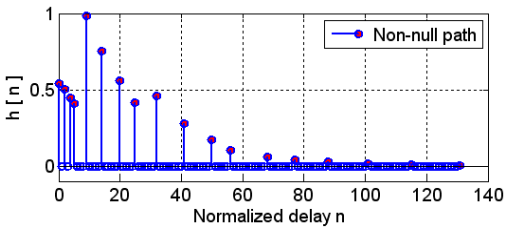

Figure 1. Channel impulse response of TGn channel model E.

The channel models used by the simulator can also be obtained from measurements by using a time domain MIMO channel sounder designed and realized at the IETR [9], as shown in Fig. 2.

Figure 2. MIMO channel sounder: receiver and transmitter.

B. Digital Block

According to the considered propagation environments, Table II summarizes some useful parameters for WLAN 802.11ac standard. The number of samples is:

$$N = W_t f_s \quad (1)$$

where W_t represents the width of the time window of the impulse response of the propagation channel.

TABLE II. SIMULATION PARAMETERS

Type	Cell Size	$W_{t\,eff}(\mu s)$	N	$W_t(\mu s)$
Office	40 m	0.35	64	0.35
Indoor	50-150 m	0.71	128	0.71
Outdoor	50-150 m	1.16	256	1.42

In order to have a suitable trade-off between complexity and latency, two solutions are considered: a time domain approach and a frequency domain approach. For indoor environments, W_t is smaller than 1 µs. Therefore, the time domain approach is more suitable to use, because a FIR filter has, in spite of its relative complexity, much lower latency. However, the frequency approach has huge generated latency (more than 1µs). N is the closest 2^n value which is imposed by the FFT. Therefore, both approaches can be used according to the considered propagation environment.

A description of the architecture of the digital block for the "simple" frequency domain is presented in [12]. In this section, we present a new improved frequency domain architecture and a time domain architecture based on a FIR filter.

1) *New Frequency Domain Architecture*

The new frequency architecture for a SISO channel is presented in Fig. 3. This architecture has been verified and tested with Gaussian impulse response and a description is presented in [16]. It operates correctly for signals with a number of samples exceeding the size of the FFT module.

For TGn channel model E, $N_{eff} = 131$ samples. Thus, N = 128 samples (the last tap has a relative power of -24.6 dB, therefore it will be considered as zero). However, to test the new architecture, it is mandatory to extend each partial input of

* CPER PALMYRE - II Project supported by "Région Bretagne".

N samples with a "tail" of N null samples, as in [16], to avoid a wrong result. Therefore, 256-FFT/IFFT modules are used.

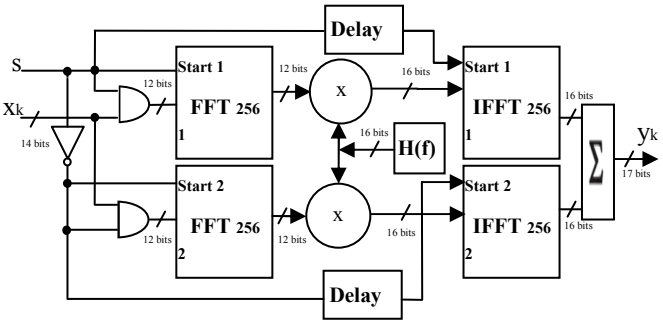

Figure 3. Frequency architecture of a SISO channel.

Due to the use of a 14-bit digital-to-analog convertor (DAC), the output of the final adder must be truncated. A simple solution is to keep the 14 most significant bits. This is a "brutal" truncation. However, a better solution is the sliding window truncation presented in Fig. 4 which uses the 14 most effective significant bits [11].

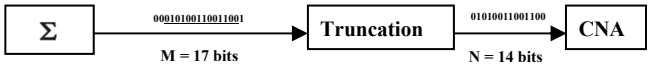

Figure 4. Sliding window truncation, from 17 to 14 bits.

2) *Time Domain Architecture*

Studies of the FIR filter with 64 points are presented in [11]. For TGn channel model E, the length of the FIR filter is N = 131. This model imposes the use of 18 multipliers. Thus, the output signal can be computed as:

$$y_q(i) = \sum_{k=1}^{18} h_q(i_k)x_q(i-i_k),\ i \in \mathbb{N}. \qquad (2)$$

The index q suggests the use of quantified samples and $h_q(i_k)$ is the attenuation of the k^{th} path with the delay $i_k T_s$. Fig. 5 presents the architecture of the FIR filter 131 with 18 non-null coefficients. This architecture uses series of impulse responses with a refresh frequency f_{ref} depending on the coherence time of the channel, in order to simulate a time variant channel. Therefore, we have developed our own FIR filter instead of using Xilinx MAC FIR filter to make it possible to reload the FIR filter coefficients. f_{ref} must be at least twice the maximum Doppler frequency.

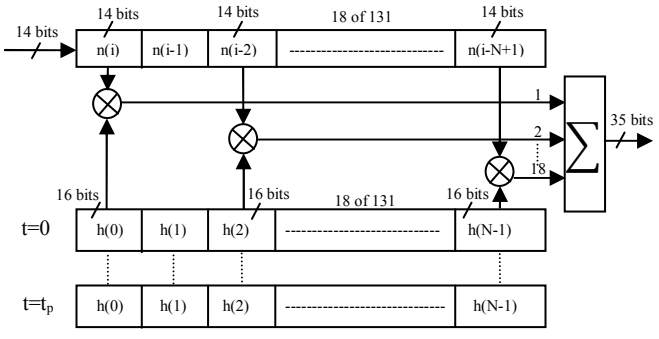

Figure 5. FIR 131 with 18 multipliers.

III. IMPLEMENTATION

In order to implement the hardware simulator, the adopted solution uses a prototyping platform (XtremeDSP Development Kit-IV for Virtex-4) from Xilinx [7], which is presented in Fig. 6 and described in [16].

Figure 6. XtremeDSP Development board Kit-IV for Virtex-4.

The simulations and synthesis are made with Xilinx ISE [7] and ModelSim software [17].

A. Implementation and Results of Frequency Architecture

The V4-SX35 utilization summary for this architecture with FFT 256 and IFFT 256 blocks is given in Table III.

TABLE III. VIRTEX-4 SX35 UTILIZATION FOR 2 FFTS AND 2 IFFTS IN PING-PONG FREQUENCY ARCHITECTURE

Number of slices	3,651 out of 15,360	24 %
Number of bloc RAM	18 out of 192	10 %
Number of DSP48s	30 out of 192	16 %

In order to determine the accuracy of the architecture, Gaussian input signal x(t) is considered long enough (more than N = 256 samples) to be used in streaming mode:

$$x(t) = x_m e^{-\frac{(t-m_x)^2}{2\sigma^2}},\ 0 \le t \le 3W_t \qquad (3)$$

where N = 256, $W_t = NT_s$, $m_x = 3W_t/4$ and $\sigma = m_x/4$.

The A/D and D/A convertors of the development board have a full scale $[-V_m, V_m]$, with $V_m = 1\ V$. For the simulations we consider $x_m = V_m/2$. The theoretical output signal is:

$$y(t) = \sum_{k=1}^{18} h(i_k)x(t-i_k T_s) \qquad (4)$$

The relative error is computed for each output sample by:

$$\varepsilon = \frac{Y_{Xilinx} - Y_{theory}}{Y_{theory}}.100\ [\%] \qquad (5)$$

where Y_{Xilinx} and Y_{theory} are vectors containing the samples of corresponding signals. The Signal-to-Noise Ratio (SNR) is:

$$SNR(i) = 20\log_{10}\left|\frac{Y_{theory}(i)}{Y_{Xilinx}(i) - Y_{theory}(i)}\right|\ [dB],\ i=\overline{1,3N+i_{18}} \qquad (6)$$

Fig. 7 shows the theoretic signal and Xilinx signal at the output with their relative error for the new frequency architecture using TGn channel model E, with $f_s = 180$ MHz.

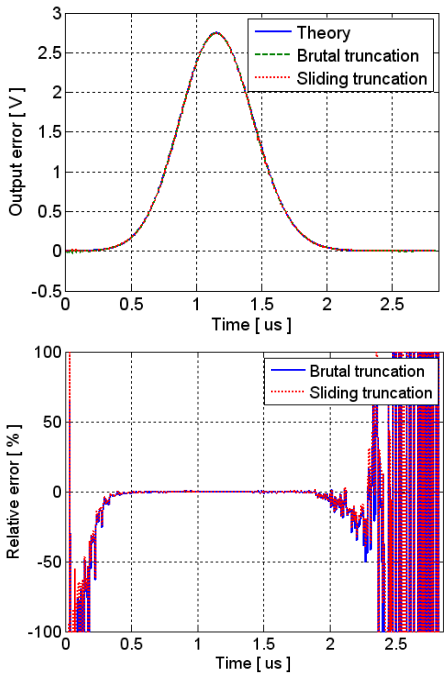

Figure 7. Theoretic and Xilinx output signals for the frequency architecture and the relative error, with TGn channel model E.

The values with brutal and sliding truncation are close because the signal before truncation is presented on 17 bits.

After the D/A convertor, the signal is limited to $[-V_m,V_m]$ with $V_m = 1$. If $y_{max} > 1$ V as shown in Fig. 7, a reconfigurable analog amplifier placed after the DAC is mandatory to multiply the signal with 2^{k_0}, where k_0 is the smallest integer verifying $y_{max} < 2^{k_0}$. The relative error is high only for small values of the output signal because the signal Gaussian test is close to 0.

The global values of the relative error and of the *SNR* of the output signal after the final truncation are:

$$\varepsilon_g = \frac{\|E\|}{\|Y_{theory}\|} 100\ [\%] \qquad (7)$$

$$SNR_g = 20.\log 10 \frac{\|Y_{theory}\|}{\|E\|}\ [dB] \qquad (8)$$

where $E = Y_{Xilinx} - Y_{theory}$ is the error vector. For a given vector $X = [x_1, x_2, \ldots, x_L]$, its Euclidean norm $\| x \|$ is:

$$\|X\| = \sqrt{\frac{1}{L}\sum_{k=1}^{L} x_k^2} \qquad (9)$$

Table IV shows the global values of the relative error and the global SNR between the theoretical and the Xilinx signal.

TABLE IV. COMPARISON OF THE GLOBAL ERROR AND SNR WITH FREQUENCY DOMAIN ARCHITECTURE

Truncation effect	Error (%)	SNR (dB)
Output without truncation	0.2390	52.42
Output with sliding truncation	0.2390	52.42
Output with brutal truncation	0.2463	52.16

B. *Implementation and Results of Temporal Architecture*

Table V shows the device utilization for a single FIR filter 131 for 18 selected positions for the channel impulse response which are considered as non-null, in one V4-SX35 after synthesis, mapping and route.

TABLE V. SIMULATION RESULTS FOR FIR FILTER

Number of slices	2,189 out of 15,360	14 %
Number of bloc RAM	18 out of 192	9 %
Number of multipliers	18 out of 192	9 %

Fig. 8 presents the theoretic and Xilinx output signals using one FIR 131 with 18 coefficients considered as non-null and the relative error.

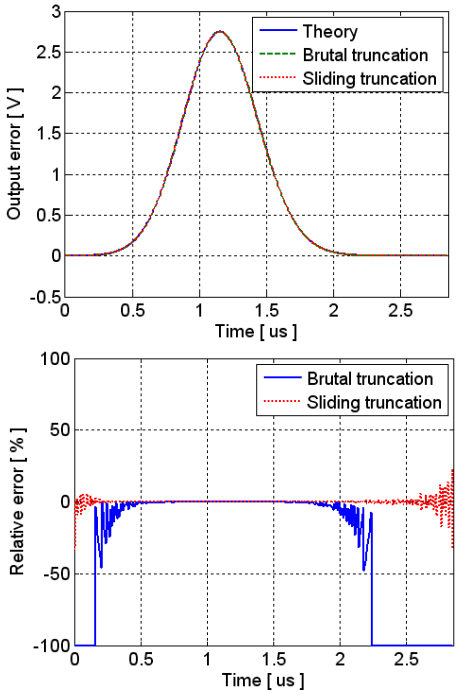

Figure 8. Theoretic and Xilinx output signals for the time domain architecture and the relative error, with TGn channel model E.

Table VI shows the global values of the relative error and the global SNR between the theoretical and the Xilinx signal.

TABLE VI. COMPARISON OF THE GLOBAL ERROR AND SNR WITH TIME DOMAIN ARCHITECTURE

Truncation effect	Error (%)	SNR (dB)
Output without truncation	0.0050	86.10
Output with sliding truncation	0.0120	78.43
Output with brutal truncation	0.1699	55.38

Before each operation, the 18 coefficients of the FIR filter are stored first in 1 shift register of length 18 via the USB port of the development board. Then, they are stored in the FPGA dual-port RAM.

C. *Result with all TGn Channel Models*

Table VII shows the global values of the relative error and SNR with sliding window truncation, and the occupation on the FPGA, for both architectures and for all TGn channel model B

to F. As presented in [8], TGn model A should not be used for system performance comparisons.

TABLE VII. COMPARISON OF THE GLOBAL ERROR AND THE SNR FOR TGN CHANNEL MODELS

Model B	**Frequency Architecture**		**Time Architecture**	
Relative Error	Error (%)	SNR (dB)	Error (%)	SNR (dB)
	0.9666	40.25	0.0132	77.61
Slices (%)	15 (with FFTs 32)		11(with FIR 14)	
Model C				
Relative Error	Error (%)	SNR (dB)	Error (%)	SNR (dB)
	0.4121	47.69	0.0109	79.24
Slices (%)	20 (with FFTs 128)		12(with FIR 36)	
Model D				
Relative Error	Error (%)	SNR (dB)	Error (%)	SNR (dB)
	0.2406	52.36	0.0106	79.45
Slices (%)	24 (with FFTs 256)		14(with FIR 70)	
Model E				
Relative Error	Error (%)	SNR (dB)	Error (%)	SNR (dB)
	0.2390	52.42	0.0120	78.43
Slices (%)	24 (with FFTs 256)		14(with FIR 131)	
Model F				
Relative Error	Error (%)	SNR (dB)	Error (%)	SNR (dB)
	0.1714	55.31	0.0110	79.18
Slices (%)	30 (with FFTs 512)		14(with FIR 189)	

D. Discussion

We compare the time domain architecture with the new frequency domain architecture. According to Table VII, three points resume the comparison: the precision, the occupation on the FPGA and the latency.

With sliding truncation, the relative error do not exceed 1 % (for the worst case, with TGn model B), which is sufficient for the test. However, the time domain architecture presents high precision.

In terms of occupation of slices on the FPGA Virtex IV, the maximum value for the time domain architecture is 14 % in contrast with the occupation of the frequency domain architecture which vary between 15 % and 30 %. Thus, the time domain architecture presents another advantage which allows the implementation of 6 SISO channels with model D, E and F. Therefore, MIMO 3x2 system can be used and which operates via 18x6 = 108 multipliers and producing an occupation of 84 % of slices on the FPGA. With model B and C, it is possible to implement 8 SISO channels.

In term of latency, the time domain architecture presents another point of advantage by generating a latency of 165 ns. However, the new frequency architecture generates 7 µs.

Therefore, the time domain architecture is more efficient to use, especially for MIMO systems. However, the use of more performing FPGAs as Virtex 6 is mandatory to solve the occupation problem for the new frequency domain architecture. It will provide the use of many SISO channels and be able to test a MIMO system.

IV. CONCLUSION

After a comparative study, in order to reduce occupation on the FPGA, the error and the latency of the digital block, the time domain architecture present the best solution for indoor environments, which has been tested in this paper with TGn channel model.

Nowadays, we test a configuration which requires 3 XtremeDSP Development Kit-IV. More measurement campaigns will be carried out with the MIMO channel sounder realized by IETR, for various types of environments (indoor, outdoor). More tests will be done by using a time-varying channel. Thus, the architectures will be completed to obtain a "dynamic" system. A Graphical User Interface will be designed to allow the user to reconfigure the channel parameters. The final objective is to obtain realistic and reliable impulse responses of the MIMO channel in order to supply the digital block of the hardware simulator.

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