WK2132 Multibus Interface 2-Channel Universal Asynch

Transceiver Lead (Pb) free package

1. Product overview

The WK2132 is the first 2-channel UART with low power consumption of 256-level FIFOs and support for UART/SPI™/IIC interfaces Devices. Mode selection allows the chip to operate in either of the above main interface modes, expanding the selected main interface into 2 enhanced UARTs.

The extended sub-channel UART has the following functional features:

- The baud rate, word length, and check format of each subchannel UART can be set independently, and the communication rate can be up to 2Mbps. Each subchannel can be set up independently to work on IrDA irred communication.
- Each subchannel has a 256-level FIFO that receives/sends independently, and the interrupts of the FIFO can be programmed to trigger the user's needs and have Timeout interrupt function.

The WK2132 is available in the SSOP16 green lead(pb) free package, which can operate over a wide operating voltage range of 2.5 to 5.0V and is configurable Auto sleep/wake function.

[Note]. : SPI™ is a registered trademark of Motolora Corporation.

2. Basic features

2.1 Overall characteristics

- Supports a wide range of host interfaces: UART, SPI, IIC can be selected
- Large hardware caching with support for 256 levels of FIFO
- Low-power design, can be configured with automatic sleep, automatic wake-up mode (uS level wake-up) wide operating voltage design, operating voltage of 2.5V ~ 5.0V
- Streamlined configuration registers and control words for simple and reliable operation
- Provide industrial grade products
  High-speed CMOS process, sub-serial port rate up to 2Mbps@5V, 1.5Mbps@3.3V, 1Mbps@2.5V
  The SSOP16 is available in a green policy-compliant lead-free package

2.2 Extend the sub-channel UART characteristics

The sub-channel serial port is independently configured, high-speed and flexible:

- Each sub-serial port is full-duplex, and each sub-serial port can be set independently by software to open/close the baud rate, and the sub-serial port can reach up to 2M bps

Each sub-serial character format including data length, stop bit, and parity mode can be set independently

Perfect sub-serial port status query function

The FIFO function can be

implemented to reset the FIFO

function to a single sub-

serial port software:

Each sub-serial port has an independent 256-level transmit FIFO, and the transmit FIFO trigger point is programmable Each sub-serial port has an independent 256-level receiving FIFO and receiving FIFO Trigger point programmable software FIFO enable and empty

FIFO status and counter output

- Error detection:

  Supports parity errors, data frame errors, overflow errors, and Line-Break error detection Supports start bit error detection

- Built-in SIR-compliant IrDA IR transceiver codec with transmission speeds up to 115.2K bit/s

- Interrupt features:
  Line-Break error interrupt
  is supported by a sub-
  serial port receiving FIFO
  timeout interrupts

2.3 UART main interface features

- The main interface is a standard three-wire UART serial port (RX,
- TX, GND), no need for other address signals, control signal line
  baud rate adaptive technology, the highest speed can reach 2M bit/s
- Selectable odd, parity, and no check modes
- Without the serial port expansion mode of address line control, the
- multi-serial port expansion UART main interface can be set to INFRA
  mode through the on-chip protocol processor
- Supports up to 16 bytes of continuous transceiver

2.4 SPI main interface characteristics

- The maximum speed
- of 10M bit/s only
- supports SPI slave
  mode SPI mode 0
- Supports up to 256 bytes of continuous sending and receiving

2.5 IIC main interface characteristics

- SupportSy IIC bus
- interface Maximum
- speed 1M bit/s
- Only IIC slave
  mode is supported
  Supports up to 256 bytes of continuous sending and receiving
-

3. Fields of application

- Multi-serial server/multi-serial card
- Industrial/Automation Field
- RS-485 Control Wireless
- data transmission via
- 2G/3G/4G
  Telematics platform/telematic
  GPS positioning system Remote
  Automatic Meter Reading (AMR)
  system
  POS/Tax Control
  POS/Financial
  Instruments
  DSP/Embedded Systems

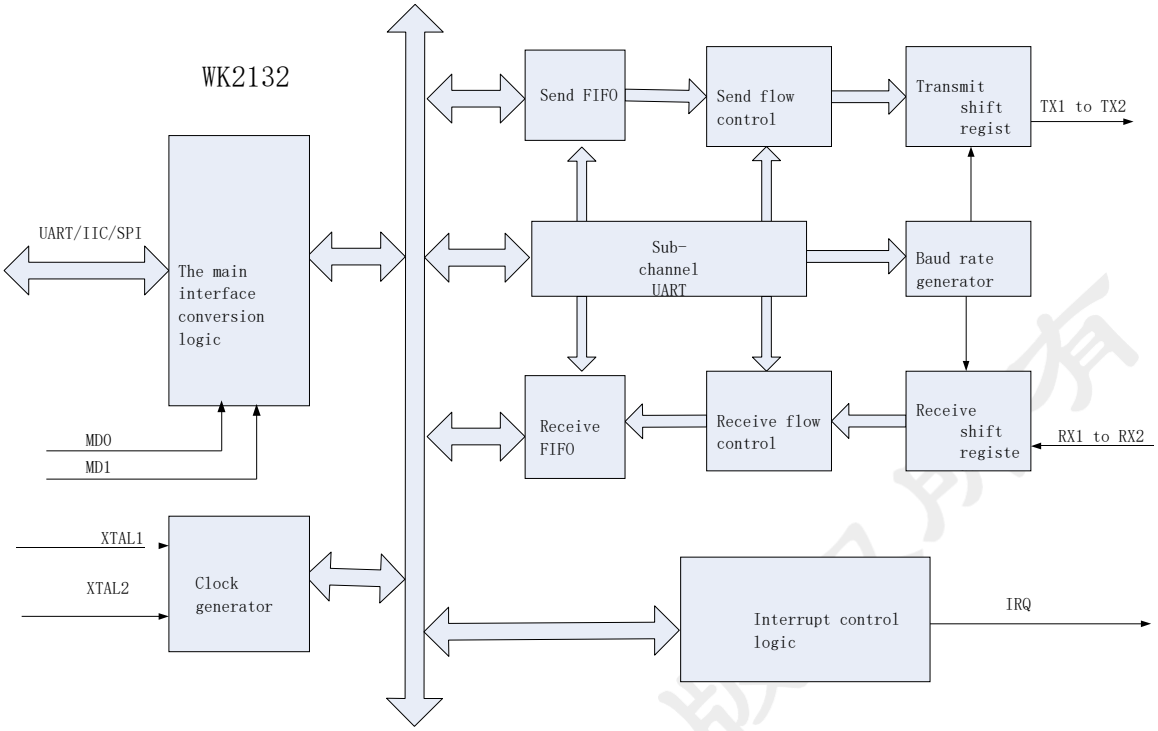
4. Ordering Information

Table 4.1 WK2132 Ordering Information

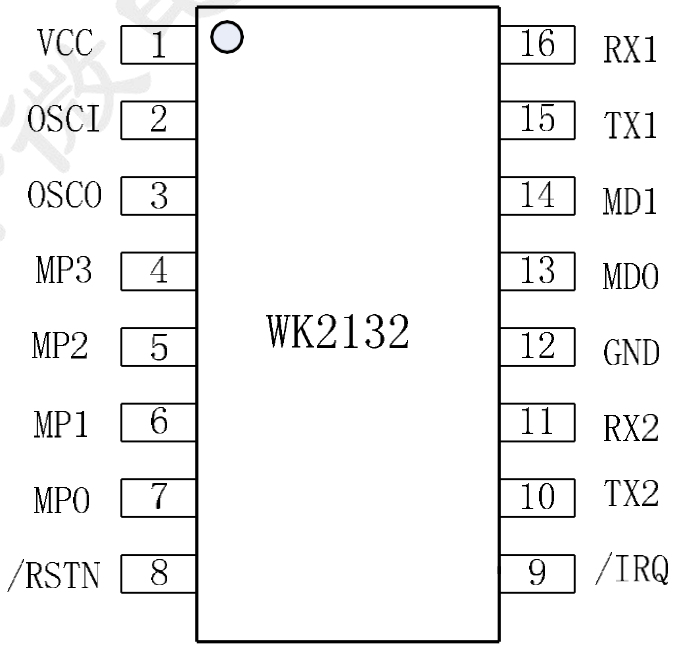
Product model	encapsulation	illustrate
WK2132-ISSG	SSOP16 lead (Pb) free package	General Industrial Grade; Operating temperature -45° C~+85° C

5. Block diagram

Figure 5.1 WK2132 Block Diagram



6. Package pins



6.2 Pin Description

Table 6.2 WK2132 pin description

name	Pins	type	description
VCC	1	-	Power supply 2.5V~5V operating voltage
OSCI	2	I	Crystal input. Note: A resistor of 1 M in parallel with the crystal is required.
OSCO	3	Or	Crystal oscillator output.
MP3	4	I/O	When the main interface is SPI, the function pin for SSEL (SPI chip selection): active low; When the main interface is IIC, it is the IA1 (IIC device address high) function pin; When the main interface is UART, it is the IR (main port infrared communication mode) function pin; IR=0 Infrared communication mode; IR=1 Ordinary UART communication mode; IR defaults to high.
MP2	5	I/O	When the main interface is SPI, it is the SCLK (SPI clock input) function pin; When the main interface is an IIC, it is an SCL (IIC clock input) function pin; When the main interface is UART, it is the MRX (Main Port UART Receive) function pin.
MP1	6	I/O	When the main interface is SPI, it is a MOSI function pin; When the main interface is an IIC, it is the IA0 (IIC device address low) function pin; When the main interface is A UART, the FUNCTION PIN is the MTX (Main Port UART Transmit).
MP0	7	I/O	When the main interface is SPI, it is the MISO function pin; When the main interface is an IIC, it is an SDA function pin; When the main interface is UART, it is NC (empty).
RSTN	8	I	Hardware reset pin, low level reset is active
IRQ	9	Or	Interrupts the output signal, active low. It is recommended to connect an external pull-up resistor, typically 5.1K
GND	12	-	Power ground
MD0 MD1	13 14	I	Main interface mode selection signal: MD1 MD0=00 SPI interface; MD1 MD0=10 IIC interface; MD1 MD0=11 UART interface; M1 M0 chip built-in pull-up circuit, M1 M0 = 11 when suspended;

RX1 RX2	16 11	I	Sub-channel serial serial data input. RX inputs the serial data of the connected data UART into the corresponding pin of the WK2132.
TX1 TX2	15 10	Or	Sub-channel serial serial data output. TX outputs serial data to the device pins connected to it.

7. Register description

7.1 List of Registers

The register address of WK2132 is numbered by 6 digits, the address 000000 ~ 111111, which is divided into global registers and sub-serial registers.

There are 5 global registers, and the addresses of the global registers are listed in Table 7.1

Table 7.1 List of global registers

Register address [5:0].	Register name	type	Register function description

000000	GENA	R/W	Global control registers
000001	GRST	R/W	Global subserial port reset register
000010	GMUT	R/W	Global main serial control register
010000	GAMES	R/W	Global interrupt registers
010001	GIFR	R	Global interrupt flag register

There are 16 sub-serial port registers, which are arranged as C1C0 REG[3:0], the high two bits are the sub-serial port channel number, and the lower 4 bits are the register addresses, pressed

The register addresses of the lower 4 bits are listed in Table 7.2

Table 7.2 Sub-serial control registers

Register address [3:0].	Register name	type	Register function description	
(C1.C0) 0011	SPAGE	R/W	Substring page control registers	
(C1.C0) 0100	SCR	R/W	Sub-serial port control register	SPAGE0
(C1.C0) 0101	LCR	R/W	Substring configuration register	SPAGE0
(C1.C0) 0110	FCR	R/W	Sub-serial FIFO control register	SPAGE0
(C1.C0) 0111	SAYS	R/W	Substring interrupt enable register	SPAGE0
(C1.C0) 1000	SIFR	R/W	Subserpin interrupt flag register	SPAGE0
(C1.C0) 1001	TFCNT	R	The subserial port sends a FIFO count register	SPAGE0
(C1.C0) 1010	RFCNT	R	The subserial port receives the FIFO count register	SPAGE0
(C1.C0) 1011	FSR	R	Subserial PORT FIFO status register	SPAGE0
(C1.C0) 1100	LSR	R	The subserial port receives the status register	SPAGE0
(C1.C0) 1101	FDAT	R/W	Subserial PORT FIFO data register	SPAGE0
(C1.C0) 0100	BAUD1	R/W	Substring port baud rate configuration register high byte	SPAGE1
(C1.C0) 0101	BAUD0	R/W	Substring port baud rate configuration register low byte	SPAGE1
(C1.C0) 0110	PRISONER	R/W	Sub-serial port baud rate configuration register fractional portion	SPAGE1
(C1.C0) 0111	RFTL	R/W	The subserial port receives the FIFO interrupt trigger point configuration mail Memory	SPAGE1
(C1.C0) 1000	TFTL	R/W	The subserial port sends a FIFO interrupt trigger point configuration mail Memory	SPAGE1

C1, C0: sub-channel number, 00 corresponds to sub-serial port 1, 01 corresponds to sub-

serial port 2

7.2 Register description

7.2.1 GENA global control register: (000000).

bit	Reset the value	Feature description	type
Bit7	1	M1 M1 pin level state (M1 defaults to high).	R
Bit6	1	MO MO pin level state (MO defaults to high).	R
Bit5	1	RSV (reserved bit).	R
Bit4	1	RSV (reserved bit).	R
Bit3	0	RSV (reserved bit).	W/R

Bit2	0	RSV (reserved bit).	W/R
Bit1	0	UT2EN sub-serial port 2 clock enable bit (shut down the sub-serial clock for lower power consumption) 0: Not enabled 1: Enable	W/R
Bit0	0	UT1EN sub-serial port 1 clock enable bit (shut down the sub-serial clock for lower power consumption) 0: Not enabled 1: Enable	W/R

2 GRST Global Subserial Reset Register: (000001).

bit	Reset the value	Feature description	type
Bit7	0	RSV (reserved bit).	R
Bit6	0	RSV (reserved bit).	R
Bit5	0	UT2SLEEP sub-serial port 2 sleep state bit (reduces power consumption, can automatically wake up) 0: not hibernating 1: Dormant	R
Bit4	0	UT1SLEEP subseries 1 sleep status bit (reduces power consumption, automatically wakes up) 0: Not hibernated 1: Dormant	R
Bit3	0	RSV (reserved bit).	W1/R0
Bit2	0	RSV (reserved bit).	W1/R0
Bit1	0	UT2RST sub-serial port 2 soft reset control bit 0: Unreplex sub-serial port 2 1: Reset sub-serial port 2	W1/R0
Bit0	0	UT1RST subserpin port 1 soft reset control bit 0: Unreplex sub-serial port 1 1: Reset sub-serial port 1	W1/R0

3 GMUT Global main serial control register: (000010).

bit	Reset the value	Feature description	type
Bit7	0	RSV (reserved bit).	W1/R0
Bit6 --- 4	0	RSV (reserved bit).	R0
Bit3	0	The PAEN main serial port check enables the control bit 0: No check 1: Enable check (determine the check mode according to the configuration of PAM1, PAM0).	W/R

Bit2 --- 1	0	PAM1—0 Main serial port calibration mode enable control position when PAEN=1 main When serial port check enable: 00: Force 0 check ; 01: Odd verification ; 10: Parity ; 11: Mandatory 1 check;	W/R
Bit0	0	The GSTPL main serial port stop bit length setting bit 0: 1bit 1: 2bits	W/R

4 GIER Global Interrupt Register: (010000).

bit	Reset the value	Feature description	type

Bit7 --- 5	000	RSV (reserved bit).	R
Bit4	0	RSV (reserved bit).	W/R
Bit3	0	RSV (reserved bit).	W/R
Bit2	0	RSV (reserved bit).	W/R
Bit1	0	UT2IE sub-serial port 2 interrupt enable control bit 0: not enabled 1: Enable	W/R
Bit0	0	UT1IE sub-serial port 1 interrupt enable control bit 0: Not enabled 1: Enable	W/R

3 GIFR Global Interrupt Flag Register: (010001).

bit	Reset the value	Feature description	type
Bit7 --- 4	000	RSV (reserved bit).	R
Bit3	0	RSV (reserved bit).	R
Bit2	0	RSV (reserved bit).	R
Bit1	0	UT2INT subserpin 2 interrupt flag bit 0: Non-disruptive 1: There is an interruption	R
Bit0	0	UT1INT subshort 1 interrupt flag bit 0: Non-disruptive 1: There is an interruption	R

4 SPAGE sub-serial page control register: (0011).

bit	Reset the value	Feature description	type
Bit7 --- 1	000000	RSV (reserved bit).	R
Bit0	0	PAGE Subserial Page Control Bits (Subserial registers are distributed between PAGE0 and PAGE1 , switching between different pages, controlled by this register). 0：PAGE0 1：PAGE1	W/R

7 SCR sub-serial control register: (PAGE0:0100).

bit	Reset the value	Feature description	type
Bit7 --- 3	000	RSV (reserved bit).	W/R

Bit2	0	SLEEPEN sub-serial dormant enable bit 0: Not enabled 1: Enable	W/R
Bit1	0	The TXEN subserpin port sends the enable bit 0: Not enabled 1: Enable	W/R
Bit0	0	The RXEN subserpin port receives the enable bit 0: Not enabled 1: Enable	W/R

LCR sub-serial configuration register: (PAGE0:0101).

bit	Reset the value	Feature description	type
Bit7 --- 6	00	RSV (reserved bit).	W/R
Bit5	0	BREAK sub-serial port Line-Break output control bit 0: Normal output 1: Line-Break output (TX forced output 0).	W/R
Bit4	0	IREN sub-serial port infrared enable bit 0: Normal mode 1: IR mode	W/R
Bit3	0	PAEN sub-serial port check enable bit 0: No check digit (8 bits of data). 1: There is a check digit (9 bits of data).	W/R
Bit2 --- 1	0	PAM1—0 Sub-serial port calibration mode selection bit when PAEN=1 sub-serial port When validation is enabled: 00:0 validation ; 01: Odd verification ; 10: Parity ; 11:1 Validation	W/R
Bit0	0	STPL sub-serial port stop length control bit 0：1bit 1： 2bits	W/R

FCR sub-serial F IFO control register: (PAGE0:0110)

bit	Reset the value	Feature description	type
Bit7 --- 6	00	TFTRIG[1:0] Sub-serial port sends FIFO contact setting bits When TFTL[7:0] equals 0: 00: 8Byte 01:16 Bytes 10: 24 Bytes 11:30 Bytes	W/R
Bit5 --- 4	00	RFTRIG[1:0] sub-serial port receives FIFO contact setting bits When RFTL [7:0] equals 0: 00: 8Byte 01:16 Bytes 10: 24 Bytes 11:28 Bytes	W/R
Bit3	0	The TFEN subserial port sends the FIFO enable bit 0: Not enabled 1: Enable	W/R

Bit2	0	The RFEN subserial port receives the FIFO enable bit 0: Not enabled 1: Enable	W/R
Bit1	0	The TFRST subserpin port sends a FIFO reset (the bit writes 1 reset and automatically sets 0 when completed). 0: Reset is not enabled 1: Reset the FIFO	W1/R0
Bit0	0	The RFRST subserial port receives the FIFO reset bit (this bit writes 1 reset and automatically when done.) Set 0).	W1/R0

		0: Reset is not enabled 1: Reset the FIFO	

■ SIER subserial interrupt enable register: (PAGE0:0111).

bit	Reset the value	Feature description	type
Bit7	0	FERR_IEN receive FIFO data error interrupt enable bits 0: Disables receiving FIFO data error interrupts 1: Enables an error interrupt to receive FIFO data	W/R
Bit6	0	RSV (reserved bit).	W/R
Bit5	0	RSV (reserved bit).	W/R
Bit4	0	RSV (reserved bit).	W/R
Bit3	0	TFEMPTY_IEN sends fifo null interrupt enable bits 0: Disables sending a FIFO null interrupt 1: Enables the sending FIFO null interrupt	W/R
Bit2	0	TFTRIG_IEN sends the FIFO contact interrupt enable bit 0: Disable sending FIFO contact interrupts 1: Enables sending FIFO contact interrupts	W/R
Bit1	0	RXOVT_IEN receives the FIFO timeout interrupt enable bit 0: Disables receiving FIFO timeout interrupts 1: Enables receive FIFO timeout interrupt	W/R
Bit0	0	RFTRIG_IEN Receive FIFO contact interrupt enable bits 0: Disable receiving FIFO contact interrupts 1: Enables the receive FIFO contact interrupt	W/R

■ SIFR subserial interrupt flag register: (PAGE0:1000).

bit	Reset the value	Feature description	type
Bit7	0	FERR_INT Receive FIFO Data Error Interrupt Flag Bit 0: No receive FIFO data error interrupt 1: There is an interrupt to receive FIFO data errors	W/R
Bit6	0	RSV (reserved bit).	W/R
Bit5	0	RSV (reserved bit).	W/R
Bit4	0	RSV (reserved bit).	W/R
Bit3	0	TFEMPTY_ INT sends the FIFO null interrupt flag bit 0: No send FIFO null interrupt 1: There is an empty interrupt that sends FIFO	W/R
Bit2		TFTRIG_ in the INT sends the FIFO contact interrupt flag bit 0: No send FIFO contact interruption 1: There is a sending FIFO contact interrupt	W/R

Bit1		RXOVT_ INT receives the FIFO timeout interrupt flag bit 0: No receive FIFO timeout interrupt 1: There is a receive FIFO timeout interrupt	W/R
Bit0	0	RFTRIG_ INT receives the FIFO contact interrupt flag bit 0: No receive FIFO contact interrupt	W/R

		1: There is a receive FIFO contact interrupt	

12 The TFCNT subserial port sends the FIFO count register: (PAGE0:1001).

bit	Reset the value	Feature description	type
Bit7 -- 0	00000000	The number of data sent by the subserial port in the FIFO	R

13 The RFCNT subserial port receives the FIFO count register: (PAGE0:1010).

bit	Reset the value	Feature description	type
Bit7 -- 0	00000000	The number of data received by the subserial port in the FIFO	R

14 FSR 子串口 FIFO 状态寄存器: （PAGE0:1011）

bit	Reset the value	Feature description	type
Bit7	0	The RFOE subserial port receives a data overflow error flag in the FIFO 0: No OE error 1: There is an OE error	R
Bit6	0	The RFBI subserial port receives data from the FIFO with a Line-Break error 0: No Line-Break error 1: There is a Line-Break error (the Rx signal is always 0, including the check digits and stop bits).	W/R
Bit5	0	The RFFE subserial port receives the data frame error flag bit in the FIFO 0: No FE error 1: There is an FE error	W/R
Bit4	0	The RFPE subserial port receives the data validation error flag bit in the FIFO 0: No PE error 1: There is a PE error	W/R
Bit3	0	The RDAT subserial port receives the FIFO null flag bit 0: The sub-serial port receives FIFO empty 1: The sub-serial port receives the FIFO is not empty	W/R
Bit2	0	The TDAT subserial port sends the FIFO null flag bit 0: The subserial port sends a FIFO empty 1: The sub-serial port sends FIFO is not empty	W/R
Bit1	0	The TFULL subserpin port sends the FIFO full flag bit 0: The sub-serial port sends a FIFO that is not full 1: The sub-serial port sends FIFO full	W/R

Bit0	0	The TBUSY subserial port sends the TX busy flag bit 0: The sub-serial port sends TX empty 1: Sub-serial port sendS TX busy	W/R

3 LSR subserial port receives status register: (PAGE0:1100).

bit	Reset the value	Feature description	type
Bit7 - 4	0	RSV (reserved bit).	
Bit3	0	The OE subserial port receives the currently read byte overflow fault flag in the FIFO 0: No OE error	R

		1: There is an OE error	
Bit2	0	The BI subserput receives the currently read bytes in the FIFO line-break error flag bit 0: No Line-Break error 1: There is a Line-Break error (the Rx signal has always been a state of 0, including the check digit.) and stop bit inside).	R
Bit1	0	The FE subserial port receives the byte frame error flag that is currently being read in the FIFO 0: No FE error 1: There is an FE error	R
Bit0	0	The PE subserial port receives the byte check error flag bit that is currently read in the FIFO 0: No PE error 1: There is a PE error	R

6 FDAT sub-serial PORT FIFO data register: (PAGE0:1101).

bit	Reset the value	Feature description	type
Bit7 -- 0	00000000	When writing: Writes data sent to the FIFO by the subserial port On read operation: Read out the data of the subserial port receiving the FIFO	W/R

7 BAUD1 subserial port baud rate configuration register high byte: (PAGE1: 0100).

bit	Reset the value	Feature description	type
Bit7 --- 0	00000000	BAUD [15:8] Subserial port baud rate configuration register high byte	W/R

8 BAUD0 sub-serial port baud rate configuration register low byte: (PAGE1:0101).

bit	Reset the value	Feature description	type
Bit7 --- 0	00000000	BAUD [7:0] Subserial port baud rate configuration register low byte	W/R

9 PRES sub-serial port baud rate configuration register fractional part: (PAGE1:0110).

bit	Reset the value	Feature description	type
Bit7 --- 4	0000	RSV	R
Bit3 --- 0	0000	PRES[3:0]	W/R

2 RFTL subserial receive FI FO trigger interrupt register: (PAGE1:0 111)

bit	Reset the value	Feature description	type
Bit7 --- 0	00000000	Receive FIFO contact control	W/R

2 The TFTL subserial port sends FIFO trigger interrupt register: (PAGE1:100 0)

bit	Reset the value	Feature description	type
Bit7 --- 0	00000000	Send FIFO contact controls	W/R

8. Global feature description

8.1 Reset

The WK2132 is a low-level reset.

The reset values for each register are listed in the 7.2 register table.

During and after the reset, each sub-serial port is in a state where transceiver is prohibited. When the sub-serial port is in the networking mode, this feature makes the sub-node where the sub-serial port is located not interfere with other nodes of the network during power-up and reset.

Each sub-serial port can be independently implemented software reset.

8.2 Clock selection

The WK2132 can optionally use a crystal oscillator clock as the clock source for the chip. Note: A 1 M start-up resistor in parallel with the crystal is required. See you Figure 8.2

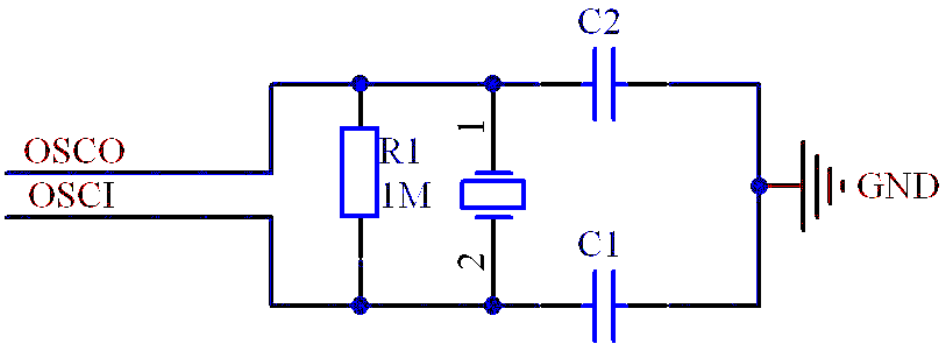
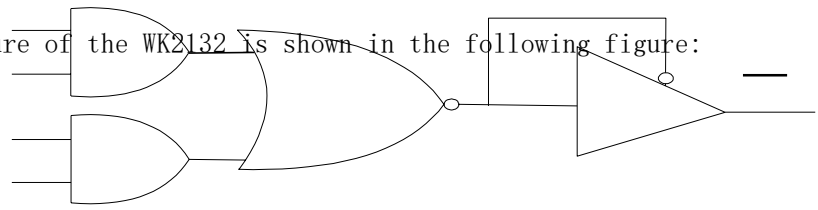


Figure 8.2 WK2132 clock circuit

8.3 Interrupt control

The WK2132 has two levels of interrupts: sub-serial interrupts and global interrupts. When the IRQ pin indicates an interrupt, the current interrupt type can be determined by reading the global interrupt register GIFR, and then reading the corresponding interrupt status register to determine the current interrupt source.

The interrupt structure of the WK2132 is shown in the following figure:



u art 1 _ ir eq u art1_ i req_en

uart 2 _ ireq u

Figure 8.3 WK2132 in a broken knot composition

Each sub-serial port of WK2132 has an independent interrupt system, including: FIFO data error interrupt, send FIFO empty interrupt, send

Send FIFO trigger point interrupt, receive FIFO timeout interrupt, receive FIFO trigger point interrupt.

When either interrupt is enabled, the interrupt condition is met to produce a corresponding interrupt.

8.3.1 FIFO data error interrupt

A FIFO data error interrupt indicates that there is currently one or more data errors in the received FIFO, and the conditions that produce the error include OE (Data Overflow Error), FE (DataFrame Error), and PE (Parity Error), BE (Line-Break Error). ）。

Once there is an error in the received FIFO, when the FSR register is read, the interrupt disappears; This can also be done by clearing the erroneous data

Clear the interrupt.

8.3.2 Send a FIFO null interrupt

When there is no data in the sending FIFO, the interrupt is generated. When the number of data in the send FIFO is greater than the set send FIFO trigger point , the interrupt is cleared.

8.3.3 Send a FIFO trigger point interrupt

This interrupt occurs when the number of data in the sending FIFO is less than the set sending FIFO trigger point. The interrupt is cleared when the number of data in the send FIFO is greater than the set send FIFO trigger point.

8.3.4 Receives a FIFO timeout interrupt

When the number of received FIFOs is less than the set receive FIFO trigger point and there is no data within 4 bytes of the RX pin, it is generated

The interrupt. The interrupt disappears when the data in the received FIFO is read away or the RX continues to receive data.

8.3.5 Receive FIFO trigger point interrupt

This interrupt occurs when the number of data received in the FIFO is greater than the set transmit FIFO trigger point. The interrupt is cleared when the number of received FIFOs is less than the set transmit FIFO trigger point.

8.4 Infrared mode operation

Both the main serial port and the sub-serial port of WK2132 can be set to become infrared communication mode. When the WK2132's UART is set to IrDA mode, it can communicate with devices that conform to the SIR infrared communication protocol standard or be applied directly to optically isolated communication.

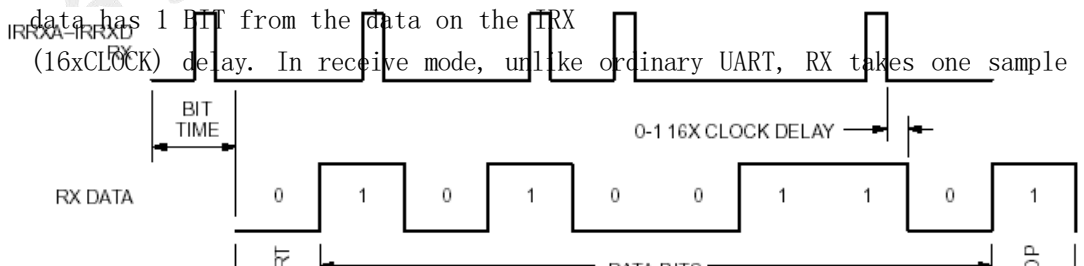
In IrDA mode, the period of one-bit data is shortened to 3/16 of the ordinary UART one-bit data, less than 1/16 of the baud period

The pulse will be ignored as interference.

8.4.1 Infrared receive operation

The corresponding figure between the timing of infrared data reception and ordinary UART data reception is shown in Figure 8.4.1: IRX is the received infrared data signal, and RX is the data decoded by infrared data. The decoded data has 1 BIT from the data on the IRX

(16xCLOCK) delay. In receive mode, unlike ordinary UART, RX takes one sample in the



middle of the pulse (3 samples to distinguish from ordinary UART). The IrDA decoder decodes the pulse of the 3/16 baud period on the IRX to data 0 and the persistent low level to data 1.

Figure 8.4.1 Infrared Receive Timing

8.4.2 Infrared send operation

The corresponding figure of infrared data transmission and ordinary UART data transmission is shown in Figure 8.4.2, TX is the ordinary UART data transmission timing, and IRTX is the infrared transmission timing. When data 0 is sent, the irred encoder will generate a 3/16-bit wide pulse sent through the TX. When data 0 is sent, leave the level low unchanged.

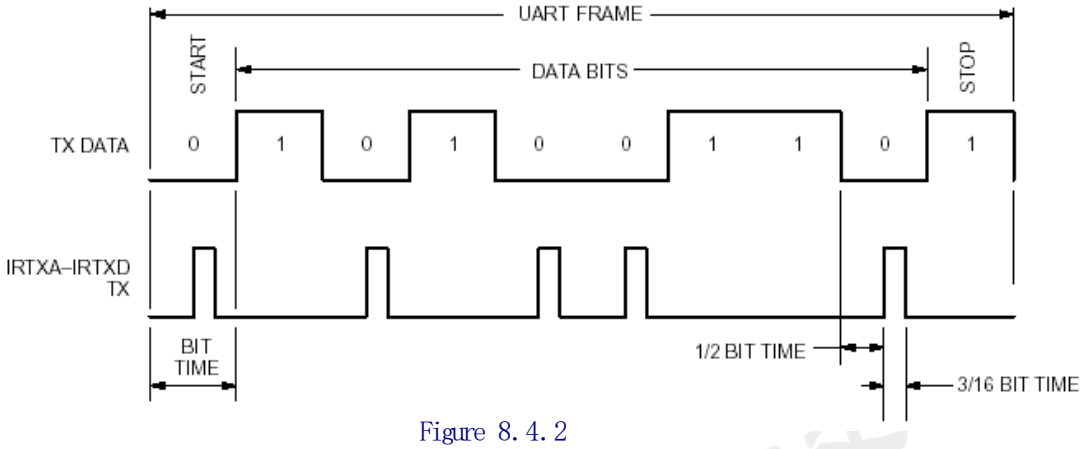


Figure 8.4.2

8.5 Programmable baud rate generator

The main serial port and sub-serial port of the WK2132 use the same independent programmable baud rate generator. This baud rate generator generates a division factor of a 16X system clock, which can be set by software.

The following table shows the serial port baud rate setting table at different system clock frequencies:

Table 8.5.1

BAUD BAUD[15-0]	PRISONER	baud rate Dark= 1.8432MHz	baud rate Dark= 3.6864MHz	baud rate Dark= 7.3728MHz	baud rate Dark= 11.0592MHz	baud rate Dark= 14.7456MHz
0X0002	0X00	38400	76800	153600	230400	307200
0X0005	0X00	19200	38400	76800	115200	153600
0X000b	0X00	9600	19200	38400	57600	76800
0X0017	0X00	4800	9600	19200	28800	38400
0X002f	0X00	2400	4800	9600	14400	19200
0X005f	0X00	1200	2400	4800	7200	9600
0X00bf	0X00	600	1200	2400	3600	4800
0X017f	0X00	300	600	1200	1800	2400
0X0000	0X00	115200	230400	460800	691200	921600
0X0001	0X00	57600	115200	230400	345600	460800
0X0003	0X00	28800	57600	115200	172800	230400
0X0007	0X00	14400	28800	57600	86400	115200
0X000f	0X00	7200	14400	28800	43200	57600
0X001f	0X00	3600	7200	14400	21600	28800
0X003f	0X00	1800	3600	7200	10800	14400
0X007f	0X00	900	1800	3600	5400	7200

8.5.2 Calculation of baud rate under arbitrary crystal oscillation

Calculation formula: $\frac{f_s}{*16 \cdot baud} = Reg$

Note: f_s is the system clock, $baud$ is the baud rate that needs to be set, and Reg is the result of the calculation (usually accurate to two decimal points bit)

Reg integer part minus one and converted to hexadecimal write {BAUD1,BAUA0}; If there is still a decimal part, the first decimal part is written to THE PRES. If there is no fractional part, just write the integer part {BAUD1, BAUA0}, PRES to 0.

Example 1: f_s = 11.0592MHz, $baud$ =115200 According to the formula, Reg=6 is obtained. Then the data filled in the register is: BAUD1=0X00; BAUD0=0X05; PRES=0X00.

Example 2: f_s = 12MHz, $baud$ = 115200 According to the formula, Reg= 6.51 (accurate to two decimal places) is obtained. Then fill in the deposit

The data of the device is BAUD1=0X00; BAUD0=0X05; PRES=0X05.

Example 3: High baud rate calculation

BAUD BAUD[15-0]	PRISONER	baud rate Dark= 8MHz	baud rate Dark= 16MHz	baud rate Dark= 24MHz
0X0000	0X00	500K	1M	1.5M
0X0001	0X00	250K	500K	750K
0X0003	0X00	125K	250K	375K

8.6 Data formatting

8.6.1 Validation mode

The WK2132's UART can provide a mandatory checksum, computational checksum and no checksum data format via LCR (Sub-Serial Port Configuration Register) to set:

Force check mode

WK2132 supports strong 1 checksum, strong 0 checksum and user-specified check mode. In this mode, the validation setting only affects data transmission, and data reception ignores parity.

In RS-485 mode, it is recommended to use forced check mode, in which data and addresses can be easily distinguished.

Compute validation mode

WK2132 supports 1 check, 0 check, odd check, and parity modes. In this mode, both the received and sent data are parity computed.

8.6.2 The length of the data

WK2132 supports 1 or 2-bit stop mode, the main serial port through GMAT GSTPL setting, sub-serial port through LCR.STPL setting

Place.

8.7 Sleep and wake up automatically

WK2132 supports hibernation and auto-wake modes, and each sub-serial port can be set to hibernate individually.

Dormancy conditions: 1, SCR. SLEEPEN=1

2. Receive FIFO and send FIFO to be empty

3. There is no data reception on RX and no data transmission on TX
4. There is no interruption in the sub-serial port

When the appeal conditions are met at the same time, and the above state is maintained for 4 Bytes time, the sub-string port automatically enters the dormant state, the sub-string

The clock of the port is automatically turned off to reduce power consumption. At this time, read grest to determine whether the sub-serial port enters the sleep state.

When the sub-serial port enters the dormant state, one of the following conditions is met, and the sleeping sub-serial port can be automatically awakened, and the grst is read to determine whether the sub-serial port is awakened.

Wake-up condition: 1 , RX to start receiving data

2. Send FIFO write data to the sub-serial port
3. CTS pin level change

8.8 FIFO contact settings

WK2132 supports each sub-serial port to set different trigger points, and the receiving FIFO and sending FIFO can independently set different trigger points. There are two ways to set the contact: 1. Configure the fixed contact: through the TFTRIG [1:0] and RFTRIG [1:0] bits in the FCR register Fixed programming to configure the trigger point position. 2. Configure any contact: Set any trigger point position by setting the two registers of TFTL and RFTL. The specific configuration is shown in Table 8.8.1

表 8.8.1

TFTL [7:0]	TFTRIG [1:0]		TX Trigger Level	RFTL [7:0]	RFTRIG [1:0]		RX Trigger Level
= =0	0	0	8	= =0	0	0	8
= =0	0	1	16	= =0	0	1	16
= =0	1	0	24	= =0	1	0	24
= =0	1	1	30	= =0	1	1	28
! =0	X	X	TFTL	! =0	X	X	RFTL

9. SPI interface mode operation

9.1 SPI's connection to the host:

The SPI interface shown in Figure 9.1 consists of four signals: MISO: SPI slave device data output. MOSI: SPI slave device data input. SCLK: SPI serial clock.

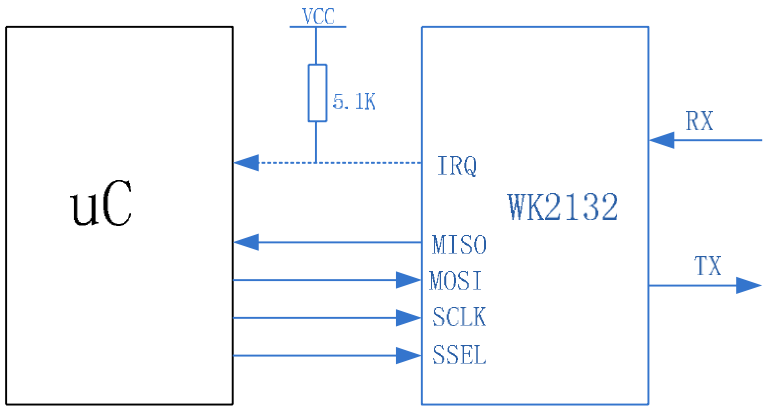


Figure 9.1 SPI connection diagram with host

9.2 Operating Timing of the SPI Interface

The WK2132 operates in slave mode for SPI synchronous serial communication and supports the SPI Mode 0 standard. Implement the host and WK2132 For communication, CPOL=0 (SPI clock polarity select bit) and CPHA=0 (SPI clock phase select bit) need to be set on the host side. The operating timing of the WK2132 SPI interface is as follows:

Write register operation timing as shown in Figure 9 2 Shown: First write a command byte (Command Byte), then write the corresponding data byte, the register address of the data byte automatically increases.

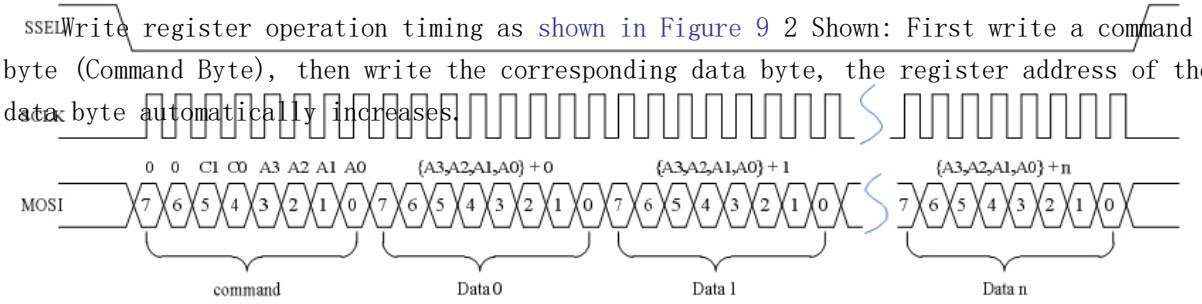


Figure 9.2 SPI Write Register Timing Diagram

Read register operation timing as shown in Figure 9 3 Shown: A command byte is written first, followed by a chip MISO line the corresponding data bytes are returned. The register address that returns the data bytes is automatically incremented.

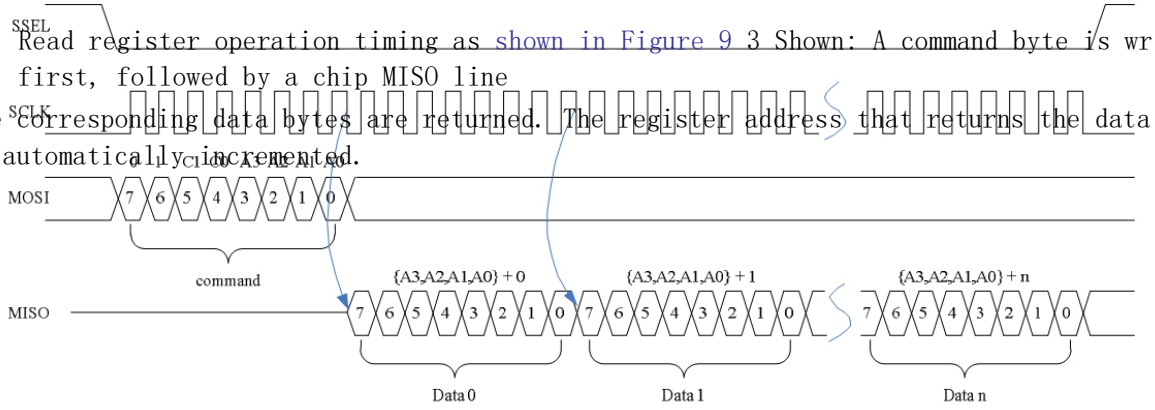


Figure 9.3 SPI Read Register Timing Diagram

写FIFO Operation timing such as图 9.4 As shown: A command byte is written first（Command Byte），The corresponding number is then writtenAccording to bytes.FIFO The address is incremented automatically。

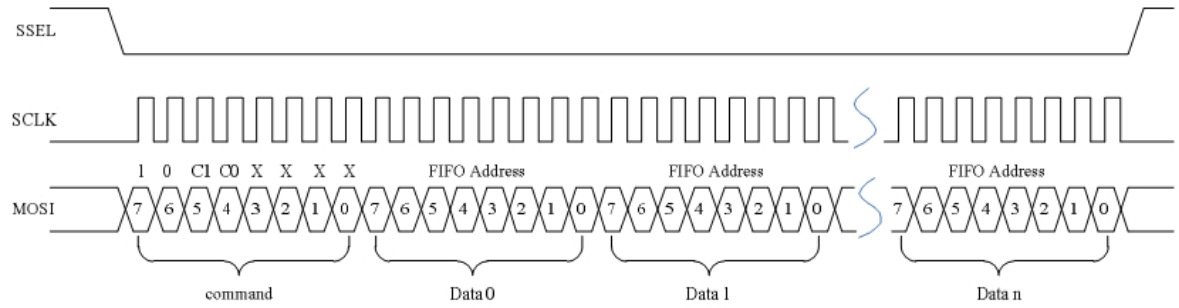


Figure 9.4 SPI Writes FIFO Timing Diagram

Read the FIFO operation timing as shown in Figure 9 5 Shown: A command byte is written

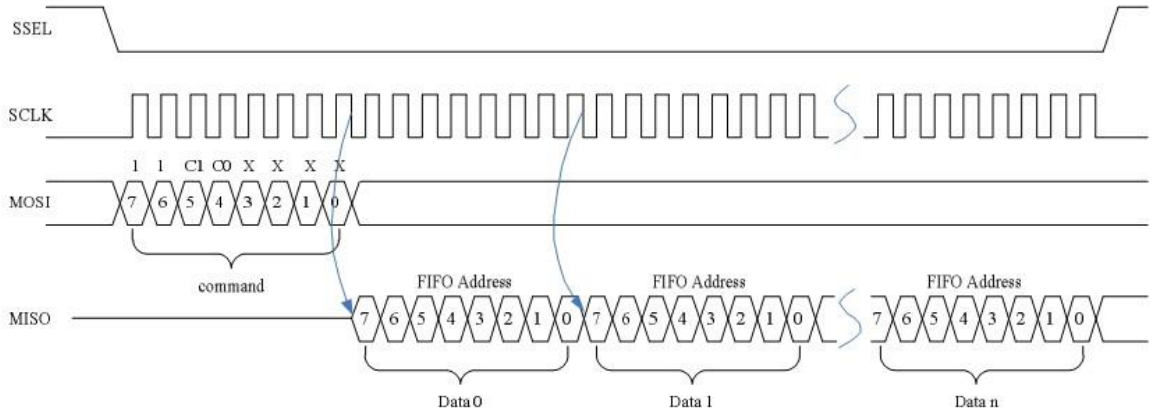


Figure 9.5 SPI Read FIFO Timing Diagram

9.3 SPI Bus Communication Protocol Description:

SPI	Control byte CMD								Data bytes DB (Write N data bytes, registered.) the address of the device is automatically incremented).							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MOSI	0	0	C1	C0	A3	A2	A1	A0	D7t	D6t	D5t	D4t	D3t	D2t	D1t	D0t
MISO	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ

9.3.2. SPI read register

SPI	Control byte CMD	Data bytes DB (Read N data bytes, registered

									the address of the device is automatically incremented).							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MOSI	0	1	C1	C0	A3	A2	A1	A0	X	X	X	X	X	X	X	X

MISO	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	D7t	D6t	D5t	D4t	D3t	D2t	D1t	D0t

9.3.3. SPI 写 FIFO

SPI	Control byte CMD								Data bytes DB (Write N data bytes to {C1C0} (FIFO, the FIFO address is automatically incremented).							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MOSI	1	0	C1	C0	X	X	X	X	D7t	D6t	D5t	D4t	D3t	D2t	D1t	D0t
MISO	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ

9.3.4. SPI 读 FIFO

SPI	Control byte CMD								Data bytes DB (read N from FIFO of {C1C0} Data bytes, FIFO address automatically incremented).							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
MOSI	1	1	C1	C0	X	X	X	X	X	X	X	X	X	X	X	X
MISO	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	D7t	D6t	D5t	D4t	D3t	D2t	D1t	D0t

Description: C1 C0: Sub-serial port channel number 00~11 is divided into sub-serial ports 1 to sub-serial port 4 A3-A0: Sub-serial port is registered The address of the device
D7t... D0t: 8-bit data bytes

10. UART interface mode operation

10.1 The connection of the UART interface to the host

When the main interface of the WK2132 is UART, only RX is required, and the TX is connected to the host. Communication is carried out using the standard UART protocol. The main interface UART can achieve baud rate adaptation. After power-on reset, the 0x55 is written to the WK2132, and the WK2132 can automatically measure the baud rate of the MCU at this time according to the written data and use the main interface UART the

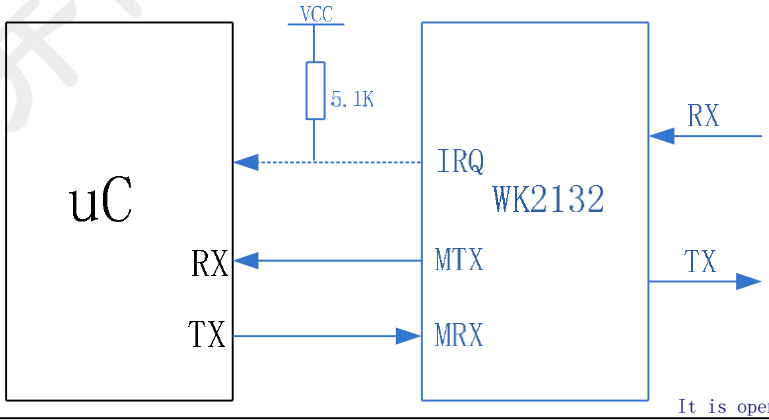


Figure 10.1 Diagram of the UART connector connecting to the host

10.2 Operating Timing of the Main UART Interface

When writing, a command byte is first written to the MRX of the WK2132, followed by the corresponding data byte, which is written

The operating timing (no check mode) is shown in Figure 10.2.1:

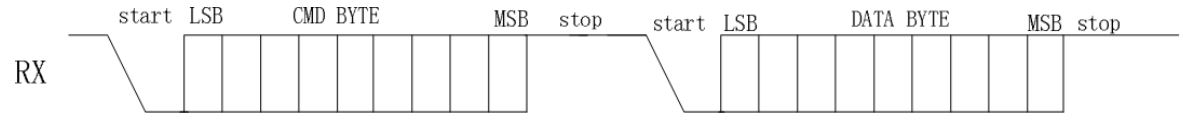


Figure 10.2.1 Timing of UART main socket write operations

When reading operations, first toWK2132的JRXWrite command bytes from which the corresponding data bytes areMTXRead, its operation timing (no check mode) as shown in

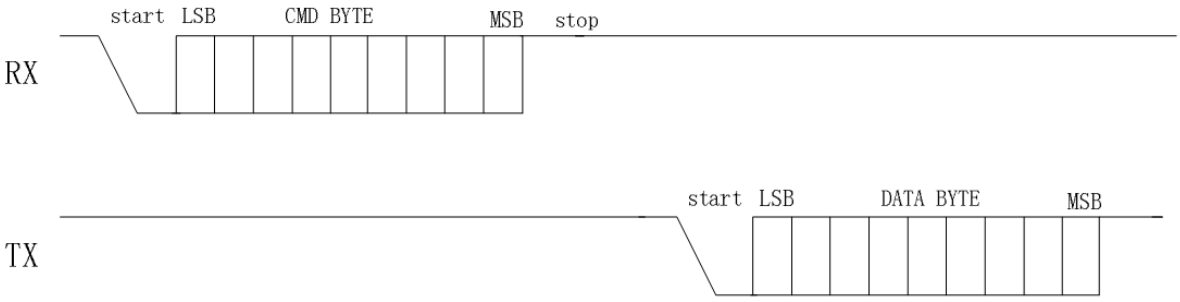


Figure 10.2.2 Timing of UART

10.3 Main UART Communication

10.3.1. Write register:

classify	Control byte CMD								1 data byte DB (downstream).							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
TX	0	0	C1	C0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
RX																

10.3.2. Write FIFO: (Multibyte Write).

classify	Control byte CMD								[N3 N2 N1 N0] data bytes DB (downstream).							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
TX	1	0	C1	C0	N3	N2	N1	N0	D7	D6	D5	D4	D3	D2	D1	D0
RX																

10.3.3. Read register:

classify	Control byte CMD								1 data byte DB (upstream).							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
TX	0	1	C1	C0	A3	A2	A1	N0								
RX									D7	D6	D5	D4	D3	D2	D1	D0

10.3.4. Read FIFO :(Multibyte Read).

classify	Control byte CMD								[N3 N2 N1 N0] data bytes DB (upstream).							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

TX	1	1	C1	C0	N3	N2	N1	N0								
RX									D7	D6	D5	D4	D3	D2	D1	D0

Description:

C1, C0: Sub-serial port channel number, 00~11 corresponds to sub-serial port 1 to sub-serial port 4 respectively. A3, A2, A1, A0: sub-serial port register address;

N3, N2, N1, N0: Number of bytes of data written/read from FIFO; When it is 0000, it indicates that it is followed by 1 data byte; When it is 1111, indicating that 16 bytes of data are followed;

There are two ways to read/write data to the substring port:

a. Read/write register mode, read/write to the sub-serial PORT FIFO register FDAT (1111), can only be read at one time /Write one byte;

b. Read/write FIFO mode, the receiving/sending FIFO directly read/write operations, at a time can read and write up to 16 consecutive data

10.4 Main UART interface IR operation mode

When the main serial PORT IR pin is connected to a high level, the WK2132 main UART works in infrared mode, and the communication between the main UART and the host follows the infrared communication

Protocol, the operating timing of which is referred to 8.8 infrared mode operation.

When the main serial PORT IR pin is low, the WK2132 operates in normal mode.

11. IC interface bus mode operation

The two-wire IIC bus consists of a serial data line SDA and a serial clock line SCL. When the bus is idle, two The wires are pulled to the positive supply voltage through pull-up resistors. Each device has a separate address. As shown in Figure 11

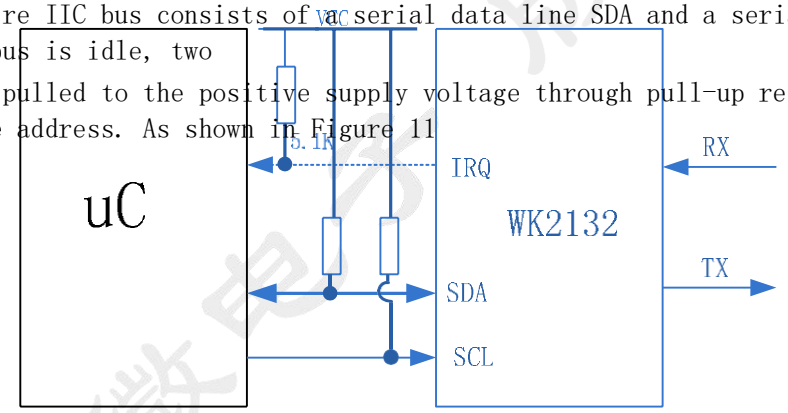


Figure 11 Schematic diagram of the IIC master interface

11.1 Data transmission

Every bit of data is transmitted through a constant pulse. The data on the SDA line with a high SCL must remain stable. Changing the data on the SDA line at this point is considered a control signal. When the SCL is high, the jump of the SDA line data from high to low represents a start bit, and a low-to-high jump represents a stop bit. The bus

is considered busy after the start bit; It is considered idle after the stop bit.

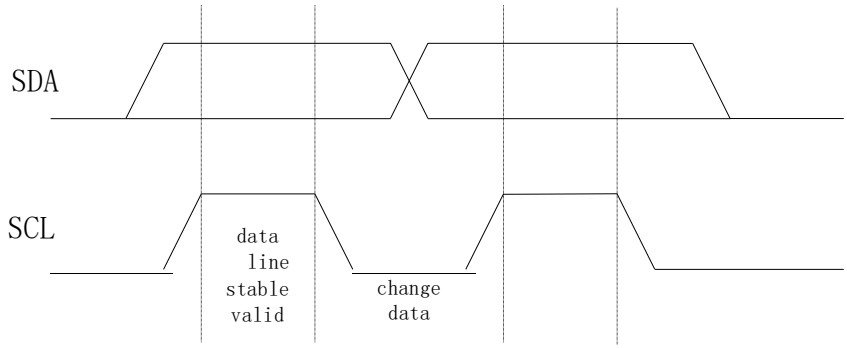


Figure 11.1.1

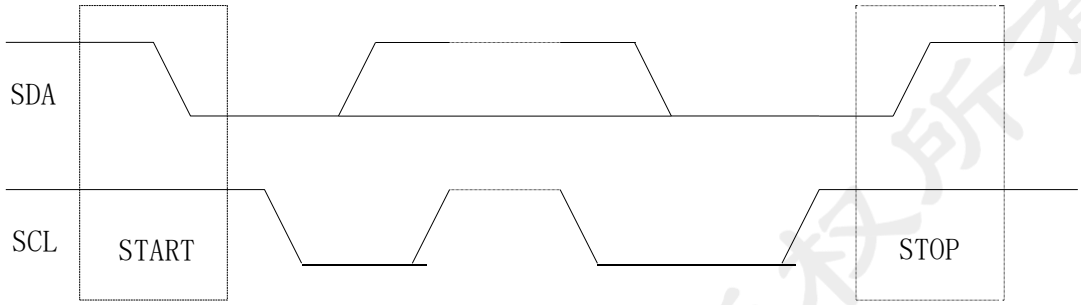


Figure 11.1.2 Start and Stop Bits

The master-to-slave data between the start and stop bits must be 8 bits (bits) long, the high bits in front and must have an answer

Low SDA line.

11.2 Operating timing of the main IIC interface

11.2.1. IIC Write Register:

The write register operation timing is shown in Figure 11.2.1, first write a command byte (Command Byte), then write the register address byte, and finally write the corresponding data byte, the register address of the data byte will automatically increase.

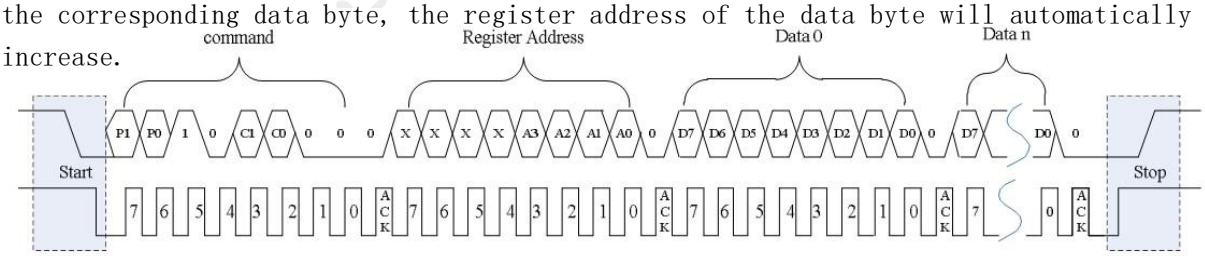


Figure 11.2.1 IIC Write Register Manipulation Timing

11.2.2.IIC Read Register::

The timing of read register operation is shown in Figure 11.2.2: The IIC read register operation is completed in two stages. Write a command byte first (Command Byte), and then write the register address byte to complete the write operation. Immediately after that, start the second operation, write first

A command byte is entered, the corresponding data byte is read in, and the register address is automatically incremented.

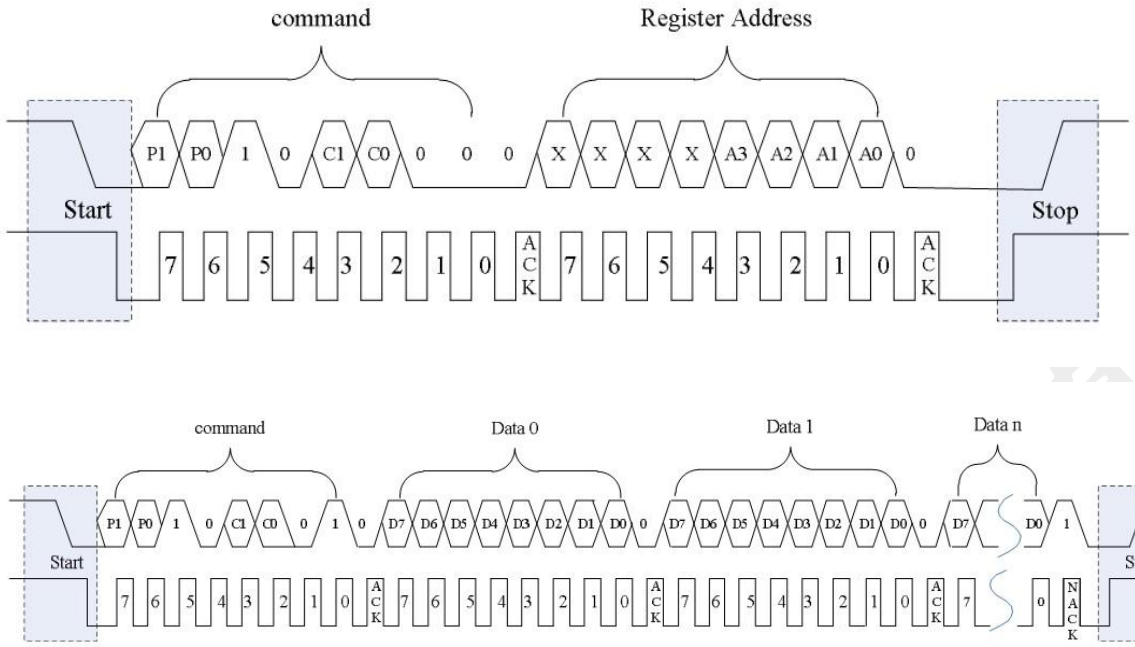


Figure 11.2.2 IIC Read Register Manipulation Timing

11.2.3.IIC写FIFO:

The timing of the write FIFO operation is shown in Figure 11.2.3, where one command byte is written first, followed by N bytes

For data, the FIFO address is automatically incremented.

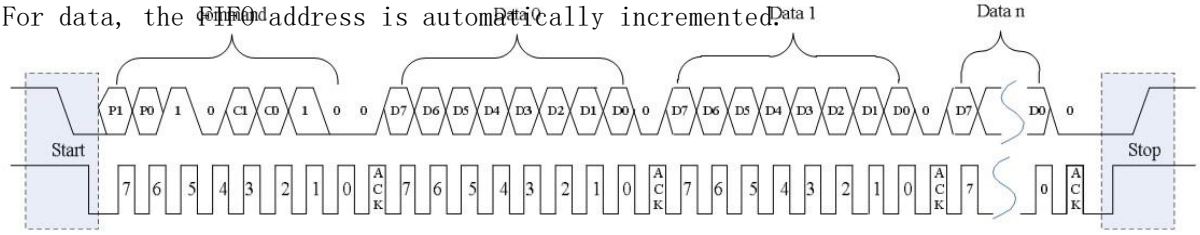


Figure 11.2.3 Timing of IIC Write FIFO Operations

11.2.4.IIC读FIFO:

The timing of the read FIFO operation is shown in Figure 11.2.4, where one command byte is written first, followed by N data bytes, the FIFO The address is incremented automatically.

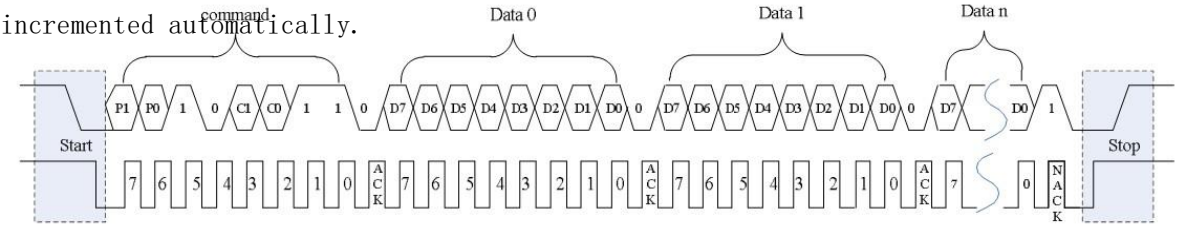


Figure 11.2.4 IIC Read FIFO Operation Timing

11.3 Addres

s:

Each device hanging on the bus must have its own unique address. Before data is transferred on the bus, the host sends it on the bus

Send the slave's address to start a transmission. All slaves compare addresses, and if there is the same address in the network, of course, the host will be answered

Address request. The address is transferred after the start bit of the first byte transferred by a high 2-bit transfer. The address of each device is controlled by the A1A0 pin

Then in the programming, only the value of P1P0 corresponds to the value of IA1 and IA0.

11.4 Transport Protocol:

11.4.1. Write register:

S	Control byte CMD								A	Register address								A	N data bytes		A	P
	P1	P0	1	0	C1	C0	0	0		X	X	X	X	A3	A2	A1	A0		Data0-DataN			

11.4.2. Read register:

S	Control byte CMD								A	Register address								A	P
	P1	P0	1	0	C1	C0	0	0		X	X	X	X	A3	A2	A1	A0		

S	Control byte CMD								A	N-1 data bytes		A	The Nth data byte		N A	P
	P1	P0	1	0	C1	C0	0	1		Data0-Data(N-1)			Date			

11.4.3. 写FIFO:

S	Control byte CMD								A	N data bytes		A	P
	P1	P0	1	0	C1	C0	1	0		Data0-DataN			

11.4.4. 读FIFO:

S	Control byte CMD								A	N-1 data bytes		A	The Nth data byte		N A	P
	P1	P0	1	0	C1	C0	1	1		Data0-Data (N-1)			Date			

Description:

Note: When the MCU does not need to continue receiving data from WK2132, it does not need to issue a reply after receiving the current byte

Just give the answer clock.

C1, C0: sub-serial port channel number, 00 ~11 corresponds to sub-serial port 1 to sub-serial port 4, respectively

A3, A2, A1, A0: Sub-serial register address

P1, P0: is the device address, which is controlled by the chip pins IA1 and IA0

S: Start bit P: Stop bit A: Answer bit On: No answer signal

12.1 Sub-serial port enable/disable

The WK2132 allows each sub-serial channel to be enabled or disabled independently. Sub-serial channels that are not used can be disabled in use.

Subserial channels can receive and send data only if they are enabled.

12.2 Send and receive FIFO control

The WK2132 provides a separate 256-level FIFO to receive and transmit FIFOs. (sub-serial FIFO control register) to set.

12.2.1 Send a FIFO trigger point action

The WK2132 provides independent programmable transmit FIFO trigger point settings for each channel to produce corresponding transmit FIFO trigger point interrupts.

When the SEND FIFO trigger point interrupt enables, the corresponding interrupt occurs when the number of data in the sending FIFO is less than the set trigger point.

12.2.2 Receive FIFO trigger point action

The WK2132 provides independent programmable receive FIFO trigger point settings for each channel to generate a corresponding receive FIFO trigger point interrupt. When the FIFO trigger point interrupt enable is received, the corresponding interrupt is generated when the number of data in the received FIFO is greater than or equal to the set trigger point.

12.2.3 Send enable/disable for FIFOs

After reset, sending FIFOs is disabled. If you want to write data to send a FIFO, you need to enable the send FIFO first.

Whether the data in the sending FIFO is sent depends on whether the corresponding subchannel UART is enabled. Once the corresponding subchannel UART is enabled, the data in the sending FIFO will be sent immediately, otherwise, the data in the sending FIFO will not be sent until the corresponding subchannel is enabled.

12.2.4 Receives enable/disable for FIFOs

After reset, the receive FIFO is disabled. If you want to receive subserial data, you need to first enable the corresponding subserial channel and its receiving FIFO. Only after the corresponding UART and receive FIFO are enabled can the received data be written to the receiving FIFO storage.

If the subserial port channel is enabled and the receive FIFO is disabled, the subserial port can receive data, but the data is not written to the receiving FIFO and is ignored.

12.2.5 Send FIFO empty

When the Transmit FIFO Clear Bit (TFRST) in the FFRR is set to 1, the data in the subchannel sending the FIFO will be emptied and the FIFO will be sent

Both the counter and the pointer will be zeroed.

When the TFRST bit is set to 1, it will be automatically cleared by the hardware after one clock.

12.2.6 Receive FIFO emptying

When the Receive FIFO Empty Bit (RFRST) in the FCR is set to 1, the subchannel receives the data in the FIFO to be emptied and the FIFO is received

Both the counter and the pointer will be zeroed.

When the RFRST bit is set to 1, it will be automatically cleared by the hardware after a clock.

12.2.7 Sends FIFO counters

The WK2132 uses an 8-bit register to reflect the number of data currently sent in the FIFO: when a byte of data is written to the sending FIFO

After sending the FIFO counter, the 1 is automatically added; When a send fifo is sent, the send FIFO counter is automatically minus 1.

Note: When the send FIFO counter is 255 (11111111), the counter becomes 0 if another data is written

（00000000）。 When the send FIFO counter is 1 (00000001), after sending a data, the counter also becomes 0

（00000000）。 Therefore, when the Send FIFO counter is 0, it indicates that the send FIFO is full or empty, in which case it is required

The judgment is made by combining the relevant status bits in the sub-serial port status register (FSR).

12.2.8 Receives FIFO counters

The WK2132 uses an 8-bit register to reflect the number of data currently received in the FIFO: when a byte of data is written to the receiving FIFO

After receiving the FIFO counter, the 1 is automatically added; When the data in a receive FIFO is read, the receive FIFO counter is automatically decremented by 1.

Note: When the receive FIFO counter is 255 (11111111), if one more data is received the counter becomes 0

（00000000）。 When the receive FIFO counter is 1 (00000001), after reading a piece of data, the counter also becomes 0

（00000000）。 Therefore, when the Receive FIFO counter is 0, it indicates that the receive FIFO is full or empty, in which case it is required

The judgment is made by combining the relevant status bits in the sub-serial port status register (FSR).

13. Parameter indicators

13.1 Static parameters for WK2132

Unless otherwise specified, satisfies: VC C= (2.5V±0 2V) or (3 3±0. 3V) or (5V),-40° C to +85° C;

symbol	illustrate	condition	VCC=2.5V		VCC=3.0V		VCC=5.0V		single bit
			least	utmost	least	utmost	least	utmost	
power supply									
VCC	Supply voltage		2.3	2.7	3.0	3.6	4.5	5.0	In
ICC	Working current	3.6864MHz crystal oscillator No load	0.8	2	1	2	2	3	but
ICCSL	Sleep current		150	-	200	-	460	-	uA
Input logic signals									
IN1999, THE NEW	Enter high		1.8	5.0	2.0	5.0	3.6	5.0	In
VIL	Enter a low level		-	0.6	-	0.9	-	1.1	In
IIL	Input leakage current	VI=5.0 or 0V	-	±10	-	±10	-	±10	uA
CI	Input capacitance		-	5	-	5	-	5	pF
Output logical signal									
VOH	Output high	IOH=3mA	1.9	-	2.4	-	4.5	-	In
InOL	Output low level	I OL=-3mA	-	0.4	-	0.4	0	0.4	In
IOL	Output leakage current		-	±10	-	±10	-	±10	uA
Co	Output capacitance		-	5	-	5	-	5	pF

13.2 WK2132Dynamic parameters

symbol	illustrate	condition	VCC=2.5V		VCC=3.0V		VCC=5.0V		single bit
			least	utmost	least	utmost	least	utmost	
FOSI	Crystal oscillator frequency	-	-	16	-	24	-	32	MHz

13.3 Limit parameters for WK2132

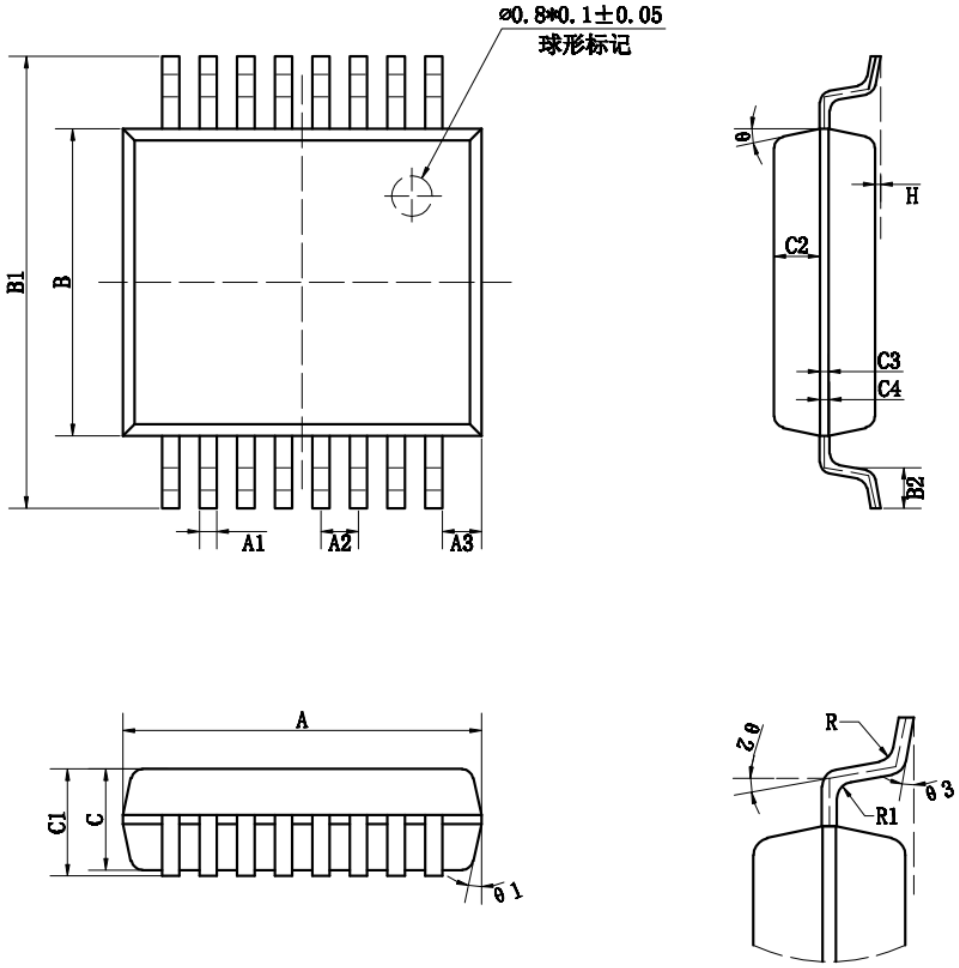
Symbol number	illustrate	condition	least	utmost	unit
VCC	Supply		-	6	In

	voltage		0.5		
VI	Input voltage		-0.5	+5.5	In
INO	Output voltage		-0.5	+5.5	In
PTOL	Total power consumption		-	300	mW
TO	Operating temperature		-40	+85	℃
TSTG	Storage temperature		-65	+150	℃

14. Encapsulation information

The WK2132 is available in SSOP16 lead(s) free green package

Figure 14.1 SSOP16 Encapsulation Information



size / Marking	Minimum (mm).	Maximum (mm).	size / Marking	Minimum (mm).	Maximum (mm).
A	6.15	6.25	C3	0.152	
A1	0.30TYPE		C4	0.172	
A2	0.65TYPE		H	0.05	0.15
A3	0.675TYP E		I	12° TYP4	
B	5.25	5.35	i2	12° TYP4	
B1	7.65	7.95	i2	10° TYPE	
B2	0.60	0.80	i3	0° ～ 8°	
C	1.70	1.80	R	0.20TYPE	
C1	1.75	1.95	R1	0.15TYPE	
C2	0.799				

15. Welding process

WK2132 uses a green material and the pins are pure tin plating. A peak temperature of less than 260° C is recommended and complies with the lead-free scale

The quasi-reflow soldering process is welded.

All SMD device soldering processes are sensitive to humidity (see outer box for humidity levels and conditions) and drying is recommended prior to soldering.

When using manual soldering, you should first solder two diagonal pins to fix them before soldering the other pins. The welding temperature is 300° C

The contact time of the soldering iron with the pin is controlled at 10 Within seconds。

16. Specially stated

This product is not designed for life support systems and aerospace systems, and will not assume any responsibility for all the consequences caused by the application of this product in this field. For the purpose of opening microelectronics, we reserve the right to modify the performance, function and parameters of the product. For products that are officially mass-produced, the modifications made for Kai Microelectronics will be notified to users in the form of announcements.

17. Version history

Versions prior to Version 1.0 were not generally available builds.

version	Date of publication	Modify the content
V1.0	2017.09	Create a file

18. Contact Information

. Please visit the web site for opening microelectronics to get our most New linkage equation. www.wkmic.com

General generation: Shenzhen Hengtairui Technology Co., Ltd. QQ3002931911 old Chen 13148878879