Answers Database

Virtex-4 Aurora - Special reset consideration for Virtex-4 Aurora designs

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Problem Description:

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This Answer Record details a special consideration when designing reset logic around the Aurora Core top level.

Solution 1:

There are two resets that go in to the Virtex-4 Aurora Core:

1. RESET - This port resets the core logic and initialization state machines. It does not reset the MGTs. This reset port must be asserted synchronously to USER_CLK.

2. PMA_INIT - This port re-initializes the MGT by resetting the GT11_INIT blocks. Asserting this port will reset the MGTs and the Aurora Core initialization logic. This reset port must be asserted synchronously to INIT_CLK.

NOTE: These reset ports are not asynchronous. They must be asserted on the appropriate clock edge. RESET must be asserted synchronous to USER_CLK, and PMA_INIT must be asserted synchronous to INIT_CLK.