AR #21012 - Virtex-4 RocketIO - How do I set up the MGT to initialize correctly in my design?

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Description

Keywords: startup, GT11, condition, power

Urgency: Standard

General Description:
How do I set up the MGT to initialize correctly in my design?

Solution

Startup Recommendations

1. After power-up, make sure the inputs TX/RXCLKSTABLE going into the MGT are asserted.

In general, these should be tied to '1'.

For further information, please refer to the RocketIO User Guide, Clocking and Timing Considerations, Clock Distribution, RXCLKSTABLE and TXCLKSTABLE.

The TX/RXLOCK signals will not assert if the TX/RXCLKSTABLE signals do not go High. The TX/RXCLKSTABLE signals start the frequency calibration process whereby the PLL lock is determined.

2. Then issue a TX/RXPMARESET that lasts a minimum of 3 USRCLK cycles.
3. Wait for TX/RXLOCK. (NOTE: In the absence of a serial data stream, the receiver will repeatedly lock and unlock.)
4. Issue a TX/RXRESET that lasts a minimum of 3 USRCLK cycles.
5. Wait for a minimum of 5 USRCLKs.
6. Begin normal data transmission and reception.

The reset minimum widths are specified as 3 USRCLKs. Each clock domain will clock in the reset and release it. Three USRCLKs should be sufficient in all cases. Five USRCLKs are needed to allow the reset to be de-asserted internally.