AR #30411 - MIG v2.2 - Release Notes and Known Issues for ISE 10.1 IP Update 1 (10.1.1)

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Description

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This Release Notes and Known Issues Answer Record is for the Memory Interface Generator (MIG) v2.2 released in ISE 10.1 IP Update 1 (10.1.1), and contains the following information:

- General Information
- Software Requirements
- New Features
- Resolved Issues
- Known Issues

For installation instructions, general CORE Generator known issues, and design tools requirements, see the IP Release Notes Guide at:
http://www.xilinx.com/support/documentation/user_guides/xtp025.pdf

Solution

General Information

MIG is no longer provided as a separate download, but is now incorporated into IP Updates. MIG v2.2 is available through ISE 10.1 IP Update 1 (10.1.1).

For a list of supported memory interfaces and frequency support, see the MIG User Guide:
http://www.xilinx.com/support/documentation/user_guides/ug086.pdf

Software Requirements

- ISE 10.1.1
- Synplify Pro 9.0.1 support
- 32-bit Windows XP
- 32-bit Linux Red Hat Enterprise 4.0
- 64-bit/32-bit Linux Red Hat Enterprise 4.0
- 64-bit XP professional
- 32-bit Vista business
- 64-bit SUSE 10

New Features

- Xilinx ISE 10.1.1 software support.
- Support of Qimonda memory parts for DDR2 SDRAM interfaces for all FPGA families.
- Multiple interface support (up to 8) in Virtex-5 FPGAs for DDR2 SDRAM and QDRII SRAM designs.
- Support to update UCF files from MIG 1.73 or following versions to the current version.
- IDELAYCTRL LOC constraints are provided in the UCF file for Virtex-4 and Virtex-5 designs.

Resolved Issues

- Updated MIG User Guide

CR Number: 458623 - Added more information about multi controller support.
CR Number: 444312 - Added new section "Timing Analysis" to the Memory Implementation Guidelines section. This section provides information on the data valid window, where the spreadsheets are located, and why they should be used.
CR Number: 457475 - Added information on the Write Pipe Stages option for Spartan designs.

- Debug Enable feature allows user to select different tap values for DQS and loop back signals using VIO.
CR Number: 455754
- MIG generates a warning message when unsupported synthesis tool is selected.
CR Number: 458627
- Syn_noprune Synplicity attribute is replaced with syn_preserve to prevent specific registers from being optimized.
CR Number: 466160
- Added more description for the "DCI Cascading" option in the GUI.
CR Number: 467112
- MIG supports the option "Recustomize Under Current Project Settings" in CORE Generator.
CR Number: 458489
- MIG now generates UCF files for all selected "Compatible FPGA Devices" in a 'compatible_ucf' folder.
CR Number: 458436
- "Read UCF File" option now defaults to the previously loaded UCF path.
CR Number: 456703
- The default memory part for DDR2/DDR SDRAM is to set x8 rather than x4 in the GUI.
CR Number: 466295
- License agreement page has been moved in the GUI. It is now located after the summary page.
CR Number: 467023
- "Close" button on last page of MIG GUI is replaced with "Finish."
CR Number: 458493
- MIG properly allocates the masterbank_sel pin used for DCI Cascade in a user selected bank. Previously this pin was allocated to a non-selected bank in specific configurations.
CR Number: 458600
- Added support the Virtex-5 SX240T device.
CR Number: 466136
- Resolved errors in the DDR2 SDRAM design for Virtex-5 in the usr_rd.v/.vhd files for a 144-bit ECC design which caused multi-source errors during synthesis. See (Xilinx Answer 30702) for further information.
- Provided comments in the Virtex-5 DDR2 SDRAM UCF for the MAXDELAY constraints on the DQS gate. These provide guidelines on how and if the constraint can be relaxed.
CR Number: 452234
- Resolved issue with Virtex-5 DDR2 SDRAM stage 4 calibration algorithm which potentially caused data corruption on the first or last word of a sequence of consecutive read bursts. See (Xilinx Answer 30410) for full details.
CR Number: 467222
- Resolved issue with Virtex-5 DDR2 design that cause Pack errors during MAP in regards to LUTNM combinations. See (Xilinx Answer 30129) for further information.
- ChipScope debug port is included for V5 DDR2 ML561 board files.
CR Number: 453749
- Removed the MAX_FANOUT attribute in V5 DDR SDRAM design. This resolved timing errors.
CR Number: 458171
- MIG generates the IDELAYCTRL LOC constraints for Virtex-4 and Virtex-5 designs. Previously, the designs instantiated one IDELAYCTRL and allowed the tools to replicate as needed. This caused problems with multi-controller designs or designs with additional IDELAYCTRLs instantiated.
CR Number: 452345
- Environment variable "XIL_ROUTE_ENABLE_DATA_CAPTURE" is not required to set in batch files for Spartan-3 generation designs.
CR Number: 456399
- In all Spartan-3 generation designs, BUFGMUXes are replaced with BUFGs.
CR Number: 455439
- For all Spartan-3 generation designs, the user can assert a command in the clock cycle following the assertion of the ar_done signal.
CR Number: 467070
- For Spartan-3 generation designs, the default value of the tapfordqs signal is properly set to tap1 in the cal_ctl module. This previously was incorrect for specific top/bottom bank configurations.
CR Number: 468632
- The read timing analysis for Spartan-3 generation designs with top/bottom banks selected includes the correct number of LUTs.
CR Number: 468631
- Memory uncertainties in Read timing analysis are corrected for Spartan-3 generation designs.
CR Number: 468616
- Removed the unused parameters READENABLE, DEEP_MEMORY, DATABITSPERMASK and NO_OF_CS from Virtex-4 DDR2 SDRAM Direct Clocking design parameter file.
CR Number: 458282

Known Issues
The following are known issues for v2.2 of this core. These issues will all be resolved in MIG v2.3.

All Multicontroller Designs
- Verify UCF/Update Design is not supported.
- Simulation test bench is not supported.
- Pin allocation takes more time when more than four controllers are selected in the GUI. Because MIG supports dynamic pin

allocation, MIG reallocates pins to all the controllers each time bank selections are made.

Virtex-5 Multicontroller Designs
- Generating multi-controller designs with DDR2 SDRAM and QDRII using the Core Generator batch mode is not supported. Using this mode with this multi-controller combination will result in generation of incorrect rtl files.
- QDRII/DDR2 multi-controller designs do not include clock and reset signals for both interfaces in the user testbench (user application). Manual modification is required. See (Xilinx Answer 30789) for further information.

MIG Tool
- Qimonda 512 Mb devices have two different versions. Devices released before and after January 9, 2007. MIG supports the devices released after January 9, 2007. If the devices released prior to this date are being used, the "Create Custom Part" option must be used as the tRAS (ACTIVE-to-PRECHARGE command time) and tRC (ACTIVE-to-ACTIVE (same bank) command time) parameter values are different between the two products.
- The MT18HTF25672PDY-53E is a x8 device and the MT18HTF25672Y-53E is a x4 device. MIG denotes the PDY/Y only as XXX making it unclear whether the part is a x4 or x8. MIG will specify the exact part and not use XXX in v2.3.
- If float values are entered when creating a custom Qimonda part for tRAS, tRP and tWR, MIG outputs incorrect timing parameter values in the memory model. MIG writes out these parameters with an extra decimal point followed by two zeros. For example, for tRP value of 11.25, tool outputs in model as 11.25.00. This causes simulation failures.

Virtex-5 QDRII
- Updating a MIG v1.73 or earlier design requires manual modification to the updated UCF/rtl files to account for the CQ_n (CQ#) pins. See (Xilinx Answer 30782) for further information.
- Using the Update UCF feature for a QDRII x36 design requires manual modifications. See (Xilinx Answer 30785) for further information.
- Verify UCF does not work properly when Master Banks are used for DCI_CASCASE. An error message should be generated when the "masterbank_sel_pin" is not allocated to the master bank.
- Pin allocation for a x18 36-bit design is incorrect when the Reserve Pins option is used. See (Xilinx Answer 30786) for further information.
- When DCI cascading is selected, it is required to have at least one input pin in the master bank. MIG allocates a dummy input pin in the master bank to meet this requirement. When the master bank is selected in an Address or Write Data bank, MIG properly allocates this additional pin as it is required. However, if the master bank is selected in the Data Read bank, this is not needed. However, MIG still allocates the additional pin.
- DCI_CONFIG setting is incorrect in UCF when Data Read banks are in two different columns for x18 36-bit designs. See (Xilinx Answer 30788) for further information.

Virtex-4 DDR2
- Direct Clocking Deep Design - ODT is not supported for dual rank parts.
- Direct Clocking Design - When a dual rank part is selected, the GUI allows depth selection of 1, 2, or 4. A depth of 1 should not be selectable since the device is dual-rank.
- The Serdes Design Preset Configurations for the following devices do not meet timing:
-- xc4vfx60-ff1152
-- xc4vlx80-ff1148,
-- xc4vfx140-ff1517
-- xc4vlx160-ff1148

Virtex-4 DDR
- Calibration is completed on a per bank basis in the current design. A bank may have multiple DQS and associated DQ bits, but the calibration is performed on only one DQS. The resultant delays are applied to all the DQ bits of other DQS. This scheme may not work reliably at all frequencies, in particular lower frequencies. To work around this issue, the calibration block should be replicated for each DQS grouping.

Spartan-3 Generation DDR/DDR2
- The generated UCF contains the following unnecessary constraint which can be removed from the UCF:
NET "*memcore/top_00/data_path0/dqs_delayed_col*" TNM_NET = "dqs_clk";
NET "*memcore/top_00/data_path0/data_read0/gen_strobe*strobe/wclk*" TNM_NET = "fifo_clk"; TIMESPEC "TS_DQS_CLK" = FROM "dqs_clk" TO "fifo_clk" 5 ns DATAPATHONLY
- DDR design does not support burst length=2. See (Xilinx Answer 30794) for further information.
- DDR/DDR2 SDRAM design for larger Spartan-3 devices do not meet 133 MHz when top/bottom banks are selected. See (Xilinx Answer 30679) for further information.
- Issue with write/read pointer algorithm might cause FIFO data to be lost. See (Xilinx Answer 30796) for further information.
- When the data mask is disabled through the GUI, the OBUF that drives the mask signal should be removed by MIG. This however is not happening. In the top level instantiation, the dm signals are left open. Because of the OBUF instantiation, the tools allocate pins to mask signals. This might create PAR errors if there is an I/O standard mismatch. The OBUF instantiation needs to be removed in this case.
- Spartan-3A and Spartan-3AN devices are pin compatible; however, this is currently not enabled in MIG.