

## Answers Database

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### Virtex-4 Aurora v2.7 - Intermittent startup failure

Answer Record: 25470  
 Family: Hardware  
 Product Line: MGT  
 Part: HW-Aurora  
 Version:  
 Last Modified: 08/27/07 01:33:51  
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#### Problem Description:

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Keywords: core, CORE Generator, ISE, installation, IP, update, GT, GT11, MGT, Aurora, Verilog, VHDL

The default Aurora initialization state machine (LANE\_INIT\_SM) contains an asynchronous input that can cause the state machine to go into an unknown state. This Answer Record describes the fix for this issue.

In addition to this Answer Record, Virtex-4 Aurora users should also look at [\(Xilinx Answer 25469\)](#). Version 2.8 of the Virtex-4 Aurora Core will contain the fix listed in Answer Record 25469.

#### Solution 1:

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The LANE\_INIT\_SM module is a one-hot state machine that controls lane initialization. This state machine is clocked by the Aurora Core's system clock called "USER\_CLK". The state machine is initialized by two signals called "TXPMA\_READY" and "RXPMA\_READY". TXPMA\_READY and RXPMA\_READY are generated by the GT11\_INIT module which is synchronous to a different clock called "DCLK".

This setup results in a race condition where the LANE\_INIT\_SM can go into a state where all one-hot state registers are '0'. The State Machine code does not check for this illegal condition and can lock up such that the core will not self-recover. To fix the issue, the asynchronous inputs (TXPMA\_READY and RXPMA\_READY) must be registered by USER\_CLK before entering the State Machine.

A quick VHDL example:

```
process (USER_CLK)
begin
if (USER_CLK 'event and USER_CLK = '1') then
txpma_ready_r <= TXPMA_READY;
rxpma_ready_r <= RXPMA_READY;
end if;
end process;
```

...

```
if ((RESET or HARD_ERROR_RESET or not txpma_ready_r or not rxpma_ready_r) = '1') then
```

...

This bug affects Virtex-4 Aurora versions 2.5, 2.6, and 2.7. The issue will be fixed in Aurora 2.8, which is scheduled to release in 9.2 IP2. Virtex-II Pro and Virtex-5 GTP Aurora cores are not affected by this issue.

#### Solution 2:

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See also:

[\(Xilinx Answer 25469\)](#) - Virtex-4 RocketIO Wizard v 1.4 - GT11\_INIT State Machine startup failure  
[\(Xilinx Answer 29208\)](#) - Virtex-4 Aurora ? Special reset consideration for Virtex-4 Aurora designs

#### Solution 3:

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A patched version of Aurora v2.7 can be downloaded below. This patch is called Aurora v2.7.1 and contains the fix mentioned in this Answer Record as well as the fix mentioned in [\(Xilinx Answer 25469\)](#).

To install this patch:

1. Make sure you have the correct ISE version. This patch is intended for ISE 9.1.03, 9.2.01 and 9.2.02.
2. Download the file here:

[ftp://ftp.xilinx.com/pub/utilities/fpga/v4aurora\\_2\\_7\\_1\\_installer.zip](ftp://ftp.xilinx.com/pub/utilities/fpga/v4aurora_2_7_1_installer.zip)

3. Copy the file to the "%XILINX%" directory.

4. Unzip the file (click Yes if asked to overwrite the files).

You can verify the patch by looking at the header in the generated HDL files. The second line of the header should read:

Project: Aurora Module Generator version 2.7.1