AR #31402 - MIG v2.3 - Release Notes and Known Issues for ISE 10.1 IP Update 3 (IP_10.1.3)

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Description

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This Release Notes and Known Issues Answer Record is for the Memory Interface Generator (MIG) v2.3 released in ISE 10.1 IP Update 3 and contains the following information:

- General Information
- Software Requirements
- New Features
- Resolved Issues
- Known Issues

For installation instructions, general CORE Generator known issues, and design tools requirements, see the IP Release Notes Guide at:
http://www.xilinx.com/support/documentation/user_guides/xtp025.pdf

Solution

General Information

MIG is no longer provided as a separate download, but it is now incorporated into IP Updates. MIG v2.3 is available through ISE 10.1 IP Update 3 (10.1.3).

For a list of supported memory interfaces and frequency support, see the MIG User Guide:
http://www.xilinx.com/support/documentation/user_guides/ug086.pdf

Software Requirements

- ISE 10.1.3
- Synplify Pro 9.2.4 support
- 32-bit Windows XP
- 32-bit Linux Red Hat Enterprise 4.0
- 64-bit/32-bit Linux Red Hat Enterprise 4.0
- 64-bit XP professional
- 32-bit Vista business
- 64-bit SUSE 10

New Features

- Support for Dual Rank Virtex-5 DDR2 SDRAM design.
- Virtex-4 DDR SDRAM design updated to use per-bit deskew calibration technique.
- PPC440 compatible pin-out support for Virtex-5 DDR2 SDRAM.
- Support of Single-Ended vs Differential system clock selection in MIG tool.
- Support of high-performance mode for IODELAY in MIG tool.
- FPGA floor plan changed to an architectural view from package view in bank selection screen in MIG tool.
- Separate options for Verify UCF and Update Design in MIG tool.
- Support for Verify UCF and Update Design for Spartan-3 Generation in MIG tool.
- Support of Virtex-5 multiple interface simulation test bench.
- Support of two bytes per bank for data signals for Virtex-5 DDR2 SDRAM design.

- Support of DDRII SRAM for Virtex-5.
- TXT parts support for Virtex-5 designs.
- Support for Debug Port for Virtex-4 DDR2 SDRAM Direct Clocking design.

Resolved Issues

DDR2 SDRAM Virtex-5
- Tri-state control polarity for DQ during reset corrected.
-- CR 475131
- The parameter IDELAYCTRL_NUM is moved to the top level.
-- CR 469681

QDRII SRAM Virtex-5
- Half cycle path on compare_error signal changed to full clock cycle path.
-- CR 476583
- Unused signal clk180 removed from input ports when DCM Option is disabled.
-- CR 474498
- Corrected the X_CORE_INFO data.
-- CR 474278
- Calibration logic does not consider input data from user interface.
-- CR 471643
- User does not need to drive the active byte write signals during calibration.
-- CR 469050
- The parameter IDELAYCTRL_NUM is moved to the top level.
-- CR 469681

DDR2 SDRAM Virtex-4
- Enabled deep design support for MT8HTF6464AY-53E and MT8HTF6464AY-667 parts for Direct Clocking design.
-- CR 475264
- Instance name of IDELAY_CTRL in mem_interface_top corrected for Direct Clocking, no DCM, VHDL design.
-- CR 474962
- Support added for Debug Port.
-- CR 472813
- Timing is met for all SERDES design preset configurations.
-- CR 471731
- ACTIVE command is not supported from user interface (Direct Clocking and SERDES designs).
-- CR 445050

DDR SDRAM Virtex-4
- Implemented per bit calibration algorithm.
-- CR 471733
- ACTIVE command is not supported from user interface.
-- CR 445050

DDR/DDR2 SDRAM Spartan-3
- Removed the environment variable "set XIL_PAR_ALIGN_USER_RPMS=1" from ise_flow.bat file for all Spartan-3 Generation designs. This environment variable is no longer needed. See (Xilinx Answer 31107) for further information.
-- CR 473718
- Corrected the CLKOUT_PHASE value for Spartan-3A timing analysis.
-- CR 472309
- Corrected the pjcli script for Spartan-3A DSP and Spartan-3E devices.
-- CR 471668
- Pin compatibility works between Spartan-3A and Spartan-3AN.
-- CR 471666
- When data mask is disabled, removed logic that drives the data mask signals for all Spartan-3 Generation designs.
-- CR 471665
- In all Spartan-3 Generations designs, the logic for the read data FIFO read enable generation was modified. See (Xilinx Answer 471470) for further information.
-- CR 471470
- Single burst of burst length 2 is not supported in all Spartan-3 Generation designs.
-- CR 471469
- Removed invalid constraints from UCF file for all Spartan-3 Generation designs.
-- CR 470778
- Resolved issue with larger Spartan-3 devices where the local route delay was greater than 1900 ps for top/bottom banks. See (Xilinx Answer 30679) for further details.
-- CR 469861
- BUFGMUXs replaced with BUFGs in all Spartan-3 Generation designs.
-- CR 455439

Updates to MIG User Guide
-- CR 475354 - Corrected the QDRII SRAM Virtex-5 burst read operation description.
-- CR 475228 - Added more description about the MIG output file names.
-- CR 474085 - Memory implementation guidelines for CK and CK_n signals corrected for Spartan designs.
-- CR 473994 - Added CLKDIV0 description to DDR2 SDRAM Virtex-5.
-- CR 473966 - Detailed description of clock requirements added to the FPGA options of the DCM section of user guide when DCM is enabled and disabled.
-- CR 473965 - New sections on clocking scheme added to all design descriptions.
-- CR 473932 - Added a separate section "Using MIG in Batch Mode".
-- CR 473445 - Added more details on the user design clocks.
-- CR 473215 - Added description on using the pin compatible memory devices without changing the UCF file.
-- CR 472715 - Two new devices XC3S700AFT256 and XC3S1400AFT256 added to the device table list.
-- CR 471644 - Added notes about selecting master bank for QDRII SRAM Virtex-5, x18 part and 36-bit data. User must not select data read bank as master bank when there is only one data read bank allocated in that column.
-- CR 471170 - The order of app_wdf_data and app_mask_data corrected in figure 9-10.
-- CR 471128 - User interface to controller signal description table added for Virtex-5 sections.
-- CR 470417 - Added CLKDIV signal to the top level DDR2 SDRAM Virtex-5 block diagram.
-- CR 469684 - GUI screen shots updated.
-- CR 469107 - Details added to the Update Design and Verify UCF flows.
-- CR 467479 - Added a note about running CORE Generator to generate a MIG design in batch mode with a space in project path.
-- CR 467470 - Updated Verify UCF error messages.
-- CR 455672 - Added clarifying details to the WASSO section.

- MIG Tool
- Resolved issues with Update Design as noted in (Xilinx Answer 31081).
-- CR 474553 - When non-DCI banks are selected for DQ, corrected the RLOC constraints of the slave pins.
-- CR 474552 - Resolved DM pin allocation issue when non-DCI banks are selected for DQ/DQS of DDR and DDR2 SDRAM Virtex-5 designs.
-- CR474083 - Update Design outputs the correct DQS Squelch constraints for DDR2 SDRAM Virtex-5 design when DQS pins are swapped.
-- CR 474081- Update Design outputs correct RLOC_ORIGIN constraints for DDR2 SDRAM Virtex-5 design.
-- CR 474067 - Update Design outputs the IDELAYCTRL LOC constraints based on new pin-out.
-- CR 474356 - Removed the undesired string with special characters from the VHDL top level RTL file of updated design.
-- CR 473856 - Fixed bugs in Update Design Feature.
-- CR 474578 - Update Design works for x4 memory parts of 1.73 input UCF file.
-- CR 474554 - Update Design does not parse the comments in input UCF file.
- Support for Single-Ended and Differential System Clock selection.
-- CR 416890
- Bank floor plan is changed from top view to an architectural view.
-- CR 416850
- Verify UCF now checks the port signal case.
-- CR 475617
- Verify UCF now checks whether the CC_N pin of the DQS tile is allocated to only output signal for DDR SDRAM Virtex-5 design.
-- CR 475616
- Resolved issue with FXT single PPC non-DCI banks for DDR2 SDRAM Virtex-5 data group.
-- CR 475265
- More details added to the Bank Selection screen of MIG GUI.
-- CR 473964
- Design notes are viewed before the generation of design.
-- CR 473963
- Enhanced features of Update Design.
-- CR 473857
- Added the internalmodulename parameter to CORE Generator summary.xml file.
-- CR 473738
- Separated out the Verify UCF and Update Design features in MIG GUI.
-- CR 472747
- Corrected the supported CAS latency to be 2.5 for DDR SDRAM -75 parts and frequency greater than 100 MHz.
-- CR 472059
- Update Design outputs the correct UCF file when 1.73 input UCF file is passed for DDR2 SDRAM Virtex-4 SERDES design.
-- CR 471908
- Batch mode is supported for Virtex-5 multiple interface designs.
-- CR 471885
- Resolved issue with reserved pins in data read bank for QDRII SRAM Virtex-5 with the DCI cascade option. See (Xilinx Answer 30786) for further information.
-- CR 471884
- Verify UCF feature will not consider the error, init_done, and sys_rst signals for verification.
-- CR 471846
- Low power option is supported for Virtex-5 designs.

-- CR 471762
- Removed the enable/disable text for the Data Mask option.
-- CR 471759
- Data mask module is properly instantiated depending on the MIG Data Mask setting for all DDR and DDR2 SDRAM designs.
-- CR 471726
- Removed the black_box files in Virtex-5 designs for Synplify Pro. Black_box files are no longer required. See (Xilinx Answer 30814) for further information.
-- CR 471745
- Simulation test bench file modified for Virtex-5 designs to run VCS simulations. See (Xilinx Answer 30814) for further information.
-- CR 471697
- Verify UCF for QDRII SRAM Virtex-5 reports an error message when the "masterbank_sel_pin" is moved to a non-master bank.
-- CR 471642
- Virtex-4 and Virtex-5 DDR SDRAM designs support the minimum frequency of 77 MHz.
-- CR 471637
- MIG properly enables memory depth of 2 or 4 for dual rank DDR2 SDRAM parts for Virtex-4 Direct Clocking designs.
-- CR 470539
- Removed the async reset primitives in all MIG designs where applicable.
-- CR 470352
- Verify UCF for QDRII SRAM Virtex-5 supports verification of input UCF when 36-bit data is split between two banks.
-- CR 470132
- Resolved issue with Update Design for QDRII Virtex-5 when a UCF for a MIG v1.73/v2.0 x36 device is input. See (Xilinx Answer 30785) for further information.
-- CR 469998
- Resolved issue with Update Design for QDRII Virtex-5 when a UCF for a MIG v1.73 x18 device is input. See (Xilinx Answer 30782) for further information.
-- CR 469997
- Memory device selection shows the full DIMM part numbers as per the data sheet.
-- CR 469786
- Resolved simulation errors on tRAS, tRP and tWR parameters for Qimonda Create Custom Part.
-- CR 469686
- New memory parts created using Create Custom Part option are saved to the CORE Generator project folder.
-- CR 469465
-- CR 448842
- Virtex-5 multi-controller designs support Webtalk attribute "CORE_GENERATION_INFO".
-- CR 469245
- Update UCF is supported for 1.73 and 2.0, x36 memory parts of QDRII SRAM Virtex-5.
-- CR 468852
- Virtex-5 multiple interface designs - When DCI is enabled, DDR2 SDRAM address bank cannot be selected in the QDRII SRAM data read or Master bank.
-- CR 468851
- MIG will not use dummy master bank sel pin when data read bank is selected as Master bank in QDRII SRAM Virtex-5 designs.
-- CR 468850
- Memory density for Unbuffered DIMM MT16HTF25664AX-40E properly displays 2 Gb.
-- CR 468814
- MIG supports 72-bit SODIMM.
-- CR 468565
- Write recovery value in Mode register corrected for DDR2 SDRAM Virtex-5 design.
-- CR 467851
- Blank WASSO values will set to default values.
-- CR 459764
- No need to double-click on create custom part "value" to edit. It works with single click.
-- CR 459759
- When MIG is closed without generating a design, error message is not displayed.
-- CR 459684
- MIG can now also read in UCFs with bus convention format <x>.
-- CR 456704
- Characters are no longer truncated on bank selection page when viewed in Chinese and Korean language.
-- CR 455327
- Special characters do not appear in Memory License Agreement page or Design Notes page.
-- CR 455279
- MIG supports valid FXT pin-out compatible for LX/SX design.
-- CR 452513

Known Issues

(Xilinx Answer 32097) MIG v2.3, Update Design/Verify Design - "ERROR: The same pin was allocated to more than one signal."
(Xilinx Answer 31299) MIG v2.3, Virtex-5 DDR2 SDRAM - Timing parameters are incorrect in simulation and hardware
(Xilinx Answer 31590) MIG v2.3 - Memory parts created using the Create Custom Part feature are not visible in the GUI after relaunching MIG

(Xilinx Answer 31807) MIG v2.3 - Why does MIG crash after uploading my mig.prj and UCF to the "Update Design" tool?
(Xilinx Answer 31802) MIG v2.3 - Virtex-5 DDR2 Multi-Controller: Example_Design and User_Design pinouts do not match
(Xilinx Answer 31797) MIG v2.3 - Virtex-4 DDR/DDR2 Direct Clocking: Extra IDELAYCTRL instance LOC causing WARNING:Place:851
(Xilinx Answer 31772) MIG v2.3 - Known Issues for Verify UCF with Spartan-3 Generation devices
(Xilinx Answer 31580) MIG v2.3 - Virtex-5 QDRII, DDRII, Multi-Controller: Provided active high reset logic does not work properly in simulation
(Xilinx Answer 31588) MIG v2.3 - Virtex-5 DDR SDRAM: Simulation will remain in reset if the value of the parameter RST_ACT_LOW is changed from '1' to '0' in the simulation test bench (sim_tb_top.v/.vhd)
(Xilinx Answer 31578) MIG v2.3 - DDR2 SDRAM: Simulating with Qimonda models causes "Memory Allocation Failure" error
(Xilinx Answer 31579) MIG v2.3 - Virtex-5 QDRII: ERROR:Place:899 - The following IOBs use DCI and have been locked to the I/O bank #
(Xilinx Answer 31606) MIG v2.3, Virtex-5 DDR2 - Are CLK and CLK90 related?
(Xilinx Answer 31734) MIG v2.3 - Spartan-3 Generation DDR2 SDRAM: tRAS and tRFC specifications are violated for certain memory parts
(Xilinx Answer 31801) MIG v2.3 - Spartan-3A Starter Kit: When running the ISE project output by create_ise.bat, Translate fails with ERROR:ConstraintSystem:59
(Xilinx Answer 31591) MIG v2.3 - Spartan-3 Generation DDR/DDR2 SDRAM: Incorrect hierarchy for the fifo_we_clk constraint in the provided user_design UCF
(Xilinx Answer 31771) MIG v2.3 - Virtex-5 DDR2 SDRAM Dual Rank - ERROR: tRFC maximum violation during No Op occur in simulation