AR #24448 - MIG v1.6 - Virtex-4 DDR2 SDRAM controller does not exit initial startup calibration

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Description

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DDR2 SDRAM controller from MIG v1.6 or earlier does not exit initial startup calibration. What could be causing this?

Solution

The MIG-generated UCF for versions 1.6 and earlier for certain configurations of the Virtex-4 DDR2 designs (for both Direct Clocking and SERDES architectures) incorrectly marks false timing paths between the synchronous logic clocked off the system clock and clocked off the divided-down version of the system clock. This can cause synchronization issues between the two clock domains and startup problems with the memory calibration logic.

To fix this problem, comment out the following TIG statements:
TIMESPEC TS_IGNORE1 = FROM clk_50 TO clk_0 TIG;
TIMESPEC TS_IGNORE2 = FROM clk_0 TO clk_50 TIG;
TIMESPEC TS_IGNORE3 = FROM clk_50 TO clk_90 TIG;
TIMESPEC TS_IGNORE4 = FROM clk_refresh TO clk_0 TIG;

The MIG-generated UCF also marks internal reset nets as false paths. This can lead to synchronization issues for state logic coming out of reset, especially if the MIG reset logic is used to reset other parts of the design. Suggested modifications to provide for a synchronous reset are outlined in (Xilinx Answer 23783).

Both of these issues have been resolved in the MIG v1.7 release.