AR #29912 - MIG v2.0 - Calibration failures occur at slower frequencies (under 170 MHz) for the MIG Virtex-4 DDR2 Direct Clocking design

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Description

Keywords: straddle, underrun, overflow

The Virtex-4 DDR2 Direct Clocking design provided with MIG v2.0 might have problems calibrating reliably at slower frequencies (under 170 MHz) for specific corner cases. This issue will be experienced in hardware and can occur on any or all of the DQS groups.

Solution

During calibration, the Direct Clocking algorithm looks for an edge on the DQ bits within a DQS group while incrementing the DQ IDELAY taps. If an edge is not found, the algorithm decrements the IDELAY taps to the center of the window. This will work for faster frequencies, but can cause problems at slower frequencies (under 170 MHz) in select corner cases because the taps get into an overflow condition while searching for the next edge of the DQ valid window.

This issue is resolved in MIG 2.1.