mailavj
Visitor

Posts: 15
Registered: 04-10-2009

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Histogram collection Options

04-14-2009 07:48 AM

Hi

I am working on an image processing project where i have to collect histogram of incoming image.
Per clock i am recieving 4 pixels. I am planning to implement it in one blockram. My image is has got intensities represented over 16 bit. 64 contigous intensites come under one bin. 1024 such bins are there. Since i am recieving 4 pixels at a time, i wont be able to update same memory location twice or more if all incoming pixels come under one bin. Please advice how to proceed.

Thanks
Aravind

Message 1 of 4 (1,464 Views) Reply

gszakacs
Expert Contributor

Posts: 2,533
Registered: 08-14-2007

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Re: Histogram collection Options

04-14-2009 10:59 AM

Histogram requires read/modify/write cycles. You can do this in one clock cycle using both ports of a block RAM. I would not suggest trying to update 4 bins at a time in a single block RAM. Either increase your clock rate to handle one pixel per clock, or if this is too fast for your FPGA, use four block RAMs and combine the bins as a post-processing step at the end of the frame.

Because of the pipelined nature of the block RAM, you need to handle the special case where successive pixels add into the same bin. When this happens, I bypass the RAM and use the output of the adder as the current histogram bin value. Otherwise you will continue to add to an older value of the bin and lose some of the pixels.

What is your pixel clock rate and which FPGA are you using?

Regards,
Gabor

Message 2 of 4 (1,453 Views) Reply

mailavj
Visitor

Posts: 15
Registered: 04-10-2009

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Re: Histogram collection Options

04-14-2009 11:19 AM

Hi Gabor

pixel clock is 250MHz and i am using XC5V SXT device

i cannot increase clock rate.
But if i go for an adder as u explained, i may need a comparison stage before adder to make sure new pixel is not in same bin right?
Thanks for your help

Thanks
Aravind

Message 3 of 4 (1,450 Views) Reply

gszakacs
Expert Contributor

Re: Histogram collection Options

Posts: 2,533
Registered: 08-14-2007

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04-14-2009 01:21 PM

mailavj wrote:
Hi Gabor

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Thanks for your help

Thanks
Aravind

Right. This may be hard to accomplish at 250 MHz. The critical path goes from reading the current bin through an adder (if your histogram uses the same value for all pixels, this is really an incrementer) to setup to write the bin back. If you don't use the output register on the block RAM, you are already starting with a large part of your 4 ns eaten up on the clock to output of the RAM. If you use the BRAM output register, you have an extra pipeline stage and then you need to check if the current bin was updated by either of the previous **two** pixels.

Assuming you can meet the timing, the simplest approach needs only one pipeline stage so the read address on one port of the BRAM comes on the cycle before the write address on the other port. Then you have one clock period to increment the current bin value (if the pixel has changed bins) or the previous adder value (if the pixel is on the same bin as the previous one). You can pipeline the comparison, but you still end up with a multiplexer and an adder in the critical timing path.

If you can't meet timing this way it gets a little more complex because to add another pipeline stage you need to compare the current pixel against the previous two pixels and use the appropriate sum if it matches either or both of the previous pixels.

I have done a similar histogram. In my case I had 10 pixels at a time at 66 MHz. I used 10 block RAMs running at 132 MHz to update on every other clock cycle. This way I could do the histogram using a single port of the RAM. The other port was used to access the histogram and clear it out for the next frame. It would also be possible to go with a single ported RAM in this case and use half as many block RAMs by using each port for a separate pixel.

Regards,
Gabor

Reply

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