

Answers Database

Virtex-4 RocketIO Wizard v 1.4 - GT11_INIT State Machine startup failure

Answer Record: 25469

Family: Hardware

Product Line: MGT

Part: HW-Rocket_IO

Version:

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Problem Description:

Keywords: GT11, MGT, COREGen, CORE Generator, VHDL, Verilog, FSM

The GT11_INIT State Machine that is included in the Virtex-4 RocketIO Wizard example design contains an asynchronous input that can cause the state machine to go into an unknown state. This Answer Record describes the fix for this issue.

Solution 1:

The Virtex-4 RocketIO Wizard contains two modules that control MGT resets. The GT11_INIT_TX and GT11_INIT_RX modules are one-hot encoded state machines that are synchronous to DCLK. Both of these modules look at the MGT PLL lock detect ports and the DCM Lock detect port to move between states.

The MGT PLL lock detect signal (called LOCK) gets registered by DCLK before being sent into the state machine. The problem is that the DCM Lock signal (called USRCLK_STABLE) does not get registered by DCLK before being sent to the state machine.

To fix this issue, register USRCLK_STABLE before it gets ANDed with the lock_r signal.

GT11_INIT_TX Example

```
-----  
-- Synchronize LOCK  
-----  
process(CLK)  
begin  
if(CLK'event and CLK = '1') then  
if (reset_r(0) = '1') then  
lock_r <= '0';  
usrclk_stable_r <= '0';  
else  
lock_r <= LOCK;  
usrclk_stable_r <= USRCLK_STABLE; -- Synchronize DCM Lock  
end if;  
end if;  
end process;  
  
...  
  
init_fsm_wait_lock_check <= lock_r and usrclk_stable_r;
```

GT11_INIT_RX Example

```
-----  
-- Synchronize LOCK  
-----  
process(CLK)  
begin  
if(CLK'event and CLK = '1') then  
if (reset_r(0) = '1') then  
lock_r <= '0';  
usrclk_stable_r <= '0';  
else  
lock_r <= LOCK;
```

```
usrclk_stable_r <= USRCLK_STABLE; -- Synchronize DCM Lock
end if;
end if;
end process;
```

...

```
init_fsm_wait_lock_check <= lock_r and usrclk_stable_r and lockupdate_ready_i;
```

Virtex-4 RocketIO Wizard v1.5 fixes this issue.