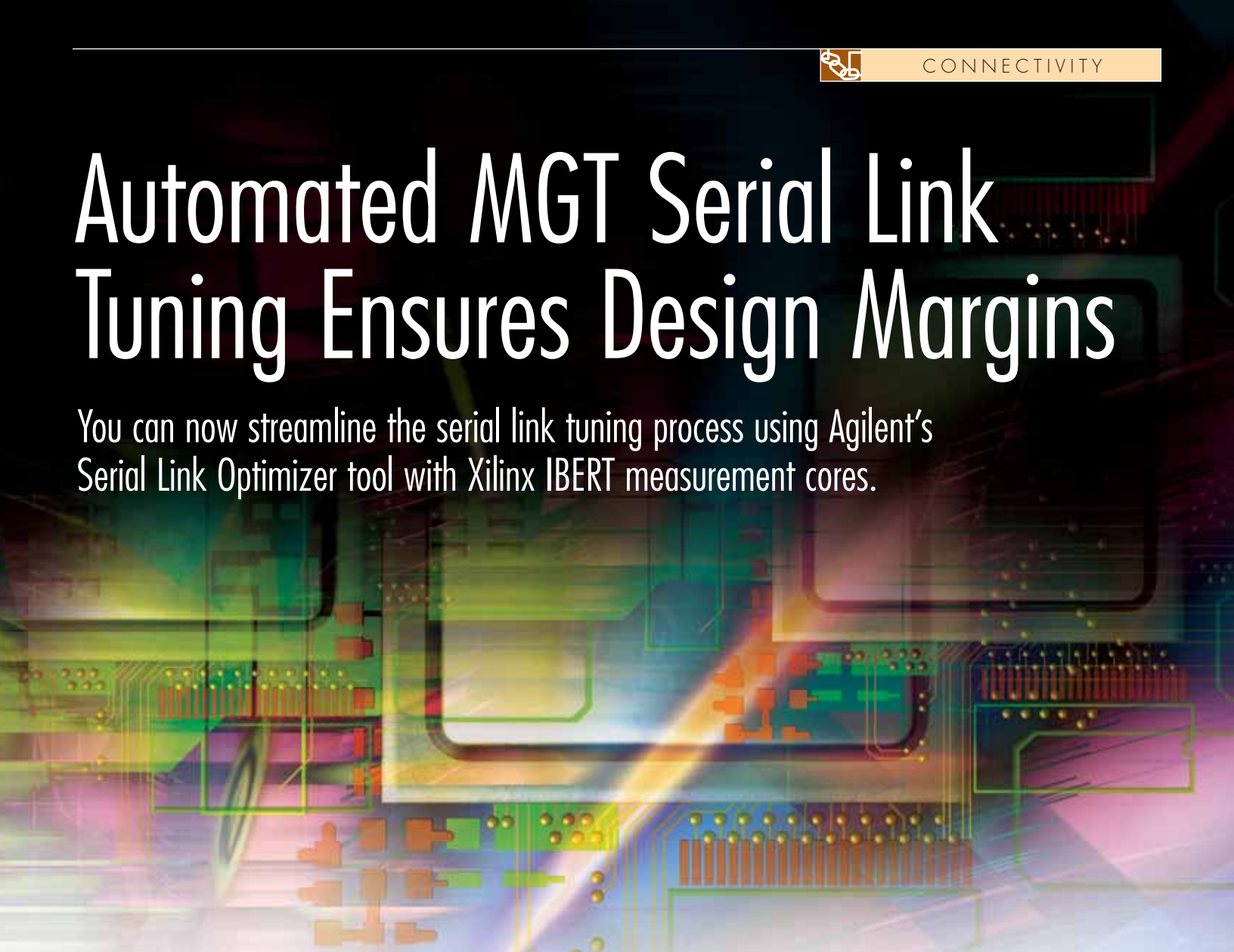
Automated MGT Serial Link Tuning Ensures Design Margins

You can now streamline the serial link tuning process using Agilent's Serial Link Optimizer tool with Xilinx IBERT measurement cores.



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When implementing high-speed serial links in FPGAs, you must consider and address the effects of transmission line signal integrity. Used together, transmitter pre-emphasis and receiver equalization extend the rate at which high-speed serial data can be transferred by opening up the eye diagram, despite physical channel limitations.

An internal bit error ratio tester (IBERT) measurement core from Xilinx can view serial signals at an internal receiver point. Used in conjunction with the Agilent Serial Link Optimizer, you can have both a graphical view of the BER across the unit interval and automatically adjust pre-emphasis and equalization settings to optimize the channel.

In this article, I'll show you how to optimize a Virtex-4 MGT high-speed serial link through this process and discuss the results.

Challenges of Signal Degradation

At 3.125- and 6-Gbps rates and rise times of 130 ps or shorter, it is no wonder that most applications end up with significant signal integrity effects from the physical channel that distort the signal at the receiver input. Distortion can come from multiple reflections caused by impedance discontinuities, but a more fundamental effect – especially in FR4 dielectric PC boards – slows down the edge speeds. Frequency-dependent skin effect causes a "slow tail" to the pulse. To compensate for this, you can apply a time-domain technique called pre-emphasis to the transmit pulse, with significant improvement at the receiver.

Additionally, because the channel is bandwidth-limited, you can apply a frequency-domain technique called equalization at the receiver to compensate for channel frequency roll off. A peaked frequency response yields a more flat response when combined with the channel roll off. The effects of equalization at the receiver input are quite drastic, but this is only visible inside the chip at the actual receiver input (post-equalization).

Measuring Link Performance

It is important to be able to verify the performance of a link and to optimize it through the combined adjustment of transmitter pre-emphasis and receiver equalization. Unfortunately, taking a measurement on the pins of the FPGA where the receiver is located yields a very distorted signal, since you are observing the signal with pre-emphasis applied but without corresponding equalization.

Figure 1 is an example of such a measurement made with an Agilent digital communications analyzer on a 6-Gbps channel implemented with ASIC technology. Notice that the eye diagram actually appears completely closed, even though good signals are present at the receiver input inside the chip.

IBERT Measurement Core

Fortunately, you can observe what is going on at the FPGA's receiver input by using an IBERT measurement core that is part of the Xilinx® ChipScope™ Pro Serial I/O toolkit. The normal FPGA design is temporarily replaced with one that creates stimulus at the transmitter and measures BER at the receiver. These stimulus/response core pairs are placed in the design using a core generation process. Now it is possible to observe BER at the receiver inside the chip. Using that basic measurement capability, you can apply a variety of pre-emphasis and equalization combinations to optimize the channel response.

Basic BERT Measurements

To understand link performance, you must have the ability to measure bit error rate. To do this, a new tool called the Agilent Serial Link Optimizer takes control of IBERT core stimulus and response in the serial link to create such a measurement. A measurement system as shown in Figure 2 allows for this kind of test. Here, two Virtex™-4 FPGAs comprise the link: one implements the transmitter, the other the receiver. Both FPGAs are under JTAG control from the Serial Link Optimizer software, and measurements are taken at the receiver input point inside the FPGA to measure BER.

Some of the selectable measurement attributes include:

- Loopback mode (internal, external, or none)
- Test pattern type
- Dwell time at each point across the unit interval
- Manual injection of errors

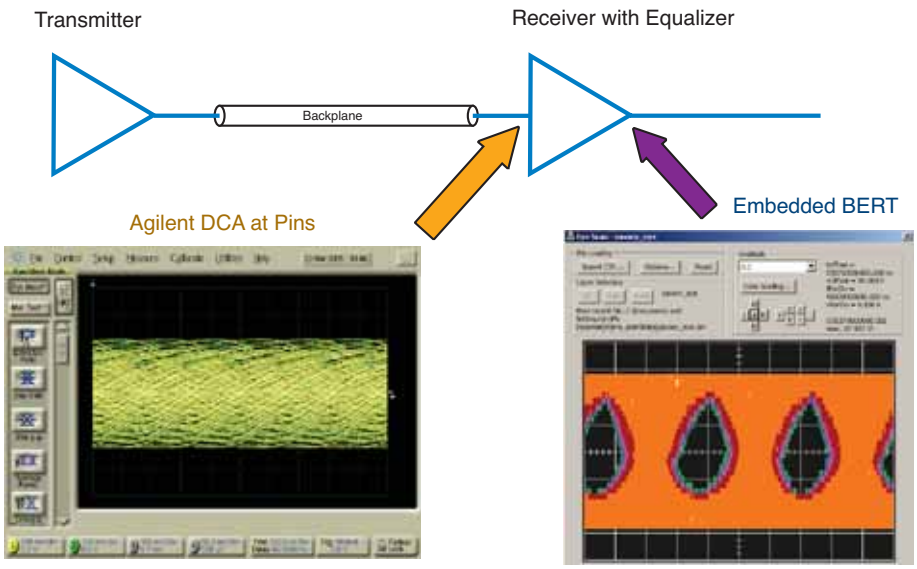

Figure 1 – DCA measurement on FPGA serial I/O pins versus on-chip measurement at the receiver input

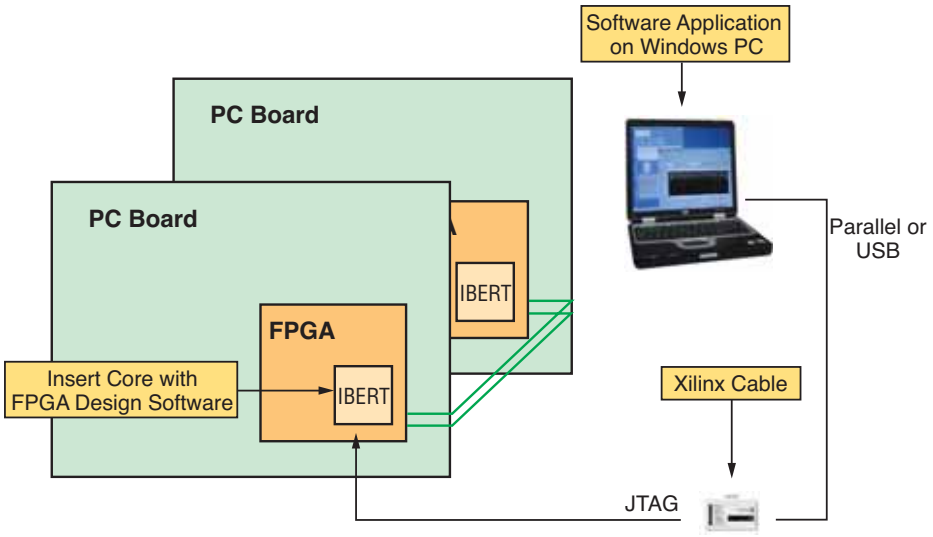

Figure 2 – Serial Link Optimizer block diagram

I obtained a measurement on a serial link that comprises a Xilinx Virtex-4 XC4VFX20 multi-gigabit transceiver (MGT) 113A transmitter on one Xilinx ML405 board, with a connection through a SATA cable over to an MGT 113A receiver in a second Virtex-4 XC4VFX20 FPGA on a second ML405 board. I made a USB JTAG connection to the first FPGA and IBERT core associated with the transmitter, and a parallel JTAG connection to the second IBERT core associated with the receiver. These cores, along with the topology of the ML405 boards, dictate the physical channel.

Steps to set up this measurement include (assuming that the IBERT cores are already created and loaded into the FPGAs):

1. Start tool and configure USB JTAG for TX and verify connection
2. Configure parallel JTAG for RX and verify connection
3. Select MGT 113A transmitter on USB cable

4. Select MGT 113A receiver on parallel cable
5. Select loopback (external)
6. Select test pattern type (PRBS7)
7. Setup TX and RX line rates (reference clock 150 MHz, line rate 6 Gbps)
8. Select BERT tab and press "Run"

I made a measurement on the link with zero errors after 1E+12 bits (~ 3-min measurement). This measurement of BER on the channel occurred at the receiver input internal to the chip and required no external measurement hardware. It forms the basis for additional capability in the Serial Link Optimizer tool.

A Graphical View of BER

The next step toward understanding link performance is to have the ability to graph BER as a function of the unit interval. To do this, the Agilent Serial Link Optimizer takes control of IBERT core stimulus and response in the serial link to create such a graph.

The same measurement system is used as with the basic BER test, but now measurements are taken at 32 discrete steps across the unit interval to show where error-free performance is achieved. The resulting graph is shown in the upper BER plot in Figure 3. The Virtex-4 MGT macro has the ability to adjust the sampling position across these 32 discrete points; the Serial Link Optimizer uses the IBERT core in conjunction with sampling position control to make the measurements. The link performance with default MGT pre-emphasis and equalization settings has zero errors for 0.06 (6%) of the unit interval. This is quite narrow, indicating very little margin. The system could benefit from proper link tuning.

Automated Link Tuning

Let's extend this measurement process yet again by automatically trying combinations of pre-emphasis and equalization settings until the error-free zone in the unit interval is maximized, resulting in the best link performance for speed and margin. The Serial Link Optimizer does just that. Link configuration options include an internal loopback test inside the I/O ring of a single FPGA; transmit and receive from one FPGA; and a transmit/receive pair test between two different FPGAs. It is also possible to inject signals from an external BERT instrument and monitor signals at the receiver inside the FPGA.

In our example, let's use the same serial channel between two Virtex-4 FPGAs with the MGT 113A/B TX/RX pair. On the Serial Link Optimizer interface, select the "Tuning" tab and Run button as shown in Figure 3. The error-free zone with default FPGA settings was 0.06 unit interval. After attempting 141 combinations of pre-emphasis and equalization, the error-free zone increased to 0.281 (28%) unit interval, also shown in Figure 3. This means significantly better margins in the link design at the 6-Gbps speed.

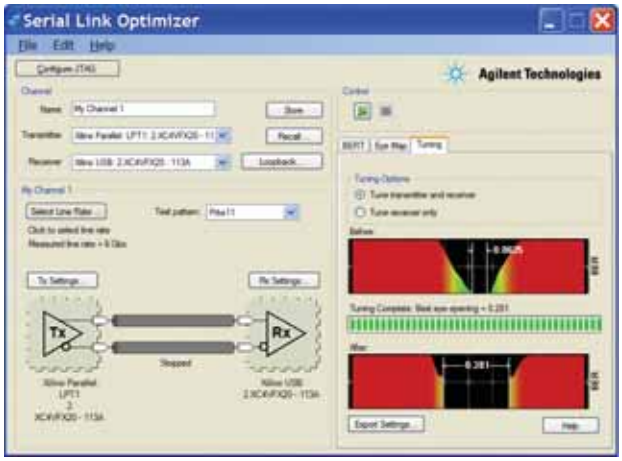

Figure 3 – BER plot before and after automatic adjustment of pre-emphasis and equalization to tune the serial link

Exporting Link Design Constraints

These new pre-emphasis and equalization settings must now be incorporated into a real design that ultimately uses the serial link. Up until this point, I placed a temporary test design into each FPGA to determine the optimal combination of pre-emphasis and equalization. Now that I have determined the optimal combination, the Serial Link Optimizer outputs the corresponding pre-emphasis and equalization settings for the MGTs. The MGT parameters are represented in VHDL, Verilog, and UCF formats and are output when clicking the "Export Setting" button. You can cut and paste these parameters back into the source design, thus incorporating the optimal link settings when the final design is programmed into the FPGAs.

For example, the Verilog settings for the first transceiver are:

```
// Verilog
//— Rocket IO MGT Preemphasis and Equalization —
defparam MGTx.RXAFEEQ = 9'b111;
defparam MGTx.RXSELDACFIX = 5'b1111;
defparam MGTx.RXSELDACTRAN = 5'b1111;
```

Required Components

To take advantage of these measurements, you will need:

1. A PC with Windows XP installed (SP2 or higher)
2. Xilinx programming cable(s), parallel and/or USB
3. Xilinx ChipScope Pro Serial I/O Toolkit (for IBERT core)
4. Agilent E5910A Serial Link Optimizer software

Conclusion

Through automated adjustments of pre-emphasis and equalization, while simultaneously monitoring BER at the receiver input inside the FPGA, it is now possible to automatically optimize an MGT-based serial link.

At 3.125-Gbps rates, such an optimization is helpful to get good margins. But at 6-Gbps rates, optimization becomes crucial to achieve link performance that ensures reliable data transfer. This process can save significant time in reaching your desired design margins and can likely achieve better results than what is possible through traditional manual tuning.

For more information, visit *www.agilent.com/find/serial_io* or *www.agilent.com/find/xilinxfpga*.