AR #29911 - MIG v2.1 - Release Notes and Known Issues for ISE 10.1 Initial IP Update (IP_10.1.0)

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Description

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This Release Notes and Known Issues Answer Record is for the Memory Interface Generator (MIG) v2.1 released in ISE 10.1 Initial IP Update (IP_10.1.0), and contains the following information:

- General Information
- Software Requirements
- New Features
- Resolved Issues
- Known Issues

For installation instructions, general CORE Generator known issues, and design tools requirements, see the IP Release Notes Guide at:
http://www.xilinx.com/support/documentation/user_guides/xtp025.pdf

Solution 1

General Information

MIG is no longer provided as a separate download, but is now incorporated into IP Updates. MIG v2.1 is available through ISE 10.1 Initial IP Update (IP_10.1.0).

For a list of supported memory interfaces and maximum frequency support, see the MIG User Guide.

Software Requirements

- ISE 10.1.0
- Synplify Pro 8.8.0.4 support
- 32-bit Windows XP
- 32-bit Linux Red Hat Enterprise 4.0
- 64-bit/32-bit Linux Red Hat Enterprise 4.0
- 64-bit XP professional
- 32-bit Vista business
- 64-bit SUSE 10

New Features

General New Features and Changes

- Xilinx ISE 10.1.0 software support
- 64-bit/32-bit Linux Red Hat Enterprise 4.0 support
- 64-bit XP professional support
- 32-bit Vista business support
- 64-bit SUSE 10 support

MIG Tool New Features and Changes

- Implemented real time pin allocation in GUI. As banks are selected, the GUI displays the total number of required pins along with the

number of allocated pins for each grouping of signals (Address, Data, System Control, System Clock).
- Implemented priority bank selection. Allocates the pins starting from exclusive Data banks first and then Data banks with the combination of other groups. This Pin Allocation Priority is applicable for only data group signals in Virtex-4 and Virtex-5.
- Simulation test bench support for Custom Memory Parts.
- Attributes "X_CORE_INFO" and "CORE_GENERATION_INFO" support for all designs.
- Uncommon Banks are greyed out in bank selection page when user selects compatible FPGA's, allowing only the common banks for pin allocation.
- "Reserve Pin" banks are changed from list view to hierarchical view.
- "Debug Signals" support.

Virtex-5 New Features and Changes

DDR2 SDRAM
- Added GUI option to select if mask signals are included in the MIG output.
- 2 Gb device support.
- Support to update a MIG v1.72 and MIG v1.73 UCF to a MIG v2.0 and following versions.

DDR SDRAM
- Added GUI option to select if mask signals are included in the MIG output.

QDRII SRAM
- Updated low frequency limit in GUI according to latest memory specs.
- Burst length 2 support.
- x18 device support at 300 MHz.
- Implemented the "DCI Cascade" and "Master Bank" selection option.

Virtex-4 New Features and Changes

DDR2 SDRAM
- Linear addressing support from user interface.
- Added GUI option to select if mask signals are included in the MIG output.
- 2 Gb device support.
- Direct Clocking:
-- CAS latency of 5 support for Direct Clocking design.
-- Calibration algorithm modified to fix issues with low frequency designs.

DDR SDRAM
- Added GUI option to select if mask signals are included in the MIG output.
- Linear addressing support from user interface.

QDRII SRAM
- Updated low frequency limit in GUI according to latest memory specifications.

DDRII SRAM
- Implementation of common Address FIFO for both write and read operations.
- Updated low frequency limit in GUI according to latest memory specifications.

Spartan-3, Spartan-3E, Spartan-3A New Features and Changes

- 166 MHz frequency support for all possible data widths for Spartan-3A, Spartan-3A DSP and Spartan-3E families.
- Linear addressing support from user interface.
- Support for Spartan-3A/-3A DSP DDR2 SDRAM 200 MHz Design.

DDR2 SDRAM
- Added GUI option to select if mask signals are included in the MIG output.
- 2 Gb device support.

DDR SDRAM
- Added GUI option to select if mask signals are included in the MIG output.

Resolved Issues

- Updated Virtex-5 DDR SDRAM support table to include all RDIMMS, UDIMMs, and SODIMMs.
CR Number: 450377
- Updated the output folders and files created from MIG in component name folder.
CR Number: 450378
- Changed references to "Timing Verified Designs" to "Preset Configurations."
CR Number: 450379
- Added SODIMM support for Spartan-3 designs.

CR Number: 452233
- Added maximum and minimum frequency information per FPGA speed grade.
CR Number: 446216
- Added more information on the User Interface.
CR Number: 446218
- Added a detailed description on the user interface for Virtex-4 and Virtex-5 designs.
CR Number: 442014
- Provided information on the recommended build options (Synthesis, Translate, MAP, PAR, TRACE, BITGEN).
CR Number: 429070
- Added a note about Read Data FIFO full condition for RLDRAMII Virtex-4 design.
CR Number: 448076
- Added information on the debug port from Answer Record 24935 for the Virtex-5 DDR2 design.
CR Number: 452432
- Added Answer Record 24935, Spartan-3/-3E/-3A memory implementation guidelines for DDR/DDR2 SDRAM interfaces.
CR Number: 452431
- Added Answer Record 22277, how to change the refresh rate for controllers.
CR Number: 452430
- Added Answer Record 24146, the correlation between the Address and Data FIFOs of Virtex-4 DDR1/DDR2 SDRAM user interface.
CR Number: 452428
- Added information regarding the UCF MAXDELAY constraints for Spartan designs.
CR Number: 449918
- Added information regarding changing the UCF for DDR2_V5 designs from Answer Record 29313.
CR Number: 453839
- Added DIMM support table for Spartan designs.
CR Number: 454614
- Removed all unused parameters from the "Create Custom Part" option.
CR Number: 449349
- The MIG "Create Custom Part" feature now allows user to change parameters to desired value according to JEDEC specifications.
CR Number: 448928
- Added MIG version number to the all file headers.
CR Number: 448183
- Updated MIG output to include the latest memory models for DDR SDRAM, DDR2 SDRAM, and RLDRAMII memories.
CR Number: 450381
- Removed the main.v/.vhd source file from the user_design MIG output. This file is only used in the example_design MIG output.
CR Number: 452861
- Removed the mask signals from the port listing for all designs when devices are selected that do not include mask signals.
CR Number: 450333
- The Virtex-5 DDR2 SDRAM controller correctly issues an ACTIVE command to the previous row after completing an AUTO REFRESH. See (Xilinx Answer 29783) for further information.
CR Number: 453809
- The Virtex-5 DDR2 SDRAM design with ECC enabled for a 144-bit design no longer has a data mask issue. See (Xilinx Answer 29478) for further information.
CR Number: 449168
- Resolved fatal out-of-bounds index errors that previously occurred when running a Virtex-5 DDR2 SDRAM VHDL simulation. See (Xilinx Answer 29478) for further information.
CR Number: 449166
- The Virtex-5 DDR SDRAM VHDL "user_design" no longer includes syntax errors which previously caused simulation to fail.
CR Number: 450374
- The Virtex-5 DDR2 SDRAM user_design successfully passes MAP. Resolved a problem with the multi-cycled path constraints within the provided UCF.
CR Number: 455991
- The Virtex-5 DDR2 SDRAM design includes multi-cycle constraints that cover all possible paths. Previously, designs running at slower frequencies with CL=3 and AL=0 had paths from flip-flops to BRAM that the multi-cycle constraints did not include causing set-up violations.
CR Number: 455991
- The Virtex-5 DDR1 SDRAM design resolved an issue where an incorrect adjustment of DQ IDELAY taps occurred causing read data to be corrupted after calibration. See (Xilinx Answer 29903) for further information.
- Modified the Spartan-3 generation MAXDELAY constraints. Previously common MAXDELAY constraints were provided. In some cases, these over constrained the paths. MAXDELAYs are now provided based on the FPGA selected.
CR Number: 449979
- Included a parameter for all Spartan-3 generation designs to properly select the number of taps to delay the DQS depending on the FPGA selected. This ensures a larger local clock route delay for larger devices with top/bottom banks selected.
CR Number: 449062
- Brought clk_tb to top level port in the Spartan-3 generation DDR SDRAM VHDL, registered DIMM, user_design.
CR Number: 450376
- Allocated the rst_dqs_div signal at the center of the data bank for top/bottom bank selection for all Spartan-3 generation designs.
CR Number: 450334
- The MIG design will successfully pass implementation with the default settings for the XC3S400-PQ208 device.
CR Number: 450335

- Resolved twr violations in simulation for the Spartan-3 generation DDR SDRAM design. This previously occurred for Burst length of 8 designs running at 166 MHz.
CR Number: 450373
- DDR and DDR2 SDRAM Preset Configuration will successfully pass implementation for the XC3S50-CP132 device.
CR Number: 450338
- Updated XST synthesis attributes for all Spartan-3 generation designs.
CR Number: 449757
- Removed all unused parameters from DDR2 SDRAM designs for both Virtex-4 and Spartan-3 generation families.
CR Number: 443545
- Proper design generation for Virtex-4 DDR2 SDRAM ECC design for a 40-bit interface.
CR Number: 453618
- DDR SDRAM Preset Configuration will successfully pass implementation for the XC4V140-FF1517 device.
CR Number: 450337
- The correct number of address pins required is now displayed for the RLDRAMII design when multiplexed addressing is selected.
CR Number: 450336
- RLDRAMII design frequency is limited based on the selected Mode Register settings.
CR Number: 449064
- CAS latency 5 is now supported for DDR2 SDRAM Virtex-4 direct clocking design.
CR Number: 444573
- Linear addressing is implemented for DDR SDRAM and DDR2 SDRAM designs for all families. A10 is considered as part of the address.
CR Number: 422014
- MIG generates the top level templates when used in ISE -> Templates -> Coregen - > VHDL or Verilog.
CR Number: 421225
- Updated the comments in the Header file for DDR2 SDRAM, DDR SDRAM and QDR2 Virtex-5 designs.
CR Number: 452722
- Provided an option to include the Mask signals or No Mask signals for DDR2 SDRAM and DDR SDRAM designs for all FPGA families.
CR Number: 448876
- Reserve Pin list banks is updated to hierarchical view.
CR Number: 448056
- DDRII SRAM Virtex-4 design is modified to use single Address FIFO for both read and write commands.
CR Number: 429909
- Implemented the dynamic pin allocation. MIG displays the information, the number of pins allocated and the number of pins required.
CR Number: 429205
- Implemented the priority bank selection. First priority is given to the exclusive Data Bank for pin allocation.
CR Number: 448875
- Provides the Memory Models for Custom Memory Parts.
CR Number: 448077
- WASSO is now applied only on output signals for RDLRAMII and DDRII SRAM designs.
CR Number: 450380
- Default data width for DDR SDRAM MT46V16M16XX-75 is set to 16 bit.
CR Number: 452677
- In 'Reserve Pins' page, 'Selected Pins' is changed to "Available Pins."
CR Number: 455382
- Added a Warning message in compatibility page regarding designs that will use FX PPC controller.
CR Number: 457316
- Added more description to timing spread sheets.
CR Number: 444312
- MIG highlights only the common banks in 'Bank Selection' page when 'Compatible FPGAs' are selected.
CR Number: 451463
- Implemented the 'Reserve Pin Banks' in numerical order.
CR Number: 455381.

Known Issues

The following are known issues for MIG v2.1. All of these issues will be fixed in MIG v2.2.

All MIG Output Designs

- Reset generation logic in the simulation testbench module does not properly set reset polarity according to the RESET_ACTIVE_LOW/RST_ACT_LOW parameter. If this parameter is changed, the reset generation logic must be manually changed in the sim_tb_top module in order to generate the proper polarity of the reset signal.
- WASSO/Pin Count always includes VRP/VRN pins. In the case of DCI, VRP/VRN pins should not be included for WASSO.
- CORE_GENERATION_INFO attribute is not working, if used in only lower level modules without keeping in mem_interface_top module for Verilog designs. This issue exists in both VHDL and Verilog designs.

Virtex-5 Designs

- Verify UCF option is only supported for 1.7 or later releases for DDR2 SDRAM designs.
- The 1440bit ECC DDR2 SDRAM design has a bug in the usr_rd.v/.vhd file for a 144-bit ECC design. This bug causes multi-source errors during synthesis. See (Xilinx Answer 30702) for further information.
- Designs synthesized with Synplify 9.0 may encounter an error similar to the following during MAP:
"ERROR:Pack:2239 - Unable to obey design constraints
(LUTNM=u_mem_if_top_0/u_phy_top_0/u_phy_io_0/u_phy_calib_0/ddr2_dimm_mem_if_t
op_0_lutnm000181) which require the combination of the following function
generator symbols into a single LUT site:
LUT symbol
"u_mem_if_top_0/u_phy_top_0/u_phy_io_0/u_phy_calib_0/count_dq_5_1[0]" (Output
Signal =
u_mem_if_top_0/u_phy_top_0/u_phy_io_0/u_phy_calib_0/count_dq_5_1[0]/O)
LUT symbol
"u_mem_if_top_0/u_phy_top_0/u_phy_io_0/u_phy_calib_0/cal1_state_s1_0_a4_0_a3"
(Output Signal =
u_mem_if_top_0/u_phy_top_0/u_phy_io_0/u_phy_calib_0/cal1_state_642_d)
LUT symbol
"u_mem_if_top_0/u_phy_top_0/u_phy_io_0/u_phy_calib_0/count_dq_5[0]" (Output
Signal = u_mem_if_top_0/u_phy_top_0/u_phy_io_0/u_phy_calib_0/count_dq_5[0]/O)
A LUTNM constraint instance may only be applied to two function generator
symbols. Please correct the design constraints accordingly."
See (Xilinx Answer 30705) for further information.

Virtex-4 Designs

- Virtex-4 RLDRAM2 Design: The COREGen fifo_generator version should be fifo_generator_v4_2 to guarantee a successful run through PAR.

Spartan-3 Family Designs

- The logic associated with PAD2 (top PAD in an IOB tile) on the left side should go to the column0 slices in order for the template router to be used. Some Spartan-3e designs violate this rule which results in higher route delays.
Work Around: Shift the UCF slice constraints manually from column1 to column0. See the MIG User Guide for more information on checking routes delay values.
- For Spartan-3 designs, rst_dqs_div is not allocated at the center of the DQ sets for top/bottom bank designs. As long as the rst_dqs_div signal meets the MAXDELAY constraint in the UCF file, this will not be an issue.
- When top/bottom banks are selected, the logic associated with the top PAD should always go to the column closer to the IO tile. In some cases, this rule is violated, which results in higher route delays.
Work-around: Shift the UCF slice constraints manually from column1 to column0.
- For Spartan-3 designs using top/bottom banks, two pins need to be allocated for data. A third pin can be allocated for address and control signals. This third pin is not properly being allocated, which reduces the pin efficiency.
- Timing reports will incorrectly show 1/2 clock cycle paths rather than 3/4 clock cycle paths on the BUFGMUX routes. This will result in false timing errors and is an issue with the 10.1.0 timing tools.
Work-around: Replace the BUFGMUX instantiations with BUFG instantiations in the infrastructure module.
- Pin compatibility between Spartan-3A and Spartan-3AN is not supported.
Work-around: Use the UCF file of the similar Spartan-3A device.

Solution 2

General Information

MIG is no longer provided as a separate download, but is now incorporated into IP Updates. MIG v2.1 is available through ISE 10.1 Initial IP Update (IP_10.1.0).

For a list of supported memory interfaces and maximum frequency support, see the MIG User Guide.

Software Requirements

- ISE 10.1.0
- Synplify Pro 8.8.0.4 support
- 32-bit Windows XP
- 32-bit Linux Red Hat Enterprise 4.0
- 64-bit/32-bit Linux Red Hat Enterprise 4.0
- 64-bit XP professional
- 32-bit Vista business
- 64-bit SUSE 10

New Features

General New Features and Changes

- Xilinx ISE 10.1.0 software support
- 64-bit/32-bit Linux Red Hat Enterprise 4.0 support
- 64-bit XP professional support
- 32-bit Vista business support
- 64-bit SUSE 10 support

MIG Tool New Features and Changes

- Implemented real time pin allocation in GUI. As banks are selected, the GUI displays the total number of required pins along with the number of allocated pins for each grouping of signals (Address, Data, System Control, System Clock).
- Implemented priority bank selection. Allocates the pins starting from exclusive Data banks first and then Data banks with the combination of other groups. This Pin Allocation Priority is applicable for only data group signals in Virtex-4 and Virtex-5.
- Simulation test bench support for Custom Memory Parts.
- Attributes "X_CORE_INFO" and "CORE_GENERATION_INFO" support for all designs.
- Uncommon Banks are grayed out in bank selection page when user selects compatible FPGA's, allowing only the common banks for pin allocation.
- "Reserve Pin" banks are changed from list view to hierarchical view.
- "Debug Signals" support.

Virtex-5 New Features and Changes

DDR2 SDRAM
- Added GUI option to select if mask signals are included in the MIG output.
- 2 Gb device support.
- Support to update a MIG v1.72 and MIG v1.73 UCF to a MIG v2.0 and following versions.

DDR SDRAM
- Added GUI option to select if mask signals are included in the MIG output.

QDRII SRAM
- Updated low frequency limit in GUI according to latest memory specs.
- Burst length 2 support.
- x18 device support at 300 MHz.
- Implemented the "DCI Cascade" and "Master Bank" selection option.

Virtex-4 New Features and Changes

DDR2 SDRAM
- Linear addressing support from user interface.
- Added GUI option to select if mask signals are included in the MIG output.
- 2 Gb device support.
- Direct Clocking:
-- CAS latency of 5 support for Direct Clocking design.
-- Calibration algorithm modified to fix issues with low frequency designs.

DDR SDRAM
- Added GUI option to select if mask signals are included in the MIG output.
- Linear addressing support from user interface.

QDRII SRAM
- Updated low frequency limit in GUI according to latest memory specs.

DDRII SRAM
- Implementation of common Address FIFO for both write and read operations.
- Updated low frequency limit in GUI according to latest memory specs.

Spartan-3, Spartan-3E, Spartan-3A New Features and Changes

- 166 MHz frequency support for all possible data widths for Spartan-3A, Spartan-3A DSP and Spartan-3E families.
- Linear addressing support from user interface.
- Support for Spartan-3A/-3A DSP DDR2 SDRAM 200 Mhz Design.

DDR2 SDRAM
- Added GUI option to select if mask signals are included in the MIG output.
- 2 Gb device support.

DDR SDRAM

- Added GUI option to select if mask signals are included in the MIG output.

Resolved Issues
- Updated Virtex-5 DDR SDRAM support table to include all RDIMMS, UDIMMs, and SODIMMs.
CR Number: 450377
- Updated the output folders and files created from MIG in component name folder.
CR Number: 450378
- Changed references to "Timing Verified Designs" to "Preset Configurations".
CR Number: 450379
- Added SODIMM support for Spartan-3 designs.
CR Number: 452233
- Added maximum and minimum frequency information per FPGA speed grade.
CR Number: 446216
- Added more information on the User Interface.
CR Number: 446218
- Added a detailed description on the user interface for Virtex-4 and Virtex-5 designs.
CR Number: 442014
- Provided information on the recommended build options (Synthesis, Translate, MAP, PAR, TRACE, BITGEN).
CR Number: 429070
- Added a note about Read Data FIFO full condition for RLDRAMII Virtex-4 design.
CR Number: 448076
- Added information on the debug port from Answer Record 24935 for the Virtex-5 DDR2 design.
CR Number: 452432
- Added Answer Record 24935, Spartan-3/-3E/-3A memory implementation guidelines for DDR/DDR2 SDRAM interfaces.
CR Number: 452431
- Added Answer Record 22277, how to change the refresh rate for controllers.
CR Number: 452430
- Added Answer Record 24146, the correlation between the Address and Data FIFOs of Virtex-4 DDR1/DDR2 SDRAM user interface.
CR Number: 452428
- Added information regarding the UCF MAXDELAY constraints for Spartan designs.
CR Number: 449918
- Added information regarding changing the UCF for DDR2_V5 designs from Answer Record 29313.
CR Number: 453839
- Added DIMM support table for Spartan designs.
CR Number: 454614
- Removed all unused parameters from the "Create Custom Part" option.
CR Number: 449349
- The MIG "Create Custom Part" feature now allows user to change parameters to desired value according to JEDEC specs.
CR Number: 448928
- Added MIG version number to the all file headers.
CR Number: 448183
- Updated MIG output to include the latest memory models for DDR SDRAM, DDR2 SDRAM, and RLDRAMII memories.
CR Number: 450381
- Removed the main.v/.vhd source file from the user_design MIG output. This file is only used in the example_design MIG output.
CR Number: 452861
- Removed the mask signals from the port listing for all designs when devices are selected that do not include mask signals.
CR Number: 450333
- The Virtex-5 DDR2 SDRAM controller correctly issues an ACTIVE command to the previous row after completing an AUTO REFRESH. See (Xilinx Answer 29783) for further information.
CR Number: 453809
- The Virtex-5 DDR2 SDRAM design with ECC enabled for a 144-bit design no longer has a data mask issue. See (Xilinx Answer 29478) for further information.
CR Number: 449168
- Resolved fatal out-of-bounds index errors that previously occurred when running a Virtex-5 DDR2 SDRAM VHDL simulation. See (Xilinx Answer 29478) for further information.
CR Number: 449166
- The Virtex-5 DDR SDRAM VHDL "user_design" no longer includes syntax errors which previously caused simulation to fail.
CR Number: 450374
- The Virtex-5 DDR2 SDRAM user_design successfully passes MAP. Resolved a problem with the multi-cycled path constraints within the provided UCF.
CR Number: 455991
- The Virtex-5 DDR2 SDRAM design includes multi-cycle constraints that cover all possible paths. Previously, designs running at slower frequencies with CL=3 and AL=0 had paths from flip-flops to BRAM that the multi-cycle constraints did not include causing set-up violations.
CR Number: 455991
- The Virtex-5 DDR1 SDRAM design resolved an issue where an incorrect adjustment of DQ IDELAY taps occurred causing read data to be corrupted after calibration. See (Xilinx Answer 29903) for further information.
- Modified the Spartan-3 generation MAXDELAY constraints. Previously common MAXDELAY constraints were provided. In some cases, these over constrained the paths. MAXDELAYs are now provided based on the FPGA selected.

CR Number: 449979
- Included a parameter for all Spartan-3 generation designs to properly select the number of taps to delay the DQS depending on the FPGA selected. This ensures a larger local clock route delay for larger devices with top/bottom banks selected.
CR Number: 449062
- Brought clk_tb to top level port in the Spartan-3 generation DDR SDRAM VHDL, registered DIMM, user_design.
CR Number: 450376
- Allocated the rst_dqs_div signal at the center of the data bank for top/bottom bank selection for all Spartan-3 generation designs.
CR Number: 450334
- The MIG design will successfully pass implementation with the default settings for the XC3S400-PQ208 device.
CR Number: 450335
- Resolved twr violations in simulation for the Spartan-3 generation DDR SDRAM design. This previously occurred for Burst length of 8 designs running at 166 MHz.
CR Number: 450373
- DDR and DDR2 SDRAM Preset Configuration will successfully pass implementation for the XC3S50-CP132 device.
CR Number: 450338
- Updated XST synthesis attributes for all Spartan-3 generation designs.
CR Number: 449757
- Removed all unused parameters from DDR2 SDRAM designs for both Virtex-4 and Spartan-3 generation families.
CR Number: 443545
- Proper design generation for Virtex-4 DDR2 SDRAM ECC design for a 40-bit interface.
CR Number: 453618
- DDR SDRAM Preset Configuration will successfully pass implementation for the XC4V140-FF1517 device.
CR Number: 450337
- The correct number of address pins required is now displayed for the RLDRAMII design when multiplexed addressing is selected.
CR Number: 450336
- RLDRAMII design frequency is limited based on the selected Mode Register settings.
CR Number: 449064
- CAS latency 5 is now supported for DDR2 SDRAM Virtex-4 direct clocking design.
CR Number: 444573
- Linear addressing is implemented for DDR SDRAM and DDR2 SDRAM designs for all families. A10 is considered as part of the address.
CR Number: 422014
- MIG generates the top level templates when used in ISE -> Templates -> Coregen - > VHDL or Verilog
CR Number: 421225
- Updated the comments in the Header file for DDR2 SDRAM, DDR SDRAM and QDR2 Virtex-5 designs.
CR Number: 452722
- Provided an option to include the Mask signals or No Mask signals for DDR2 SDRAM and DDR SDRAM designs for all FPGA families.
CR Number: 448876
- Reserve Pin list banks is updated to hierarchical view.
CR Number: 448056
- DDRII SRAM Virtex-4 design is modified to use single Address FIFO for both read and write commands.
CR Number: 429909
- Implemented the dynamic pin allocation. MIG displays the information, the number of pins allocated and the number of pins required.
CR Number: 429205
- Implemented the priority bank selection. First priority is given to the exclusive Data Bank for pin allocation.
CR Number: 448875
- Provides the Memory Models for Custom Memory Parts.
CR Number: 448077
- WASSO is now applied only on output signals for RDLRAMII and DDRII SRAM designs.
CR Number: 450380
- Default data width for DDR SDRAM MT46V16M16XX-75 is set to 16 bit.
CR Number: 452677
- In 'Reserve Pins' page, 'Selected Pins' is changed to 'Available Pins'.
CR Number: 455382
- Added a Warning message in compatibility page regarding designs that will use FX PPC controller.
CR Number: 457316
- Added more description to timing spread sheets.
CR Number: 444312
- MIG highlights only the common banks in 'Bank Selection' page when 'Compatible FPGAs' are selected.
CR Number: 451463
- Implemented the 'Reserve Pin Banks' in numerical order.
CR Number: 455381