vol.11, issue 2 2Q02

designline

A quarterly publication dedicated to the promotion of technical information and ideas.

DDR333 Memory Design Guide for Two-DIMM Unbuffered Systems

This Issue:

DDR333 Memory Design Guide for Two-DIMM Unbuffered Systems

DDR memory busses vary depending on the intended market for the finished product. Some products must support four or more registered DIMMs, some are point-to-point topologies. This document focuses on solutions requiring two unbuffered DIMMs operating at a data rate of 333 MHz and is intended to assist board designers with the development and implementation of their products.

The document is split into two sections. The first section uses data gathered from a chipset and motherboard designed by Micron to provide a set of board design rules. These rules are meant to be a starting point for a board design. The second section details the process of determining the portion of the total timing budget allotted to the board interconnect. The intent is that board designers will use the first section to develop a set of general rules and then, through simulation, verify the design in their particular environment.

Introduction

Systems using unbuffered DIMMs can implement the address and command bus using various configurations. For example, some controllers have two copies of the address and command bus so the system can have one or two DIMMs per copy. Further, the address bus can be clocked using 1T or 2T clocking. With 1T, a new command can be issued on every clock cycle. 2T timing will hold the address and command bus valid for two clock cycles. This reduces the efficiency of the bus to one command per two clocks, but it doubles the amount of setup and hold time. The data bus remains the same for all of the variations in the address bus.

This design guide covers a DDR system using two unbuffered DIMMs operating at a 333 MHz data rate and two variations of the address and command bus. The first variation covered is a system with two DIMMs on the address and command bus using 1T clocking. A block diagram of this topology is shown in Figure 1. The second variation is a system with two DIMMs on the address and command bus using 2T clocking. This topology is shown in Figure 2. Please note that the guidelines provided in this section are intended to provide a set of rules for board designers to follow. It is always advisable to simulate the final implementation to ensure proper functionality.

DDR Signal Grouping

The signals that compose a DDR memory bus can be broken into three unique groupings each with their own configuration and routing rules.

Data Group: Data Strobe DQS[8:0], Data Mask DQM[8:0], Data DQ[63:0], and Check bits CB[7:0]

Address and Control Group: Bank Address BA[1:0], Address A[13:0], Command Inputs RAS#, CAS#, and WE#. Note that Clock Enable CKE[3:0], and Chip Select S[3:0]# are also part of the command signals but they have different loading and timing.

Clock Group: Differential Clocks CK[5:0], CK#[5:0]

Board Stackup

A two DIMM DDR channel can be routed on a four-layer board. The layout should be done using controlled impedance traces of Zo = 60 ohm (±10%)

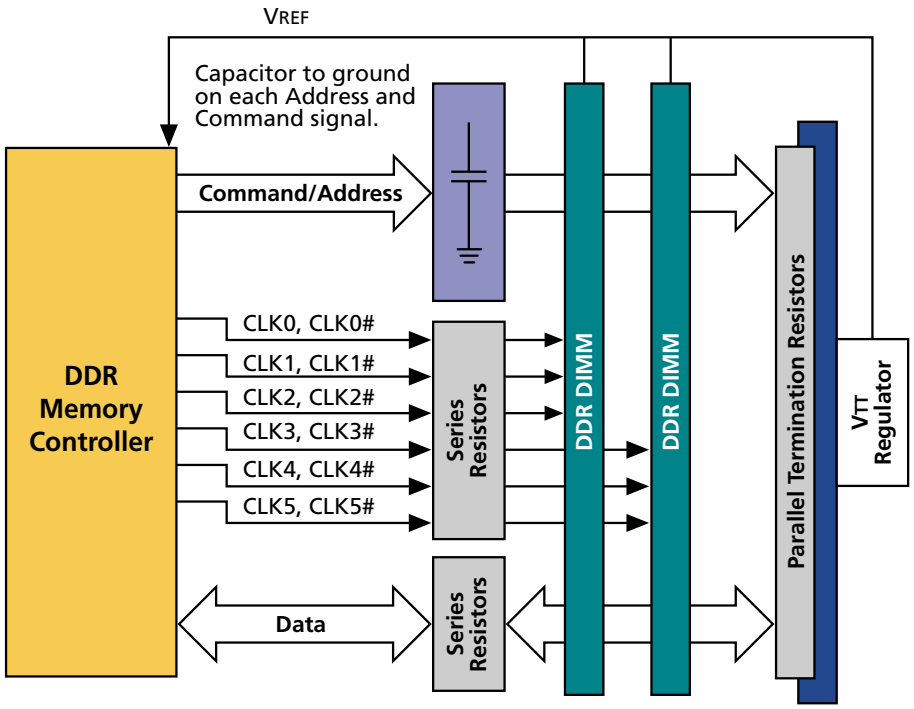


Figure 1. Two-DIMM Unbuffered DDR 333 MHz Topology 1T Address and Command Bus

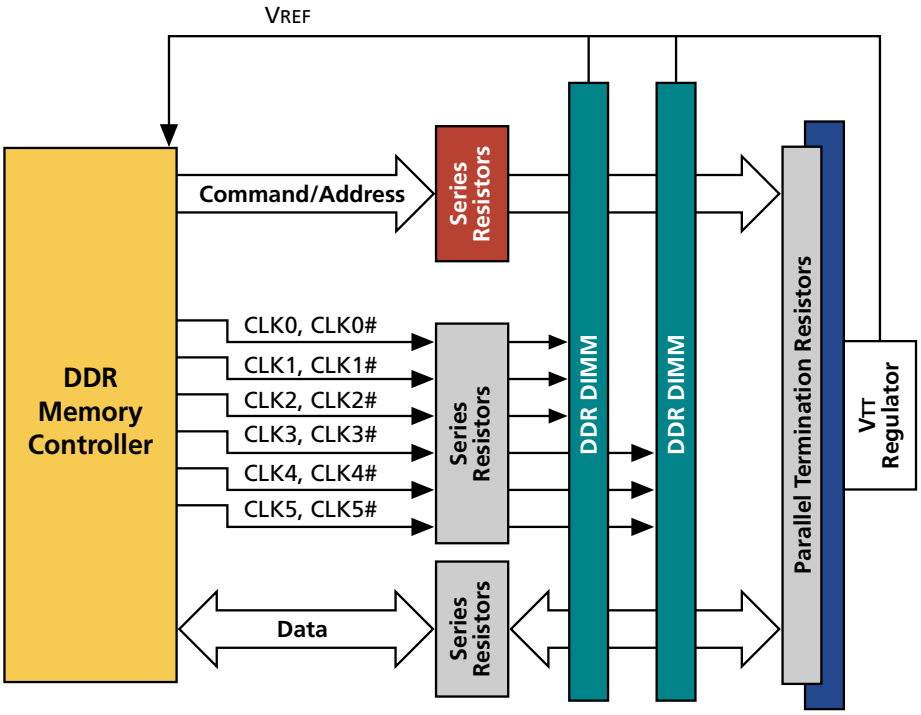


Figure 2. Two-DIMM Unbuffered DDR 333 MHz Topology 2T Address and Command Bus

characteristic impedance. The example stack up is shown in Figure 3. The trace impedance is based on a 5-mil wide trace and 1/2 oz. copper.

Address and Command Signals - 2T Clocking

On a DDR memory bus the address and command signals are unidirectional signals driven by the memory controller. For DDR333, the address and command bus runs at a clock rate of 167 MHz. The address and command signals are captured at the DRAM using the memory clocks. For a system with two unbuffered DIMMs on a single address and command bus, the loading on these signals will differ greatly depending on the type and number of DIMMs installed. A two-DIMM channel loaded with two double-sided DIMMs has 36 loads on the address and command signals. Under this heavy loading the slew rate on the address bus is slow. The reduced slew rate makes it difficult, if not impossible, to meet the setup and hold times at the DRAM. To address this issue the controller can use 2T address timing—increasing the time available for the address command bus by one clock period. Note that CS and CKE timing are not changed between 1T and 2T addressing.

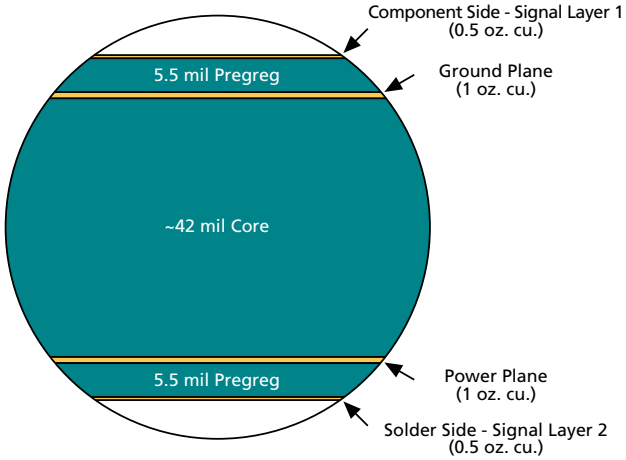


Figure 3. Sample Board Stackup

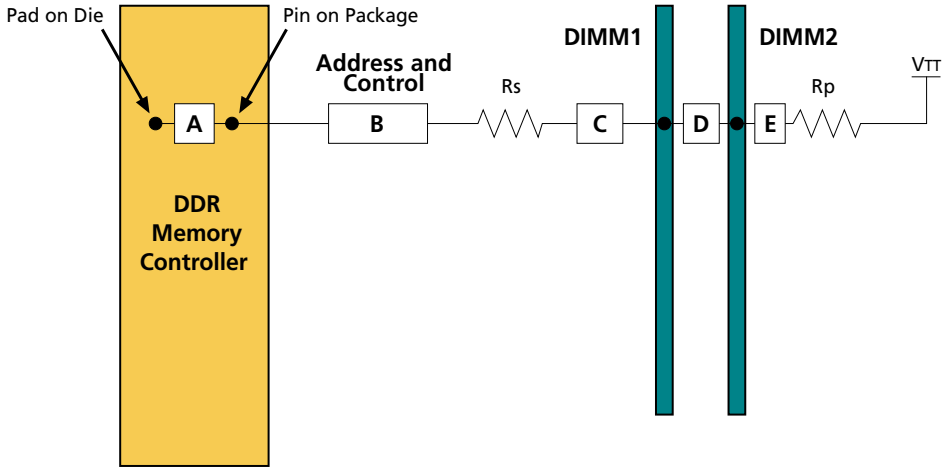


Figure 4. DDR Address and Command Signal Group Routing Topology

Table 1. Address and Command Group Routing Rules

Length
A = Obtain from DRAM controller vendor. (A is the length from the die pad to the ball on the ASIC package.)
B = 1.5 - 2.8 in.
C = 0.4 - 0.6 in.
D = 0.425 in.
E = 0.2 - 0.55 in.
Total: A + B + C = 2.4 - 3.2 in.
Length Matching
±100-mils of memory clock length at the DIMM*
Trace
Trace Width = 5 mils
Trace Space = 15 mils reducing to 11.5 mils going between the pins of the DIMM.
Trace Space from DIMM pins = 7mils
Trace Space to other signal groups = 20mils

**This value is controller-dependant, see Routing Rules on page 8.*

Series Resistors (Rs)

Location: The series resistors should be located near the first DIMM for ease of routing.

Value: The value of Rs can vary depending on the bus topology.

Range: 10-25 ohms*

Recommended: 20 ohms*

Parallel/Pull-up Resistor (Rp) Termination Resistor

Location: The parallel termination resistors should be placed behind the last DIMM slot and attached to the VTT power island.

Value: The value of the parallel resistor can vary depending on the bus topology.

Range: 25-56 ohms*

Recommended: 36 ohms*

**A recommended value. A range of values is provided for simulation when there is a need to deviate from the recommendation.*

Routing Rules

It is important that the address and command lines be referenced to a solid ground or power plane. On a four-layer board, the address and command would typically be routed on the second signal layer referenced to a solid power plane. The system address and command signals should be ground or power referenced over the entire bus to provide a low impedance current return path. The address and command signals should be kept away from the data group signals from the controller to the first DIMM.

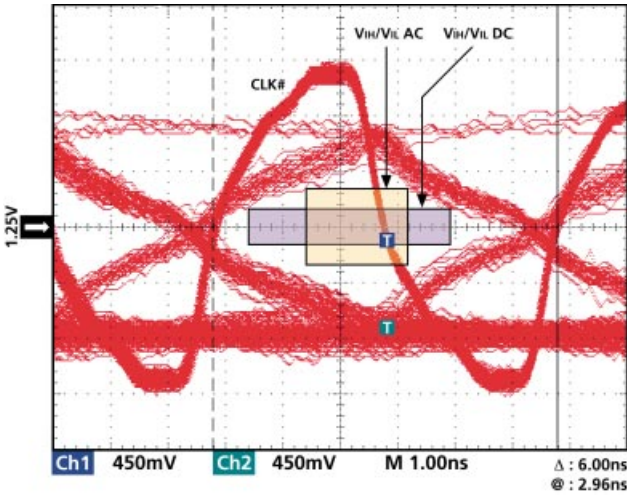


Figure 5. Uncompensated Address Line

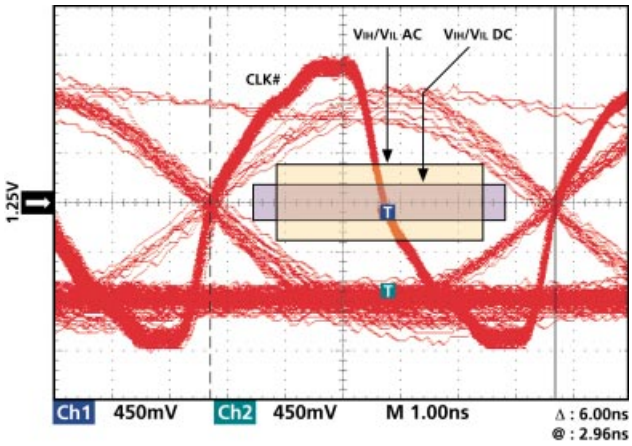


Figure 6. Compensated Address Line

Address and command signals are captured at the DIMM using the clock signals so they must maintain a length relationship to the clock signals at the DIMM.

Address and Command Signals - 1T Clocking

On a DDR memory bus the address and command signals are unidirectional signals always driven by the memory controller. For DDR333, the address runs at a clock rate of 167 MHz. The address and command signals are captured at the DRAM using the memory clocks. For a system with two unbuffered DIMMs on a single address and command bus, the loading on these signals will differ greatly depending on the type and number of DIMMs installed. A two-DIMM channel loaded with two double-sided DIMMs has 36 loads on the address and command signals. The heavy capacitive load cause a significant reduction in signal slew rate and voltage margin at the DRAM. The reduced voltage margin causes a reduction in timing margin. As a result, setup and hold times at the DRAM may not be met.

To address the poor margin, Micron has developed a compensated bus topology. This topology uses a capacitor to ground in place of the series damping resistor. A block diagram of this topology is shown in Figure 7.

Figure 5 and Figure 6 are scope captures taken off two address signals on the same system. The boxes drawn in the center of the address eye show the setup and hold times at V_{IH} and V_{IL} DC. Both signals are captured in a system populated with two double-sided DIMMs. This is the worst-case address loading situation in this type of system. All measurements are taken at room temperature and nominal voltage. The address signal in Figure 5 is using a series and parallel resistor topology. As one can see, the address signal has a slow slew rate and a low maximum V_{IH}. The combined result is a severe reduction in address setup and hold times. Under corner conditions, it is possible for this architecture to violate the DRAM setup and hold times resulting in unstable system operation. In Figure 6 the address line is using the compensated capacitor architecture. The scope capture clearly shows the improved signal quality and larger address valid window.

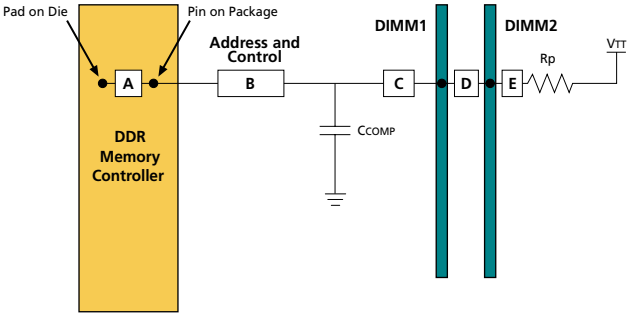


Figure 7. DDR Address and Command Signal Group Routing Topology

Table 2. Address and Command Group Routing Rules

Length
A = Obtain from DRAM controller vendor. (A is the length from the die pad to the ball on the ASIC package.)
B = 0.4 - 1.4 in.
C = 1.6 - 2.2 in.
D = 0.425 in.
E = 0.2 - 0.55 in.
Total: A + B + C = 2.4 - 3.2 in.
Length Matching
±100-mils of memory clock length at the DIMM*
Trace
Trace Space = 15 mils reducing to 11.5 mils going between the pins of the DIMM.
Trace Space from DIMM pins = 7mils
Trace Space to other signal groups = 20mils

**This value is controller-dependant, see Routing Rules on page 8.*

Routing Rules

It is important that the address and command lines be referenced to a solid ground or power plane. On a four-layer board the address and command would typically be routed on the second signal layer referenced to a solid power plane. The system address and command signals should be ground or power referenced over the entire bus to provide a low impedance current return path. The address and command signals should be kept away from the data group signals from the controller to the first DIMM. Address and command signals are captured at the DIMM using the clock signals so they must maintain a length relationship to the clock signals at the DIMM.

Compensation Capacitor (CCOMP)

Location: CCOMP should be located such that lengths B and C are close to equal.

Value: The value of CCOMP can vary depending on the bus topology.

Range: 45-82pF*

Recommended: 82pF*

Parallel/Pull-up Resistor (Rp) Termination Resistor

Location: The parallel termination resistors should be placed behind the last DIMM slot and attached to the VTT power island.

Value: The value of the parallel resistor can vary depending on the bus topology.

Range: 25-56 ohms*

Recommended: 36 ohms*

**A recommended value. A range of values is provided for simulation when there is a need to deviate from the recommendation.*

Data signals

In a DDR system the data is captured by the memory and the controller using the data strobe rather than the clock. To achieve the double data rate, data is captured on the rising and falling edge of the data strobe. Each eight bits of data has an associated data strobe (DQS) and a data mask bit (DM). Since the data is captured off the strobe the data bits associated with the strobe must be length matched closely to their strobe bit. This group of data and data strobe is referred to as a byte lane. The length matching between byte lanes is not as tight as it is within the byte lane. Table 3 shows the data and data strobe byte lane groups. Figure 8 shows the signals in a single-byte lane and the bus topology for the data signals.

Table 3. Data to Data Strobe Grouping

Data	Data Strobe	Data Mask
DQ[7:0]	DQS 0	DM 0
DQ[15:8]	DQS 1	DM 1
DQ[23:16]	DQS 2	DM 2
DQ[31:24]	DQS 3	DM 3
DQ[39:32]	DQS 4	DM 4
DQ[47:40]	DQS 5	DM 5
DQ[55:48]	DQS 6	DM 6
DQ[63:56]	DQS 7	DM 7
CB[7:0]	DQS 8	DM 8

Table 4. Data Group Routing Rules

Length
A = Obtain from DRAM controller vendor. (A is the length from the die pad to the ball on the ASIC package.) **B** = 1.5 - 2.8 in. **C** = 0.4 - 0.6 in. **D** = 0.425 in. **E** = 0.2 - 0.55 in. **Total:** A + B + C = 2.4 - 3.2 in.
Length Matching in Data/Strobe Byte Lane
±100-mils from data strobe
Length Matching Byte Lane to Byte Lane
±0.5 in of memory clock length
Trace
Trace Width = 5 mils Trace Space = 15 mils reducing to 11.5 mils going between the pins of the DIMM. Trace Space from DIMM pins = 7mils Trace Space to other signal groups = 20mils

Routing Rules

It is important that the data lines be referenced to a solid ground plane because they are operating at twice the frequency of the address and command signals. These high-speed data signals require a good ground return path to avoid degradation of signal quality due to inductance in the signal return path. The system memory signals should be ground referenced from the memory controller to the DIMM connectors and from DIMM connector to DIMM connector to provide a low impedance current return path.

This is accomplished by routing the data signals on the top layer for the entire length of the signal. The data signals should not have any vias. To help reduce crosstalk noise the data strobe signals are shielded on each side by a 5 mil ground trace.

Note: We recommend stitching shield track to ground every inch to reduce transient currents

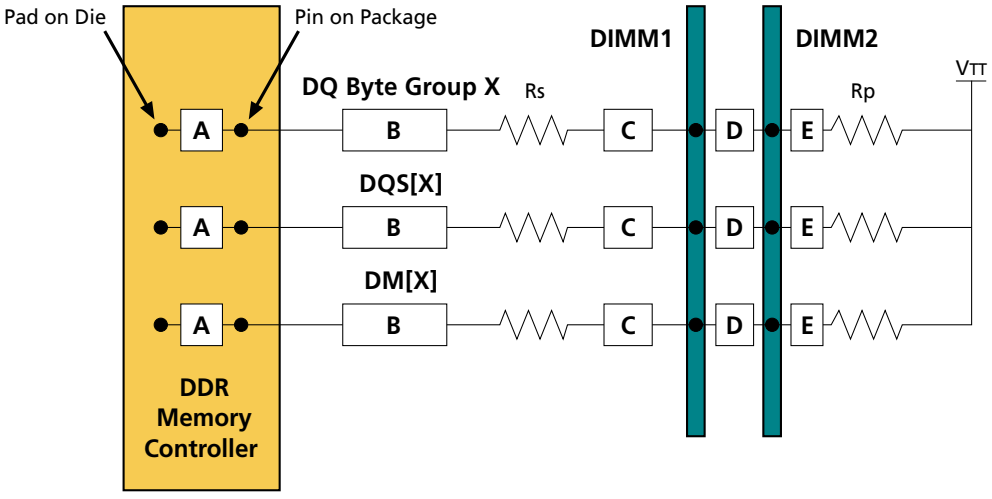


Figure 8. DDR Data Byte Lane Routing Topology

Series Resistors (Rs)

Location: The series resistors should be located near the first DIMM for ease of routing.

Value: The value of the series resistor can vary depending on the bus topology.

Range: 10-25 ohms*

Recommended: 20 ohms*

Parallel/Pull-up Resistor (Rp) Termination Resistor

Location: The parallel termination resistors should be placed behind the last DIMM slot and attached to the VTT power island.

Value: The value of the parallel resistor can vary depending on the bus lengths used.

Range: 25-56 ohms*

Recommended: 36 ohms*

**A recommended value. A range of values is provided for simulation when there is a need to deviate from the recommendation.*

Clock Signals

The memory clocks CK[5:0] and CK#[5:0] are used by the DRAM on a DDR bus to capture the address and command data. Unbuffered DIMMs require three clock pairs per DIMM. Some DDR memory controllers will drive all of these clocks and others will require an external clock driver to generate these signals. In this example it is assumed that the memory controller will drive the six clock pairs required for a two DIMM unbuffered system. Clocks are differential signals so they do not get connected to V_{TT} like the other signals of a DDR bus. The clocks are differential pairs and must be routed as a differential pair. Each clock pair is differentially terminated on the DIMM by a 120 ohm resistor. Figure 9 shows the routing topology used for the clocks. In this figure only one of the three clock pairs required by each DIMM is shown.

Routing Rules

The clocks are routed as a differential pair from the controller to the DIMM. The clocks are used to capture the address signals at the DIMM so they must maintain a length relationship to the address signals at the DIMM they are connected to. Different controllers handle the address clock relationship differently—some controllers have the ability to adjust the address to clock delay and others use a fixed delay. Memory controllers with a variable delay can better

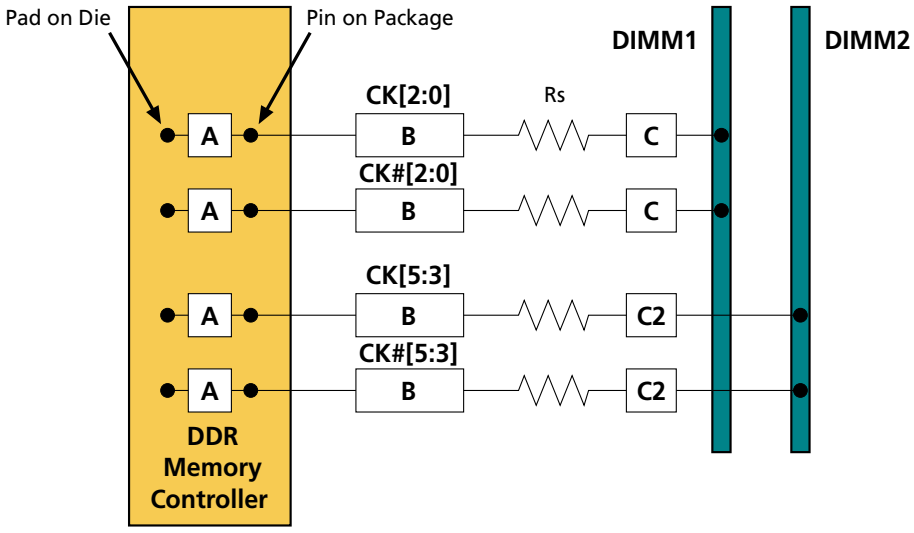


Figure 9. DDR Clock Signal Group Routing Topology

center the clock in the address valid eye over varying load conditions. Controllers with a fixed delay may require different routing of the clocks to compensate for different loading on the clock verses the address. The rules in this section are based on a controller that has variable clock delay.

DDR Memory Power Supply Requirements

A DDR bus implementation requires three separate power supplies. The DRAM and the memory portion of the controller require a 2.5 volt supply. The 2.5 volt supply provides power for the DRAM core and I/O as well as at least the I/O of the DRAM controller. The second power supply is V_{REF}, which is used as a reference voltage by the DRAM and the controller. The third supply is V_{TT} which is the termination supply of the bus. Table 6 lists the tolerances of each of these supplies.

Table 5. Clock Group Routing Rules

Length
A = Obtain from DRAM controller vendor. (A is the length from the die pad to the ball on the ASIC package.)
B = 1.5 - 2.8 in.
C = 0.4 - 0.6 in.
C2 = 0.825 - 1.025 in.
Length Matching
±30-mils for CK to CK#
±30-mils Clock pair to clock pair at the DIMM
Trace
Trace Width = 10 mils
Trace Space = 5 mils
Trace Space to other signal groups = 20 mils

Series Resistor (Rs)

Location: The series resistor is located near the driver.

Value: The value of the series resistor can vary depending on the bus topology.

Range: 22-25 ohms

Recommended: 22 ohms

MV_{TT} Voltage

The memory termination voltage, V_{TT}, requires current at a voltage level of 1.25 VDC. See Figure 6 for the V_{TT} tolerance. V_{TT} must be generated by a regulator that is able to sink and source current while still maintaining the tight voltage regulation.

- V_{REF} and V_{TT} must track variations in V_{DD} over voltage, temperature and noise ranges.
- V_{TT} of the transmitting device must track V_{REF} of the receiving device.

MV_{TT} Layout Recommendations

- Place the V_{TT} island on the component side signals layer at the end of the bus behind the last DIMM slot.
- Use a wide-island trace for current capacity
- Place V_{TT} generator as close to termination resistors as possible to minimize impedance (inductance).
- Place one or two 0.1µf decoupling cap by each termination RPACK on the V_{TT} island to minimize the noise on V_{TT}. Other bulk (10-22µf) decoupling is also recommended to be placed on the MV_{TT} island.

Table 6 Required Voltages

Symbol	Parameter	MIN	Typical	MAX	Unit
V_{DD} (V25)	Device Supply Voltage	2.3	2.5	2.7	V
V_{REF}	Memory Reference Voltage	(0.5 * V_{DD}) - 25mV	0.5 * V_{DD}	(0.5 * V_{DD}) + 25mV	V
V_{TT}	Memory Termination Voltage	V_{REF} – 40mV	V_{REF}	V_{REF} + 40mV	V

MVREF Voltage

The memory reference voltage, VREF requires approximately 3mA of current at a voltage level of 1/2 VDD with a tolerance shown in Table 6. VREF can be generated using a simple resistor divider with 1% or better accuracy. VREF must track 1/2 of VDD over voltage, noise, and temperature changes.

- Peak-to-peak AC noise on VREF may not exceed ±2% VREF (DC).

MVREF Layout Recommendations

- Use 30-mil trace between decoupling cap and destination
- Maintain a 25-mil clearance from other nets.
- Simple implementation by routing VREF on the top signal trace layer.
- Isolate VREF and/or shield with Ground.
- Decouple using distributed 0.01µf and 0.1µf capacitors by the regulator, controller, and DIMM slots. Place one 0.01µf and 0.1µf near pin one of each DIMM. Place one 0.1µf near the source of VREF, one near the VREF pin on the controller and two between the controller and the first DIMM.

Timing Budget

The previous section is useful for getting an idea of how the DDR memory bus functions and the general relationship between the signals on the bus. However, if a design should deviate from the given example, the routing rules for the design can change. Since it is unlikely that every design will follow the given example exactly, it is important to simulate the design. One of the objectives of simulation is to determine if the design will meet the signal timing requirements of the DRAM and DDR controller. To meet this objective a timing budget must be generated. This section shows how to use the data provided in the DDR DRAM and DDR controller data sheets to determine the amount of the total timing budget that the board interconnect can consume.

DDR Data Write Budget

Table 7 gives a breakdown of the timing budget for DDR WRITEs at 333 MHz. The portion of the budget consumed by the DRAM device and by the DDR controller is fixed and cannot be influenced by the board designer. The amount of the total budget

Table 7. DDR Write Budget

Element	Skew Component	Setup	Hold	Units	Comments
Transmitter	Total Skew at Transmitter	550	550	ps	From data sheet
DRAM device	^{t}DH/^{t}DS	450	450	ps	
(from spec)	Total Device	450	450	ps	From data sheet
Interconnect	XTK (cross talk) - DQ	100	100	ps	4 aggressors (A pair on each side of the victim)
	XTK (cross talk) - DQS	30	30	ps	1 shielded victim, 2 aggressors (PRBS)
	ISI - DQ	15	15	ps	
	ISI - DQS	5	5	ps	
	Path Matching	15	15	ps	Within byte lane: 165ps/in. * 0.1 in; motherboard routes account for memory controller package skew
	Input Capacitance Matching	95	95	ps	4.0 and 5.0pF loads, strobe and data shift differently
	Rterm V_{OH}/V_{OL} skew (1%)	20	20	ps	
	Input Eye Reduction (V_{REF})	100	100	ps	±75 mV included in DRAM skew; additional = (±25 mV) / (.5 V/ns). This includes DQ and DQS
	Strobe-to-Data Skew	10	+10	ps	Strobe shifts relative to data (1010 pattern vs. PRBS)
Total Interconnect	Interconnect Skew	390	390	ps	From Simulation
Total Budget	3000/2 @ 333 MHz	1500	1500	ps	
Total Budget Consumed by Controller & DRAM	Transmitter + DRAM	1000	1000	ps	
Interconnect Budget	Total - (Transmitter + DRAM)	500	500	ps	Must be greater than amount consumed by board interconnect.

Note: *These are worst case slow numbers (100C, 2.375V, slow process).*

remaining after subtracting the portion consumed by the DRAM and the controller is what remains for the board interconnect. This is the portion that is used to determine the bus routing rules. The different components of the board interconnect are broken out. The board designer can make trade-offs with trace spacing, length matching, resistor tolerance, etc., to determine the best interconnect solution.

Determining DRAM Write Budget Consumption

The amount of the write budget consumed by the DRAM is easily obtained from the data sheets. The DRAM data sheet provides the data input hold time relative to strobe (^{t}DH) and the data input setup time relative to strobe (^{t}DS). These numbers are entered directly into the timing budgets for setup and hold. They account for all of the write timing budget consumed by the DRAM.

Determining DDR Controller Write Budget Consumption

To calculate the amount of the setup timing budge consumed by the DDR controller on a DRAM WRITE, find the value for ^{t}DQSU minimum. This is the minimum amount of time all data will be valid before the data strobe transitions shown in Figure 10. ^{t}DQSU should take clock asymmetry into account. In an ideal situation ^{t}DQSU would be equal to 1/4 * ^{t}CK. The difference between 1/4 * ^{t}CK and ^{t}DQSU is the amount of the write timing budget consumed by the controller for setup. From this the following equation is derived.

Controller setup data valid reduction = 1/4 * ^{t}CK - ^{t}DQSU

To calculate the hold time use the same equation only use ^{t}DQHD in place of ^{t}DQSU.

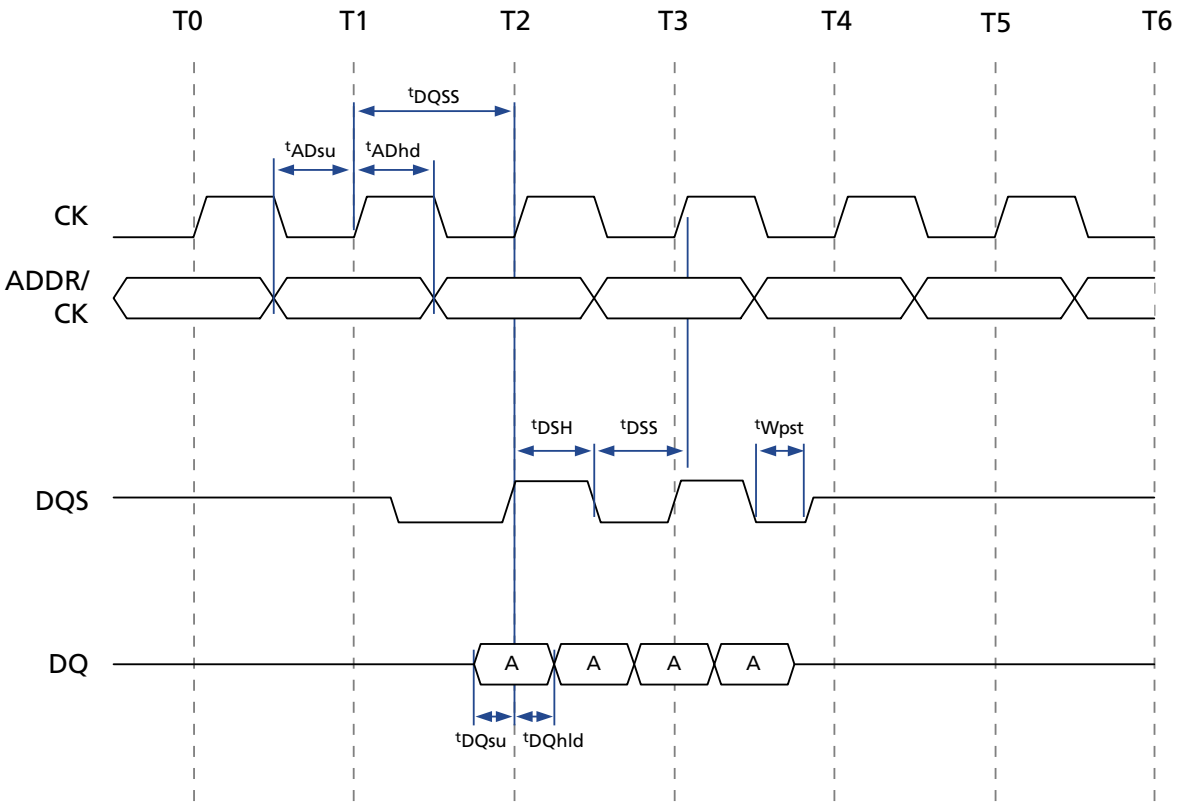


Figure 10. Memory Write and ADDR/CMD Timing

Table 8. DDR Read Budget

Element	Skew Component	Setup	Hold	Units	Comments
DRAM device	Clock	6	6	ns	
(from spec)	^{t}HP (^{t}CL/^{t}CH[MIN] at 45/55)	2.70	2.70	ns	
	^{t}DQSQ	350	350	ps	
	^{t}QHS	500	500	ps	
	^{t}QH (^{t}HP - ^{t}QHS)	2.20	2.20	ns	
	^{t}DV (^{t}HP - ^{t}DQSQ - ^{t}QHS or ^{t}QH - ^{t}DQSQ)	1.85	1.85	ns	
	[^{t}CK/2-^{t}DV]/2	575	575	ps	
DRAM Total	Total DRAM data valid reduction	575	575	ps	From data sheet
Receiver (controller)	Total skew at receiver	550	550	ps	From data sheet
Interconnect	XTK (cross talk) - DQ	70	70	ps	4 aggressors (a pair on each side of the victim)
	XTK (cross talk) - DQS	35	35	ps	1 shielded victim, 2 aggressors (PRBS)
	ISI - DQ	50	50	ps	Spice generated eye diagram
	ISI - DQS	15	15	ps	
	Path Matching	20	20	ps	Within byte lane: 165 ps/in * 0.1 in; MB routes acct. for MC pkg. skew
	Rterm V_{OH}/V_{OL} skew (1%)	20	20	ps	
	Input Eye Reduction (V_{REF})	100	100	ps	±75 mV included in DRAM skew; additional = (±25 mV) / (.5 V/ns). This includes DQ and DQS
Interconnect Total	Total Skew at Interconnect	310	310	ps	From Simulation
Total Budget	3000/2@333 MHz	1500	1500	ps	
Total budget Consumed by Controller & DRAM	Receiver + DRAM	1125	1125	ps	
Interconnect Budget	Total - (Transmitter + DRAM)	375	375	ps	Must be greater than amount consumed by board interconnect.

Note: *These are worst case slow numbers (100C, 2.375V, slow process).*

DDR Data Read Budget

Table 8 gives a breakdown of the timing budget for DDR reads at 333 MHz. The portion of the budget consumed by the DRAM device and by the DDR controller is fixed and cannot be influenced by the board designer. The amount of the total budget remaining after subtracting the portion consumed by the DRAM and the controller is what remains for the board interconnect.

Determining DRAM Read Budget Consumption

Figure 11 shows how the information from the DRAM data sheet affects the total data valid window as the data is driven from the DRAM device. This

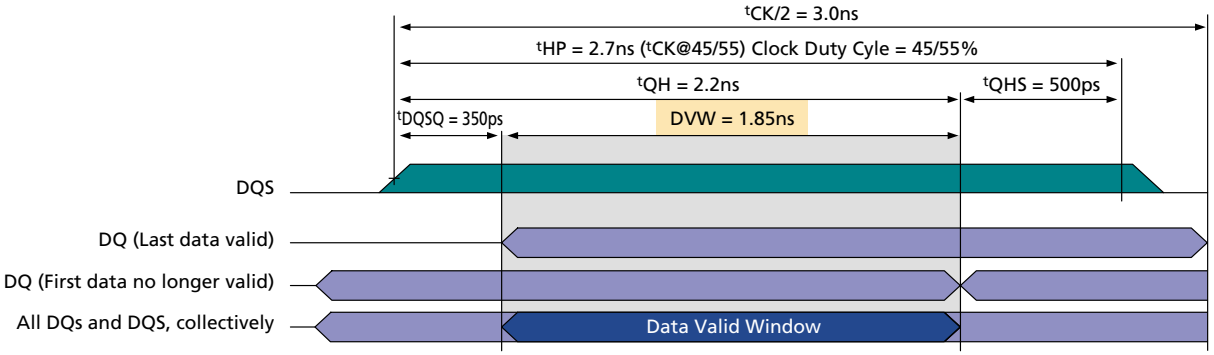


Figure 11. DRAM Read Data Valid

information is used in the timing budget to determine the amount of the total data timing budget that is consumed by the DRAM device. The total budget for the data is half the clock period. This time is halved again to determine the time allowed for setup and hold. Using the DRAM data sheet and filling in numbers for the timing parameters in Figure 11, the total data valid window at the DRAM can be calculated using the following equation:

DVW = ^{t}Hp - ^{t}DQSQ - ^{t}QHS

^{t}CK/2 - DVW/2 = DRAM data valid reduction.

The DRAM data valid reduction is used in the timing budget for setup and hold.

Determining DDR Controller Read Budget Consumption

When read data is received at the controller from the DRAM the strobe is edge aligned with the data. It is the responsibility of the controller to delay the strobe and then use the delayed strobe to capture the read data. The controller will have some minimum value it can accept for a data valid window. Internally the controller has a minimum setup and hold time that the data must maintain from the

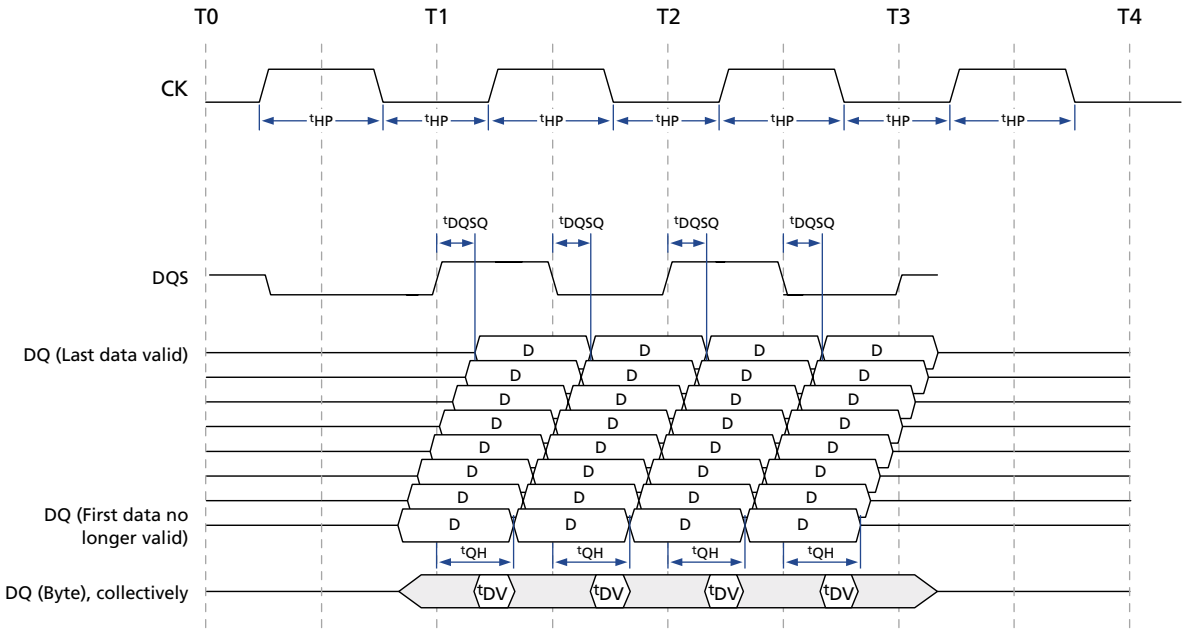


Figure 12. Read Data Timing

internally delayed strobe. Half the data valid window is the setup or hold time required by the controller plus any controller introduced signal skew and strobe centering uncertainty. The timing diagram example in Figure 12 shows the timing parameters required for calculating the data valid window. ^{t}DQSQ is the maximum delay from the last data signal to go valid after the strobe transitions. ^{t}QH is the minimum time all data must remain valid after strobe transitions. Use the following equation to obtain ^{t}DV:

$$^{t}DV = {}^{t}QH - {}^{t}DQSQ$$

Assuming ^{t}DV is split evenly between setup and hold, the portion of the timing budget consumed by the controller for setup and hold is 1/2 ^{t}DV. For the controller used in this example, an even split between setup and hold can be assumed because the controller determining the center of the data eye during the bootup routine and the DLL maintains this relationship over temperature and voltage variations.

Address Timing Budget

Table 9 gives a breakdown of the timing budget for 1T address and command at a 167 MHz clock rate. The portion of the budget consumed by the DRAM device and the DDR controller is fixed and can not be influenced by the board designer. The amount of the total budget remaining after subtracting the portion consumed by the DRAM and the controller is what remains for the board interconnect.

Determining DRAM Address Budget Consumption

The portion of the address budget consumed by the DRAM is obtained by getting the value of ^{t}IS for setup and ^{t}IH for hold. ^{t}IH and ^{t}IS are the setup and

Table 9. Address Timing Budget

Element	Skew Component	Setup	Hold	Units	Comments
Transmitter	Memory Controller Transmitter	550	550	ps	Chipset
Receiver	DRAM Skew	850	750	ps	^{t}IS, ^{t}IH from DRAM spec (Slow Edge). ^{t}IS: Additional 50ps for every .1V/ns below .5V/n (0.3V/ns)
Interconnect	Cross talk: Address	640	640	ps	1 victim (1010...), 4 aggressors (PRBS)
	ISI: Address	690	690	ps	(PRBS)
	Crosstalk: Clock	25	25	ps	Spec.
	V_{REF}: Reduction	50	50	ps	±75 mV included in DRAM skew; additional = (±25 mV) / (.5 V/ns)
	Path Matching	15	15	ps	Within byte lane: 165 ps/in * 0.1 in; MB routes acct. for MC pkg. skew
	Input Capacitance Matching	105	105	ps	1.5pF for 5 device, 2.5pF for 18 device (1610-1400) = 210 total
	Compensating Capacitor Skew (5%)	60	60	ps	Compensating Capacitor 5% Tolerance
	Rterm V_{OH}/V_{OL} Skew (1%)	10	10	ps	Estimator tool
Total Interconnect	Total Skew at Interconnect	1595	1595	ps	
Total Budget	6000 @ 333 MHz	3000	3000	ps	333 MHz-bit width
Total budget Consumed by Controller & DRAM	Transmitter + DRAM	1400	1300	ps	
Interconnect Budget	Total - (Transmitter + DRAM)	1600	1700	ps	

Note: *These are worst case slow numbers (100C, 2.375V, slow process).*

hold times required by the DRAM inputs. For systems with heavy loading on the address and command lines the value in the data sheet must be derated depending on the slew rate. For Micron DDR DRAM the setup is time is raised by 50ps for each 100mV/ns the slew rate drops below 0.5V/ns. The hold time is not changed.

Determining Controller Address Budget Consumption

The DRAM controller will provide a minimum setup and hold time for the address and command signals with respect to clock. These two parameters added together will be less than the total clock cycle. Half the difference for the setup and hold time consumed by the controller.

Clock to Data Strobe Relationship

The DDR DRAM and the DDR controller must move the data from the data strobe clocking domain into the DDR clock domain when the data is latched internally. Due to this requirement the data strobe must maintain a relationship to the DDR clock. For the DDR DRAM this relationship is specified by ^{t}DQSS. This timing parameter states that after a WRITE command the data strobe must transition 0.75 to 1.25 * ^{t}CK. Figure 10 shows the DDR controller also specifies a ^{t}DQSS timing parameter. This is the time after the WRITE command that the data strobe will transition. For the controller in this example ^{t}DQSS = ±0.06 * ^{t}CK. The following equation is used to calculate the amount of clock to data strobe skew that is left for consumption by the board interconnect.

Interconnect budget = DRAM ^{t}DQSS - Controller ^{t}DQSS

Using this equation it is apparent that this is not one of the strict timing requirements of a DDR channel. If the clocks are routed so they are between the shortest and longest strobe lengths, the designer gains some leeway in the data strobe to data strobe byte lane routing restrictions.

Appendix: Simulation Result Data

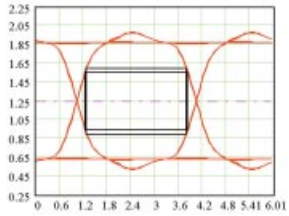
Data Bus Simulation Conditions

Standard Termination
Rs = 20
Controller Ron = 15
DRAM Ron =15
Rp = 36 Ohms
B = 2200 mils
C = 400 mils
D = 425 mils
E = 400 mils
Rise Time = 750ps
Data Rate = 333 MHz

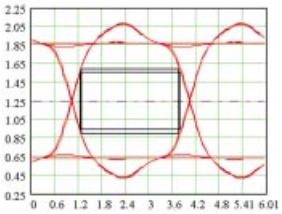
Figure 13. SSTL READs
Rs = 20 Rstub = 22 Rp = 36 Pitch = .425"

Slot 1

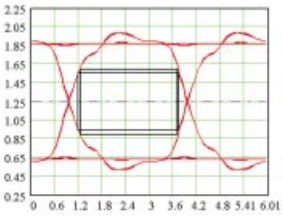
ISI_1 = 9 DD
$Apert2_1$ = 2.496 $SlewR_1$ = 1.42



ISI_3 = 23 DS
$Apert2_3$ = 2.493 $SlewR_3$ = 1.43

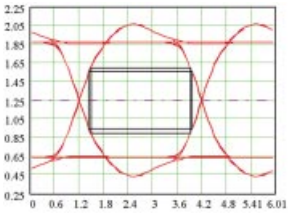


ISI_5 = 13 SD
$Apert2_5$ = 2.471 $SlewR_5$ = 1.33

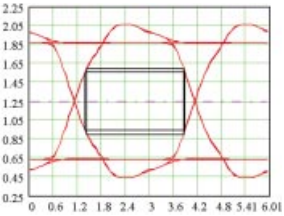


Slot 2

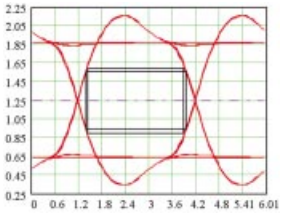
ISI_2 = 11 DD
$Apert2_2$ = 2.434 $SlewR_2$ = 1.27



ISI_4 = 11 DS
$Apert2_4$ = 2.404 $SlewR_4$ = 1.19

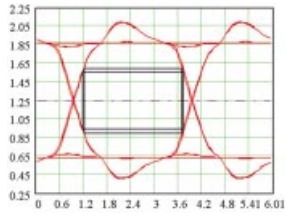


ISI_6 = 24 SD
$Apert2_6$ = 2.464 $SlewR6_1$ = 1.37

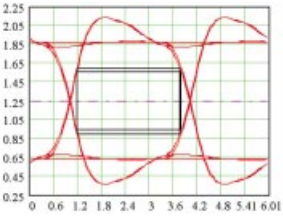


Slot 1

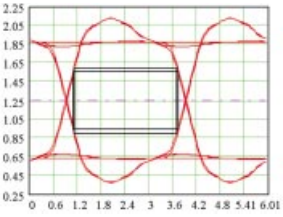
ISI_7 = 29 SS
$Apert2_7$ = 2.477 $SlewR_7$ = 1.37



ISI_9 = 25 D–
$Apert2_9$ = 2.551 $SlewR_9$ = 1.64

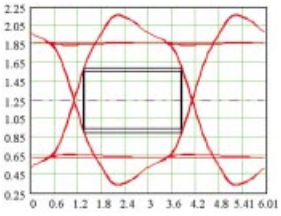


ISI_{11} = 28 S–
$Apert2_{11}$ = 2.559 $SlewR_{11}$ = 1.67

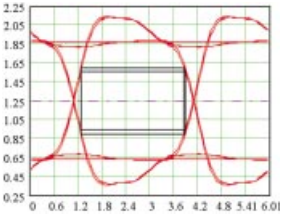


Slot 2

ISI_8 = 26 SS
$Apert2_8$ = 2.446 $SlewR_8$ = 1.31



ISI_{10} = 30 –D
$Apert2_{10}$ = 2.556 $SlewR_{10}$ = 1.69



ISI_{12} = 31 –S
$Apert2_{12}$ = 2.556 $SlewR_{12}$ = 1.75

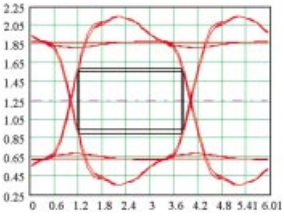
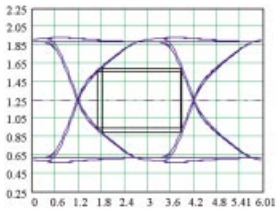


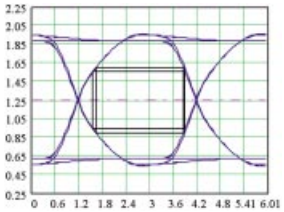
Figure 14. SSTL Writes
Rs = 20 Rstub = 22 Rp = 36 Pitch = .425”

Slot 1

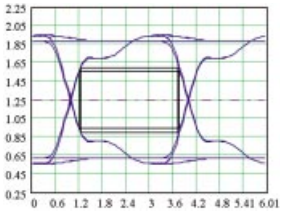
ISI_1 = 37 DD
$Apert2_1$ = 2.033 $SlewR_1$ = 0.79



ISI_3 = 21 DS
$Apert2_3$ = 2.210 $SlewR_3$ = 0.93

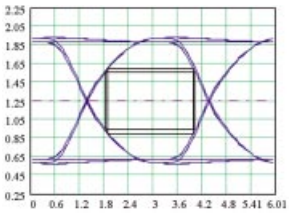


ISI_5 = 23 SD
$Apert2_5$ = 2.476 $SlewR_5$ = 1.40

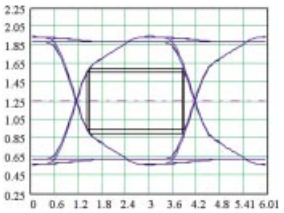


Slot 2

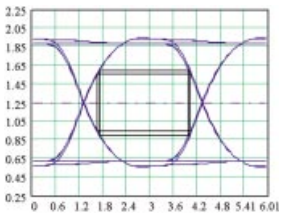
ISI_2 = 38 DD
$Apert2_2$ = 2.076 $SlewR_2$ = 0.80



ISI_4 = 20 DS
$Apert2_4$ = 2.358 $SlewR_4$ = 1.17

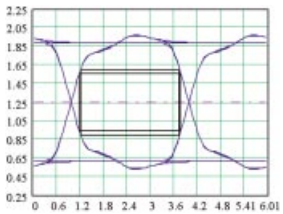


ISI_6 = 26 SD
$Apert2_6$ = 2.243 $SlewR6_1$ = 0.97

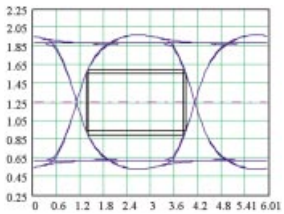


Slot 1

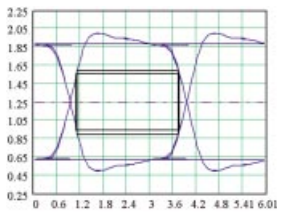
ISI_7 = 4 SS
$Apert2_7$ = 2.516 $SlewR_7$ = 1.46



ISI_9 = 3 D–
$Apert2_9$ = 2.431 $SlewR_9$ = 1.26

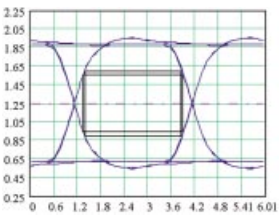


ISI_{11} = 3 S–
$Apert2_{11}$ = 2.589 $SlewR_{11}$ = 1.71

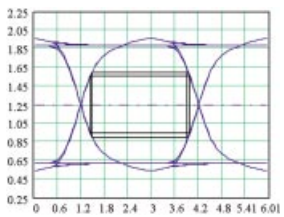


Slot 2

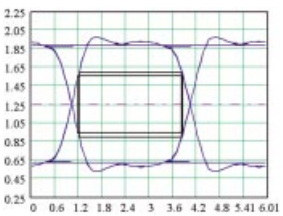
ISI_8 = 5 SS
$Apert2_8$ = 2.470 $SlewR_8$ = 1.34



ISI_{10} = 8 –D
$Apert2_{10}$ = 2.428 $SlewR_{10}$ = 1.26



ISI_{12} = 3 –S
$Apert2_{12}$ = 2.590 $SlewR_{12}$ = 1.72



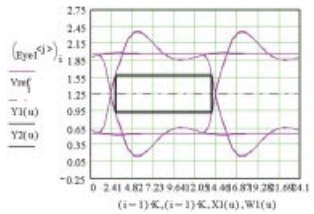
Address Bus Simulation Conditions

Standard Termination
Rs = 10
Controller Ron = 15
Rp = 33 ohms
B = 2750 mils
C = 250 mils
D = 425 mils
E = 400 mils
Rise Time = 700ps
2T Cycle @ 83 MHz
A1 address line is simulated.
Waveform shown are @ U1 memory device for both the slots

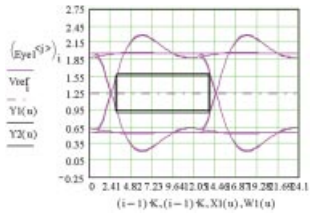
Compensated
Fcap = 82pF
Controller Ron = 15 (Except last slide, where it is 25)
Rp = 33 ohms
B = 1500 mils
C = 1500 mils
D = 425 mils
E = 400 mils
Rise Time = 700ps
1T Cycle @ 166 MHz
A1 address line is simulated.
Waveform shown are @ U1 memory device for both the slots

Figure 15. Standard Termination, 2T Cycle Slot 1

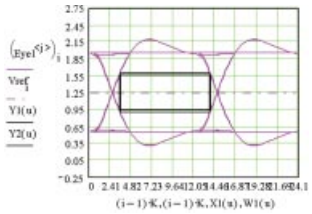
5,0
$ISI_1 = 29$
$Apert2_1 = 11.036$
$SlewR_1 = 0.72$



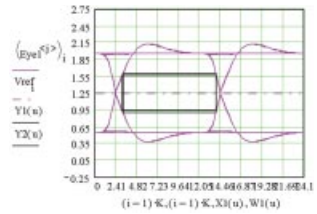
9,0
$ISI_1 = 31$
$Apert2_1 = 10.634$
$SlewR_1 = 0.49$



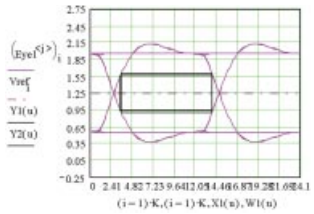
18,0
$ISI_1 = 79$
$Apert2_1 = 10.279$
$SlewR_1 = 0.41$



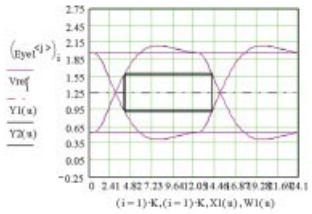
5,5
$ISI_1 = 22$
$Apert2_1 = 10.670$
$SlewR_1 = 0.52$



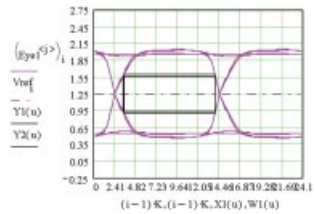
9,5
$ISI_1 = 13$
$Apert2_1 = 10.389$
$SlewR_1 = 0.42$



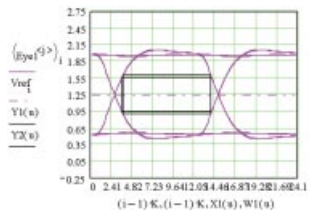
18,5
$ISI_1 = 15$
$Apert2_1 = 9.961$
$SlewR_1 = 0.34$



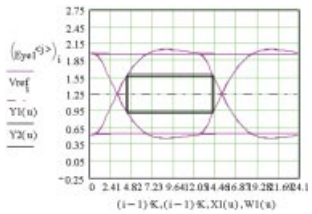
5,9
$ISI_1 = 47$
$Apert2_1 = 10.403$
$SlewR_1 = 0.43$



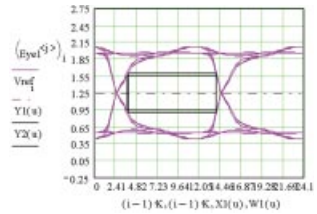
9,9
$ISI_1 = 25$
$Apert2_1 = 10.165$
$SlewR_1 = 0.38$



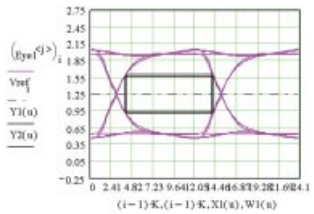
18,9
$ISI_1 = 6$
$Apert2_1 = 9.743$
$SlewR_1 = 0.31$



5,18
$ISI_1 = 38$
$Apert2_1 = 10.115$
$SlewR_1 = 0.36$



9,18
$ISI_1 = 85$
$Apert2_1 = 9.831$
$SlewR_1 = 0.32$



18,18
$ISI_1 = 77$
$Apert2_1 = 9.392$
$SlewR_1 = 0.27$

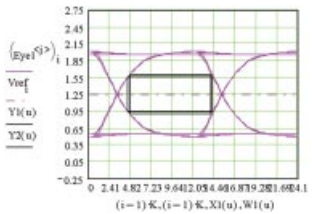
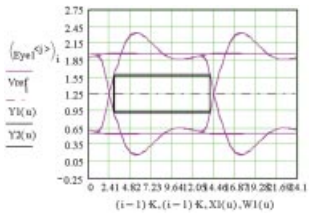


Figure 16. Standard Termination, 2T Cycle Slot 2

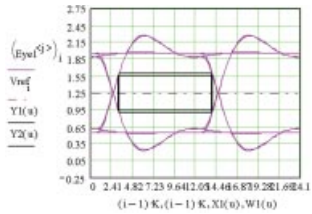
0,5

$ISI_1 = 22$
$Apert2_1 = 10.982$
$SlewR_1 = 0.68$



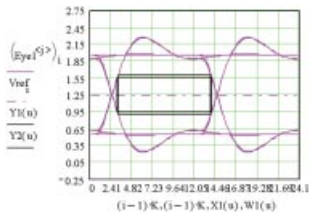
0,9

$ISI_1 = 40$
$Apert2_1 = 10.608$
$SlewR_1 = 0.49$



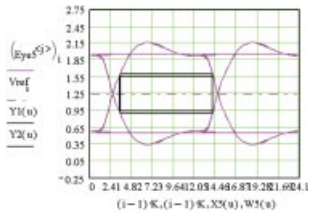
0,18

$ISI_1 = 77$
$Apert2_1 = 10.244$
$SlewR_1 = 0.40$



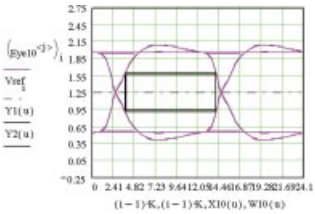
5,5

$ISI_1 = 14$
$Apert2_5 = 10.578$
$SlewR_5 = 0.48$



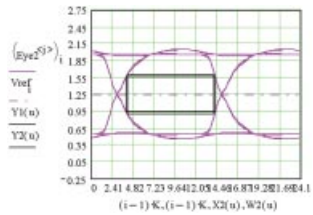
9,5

$ISI_{10} = 62$
$Apert2_{10} = 10.249$
$SlewR_{10} = 0.39$



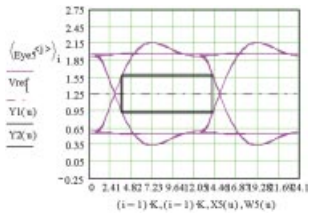
18,5

$ISI_2 = 74$
$Apert2_2 = 9.974$
$Slew2 = 0.33$



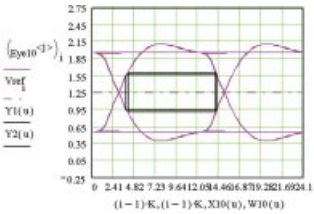
5,9

$ISI_5 = 9$
$Apert25_1 = 10.255$
$SlewR5_1 = 0.39$



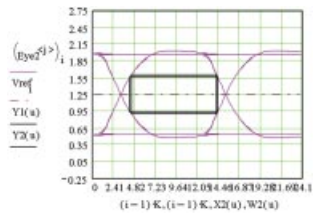
9,9

$ISI_{10} = 41$
$Apert2_{10} = 10.025$
$SlewR_{10} = 0.35$



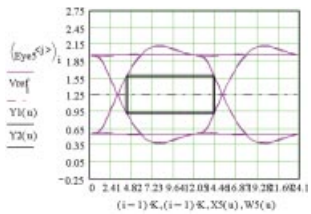
18,9

$ISI_2 = 6$
$Apert2_2 = 9.734$
$SlewR_2 = 0.31$



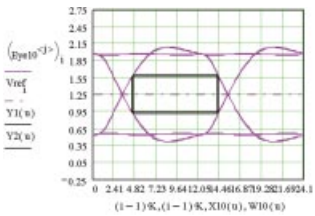
5,18

$ISI_5 = 17$
$Apert2_5 = 9.866$
$SlewR_5 = 0.32$



9,18

$ISI_{10} = 39$
$Apert2_{10} = 9.596$
$SlewR_{10} = 0.29$



18,18

$ISI_2 = 22$
$Apert2_2 = 9.326$
$SlewR_2 = 0.26$

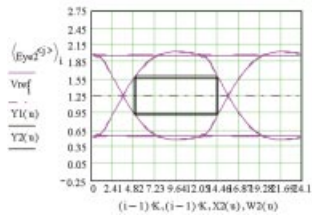
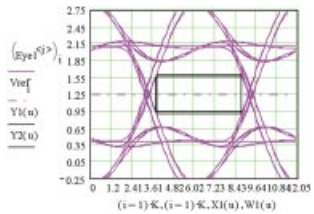
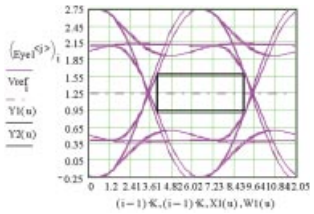


Figure 17. Compensated, 1T cycle, Slot 1

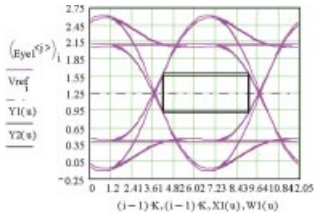
5,0 $ISI_1 = 311$ $Apert2_1 = 4.925$ $SlewR_1 = 0.77$



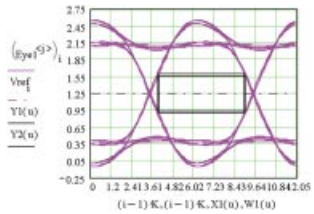
9,0 $ISI_1 = 145$ $Apert2_1 = 4.998$ $SlewR_1 = 0.71$



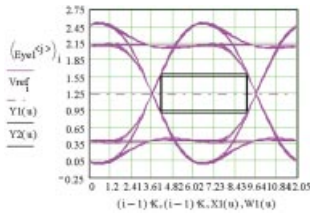
18,0 $ISI_1 = 117$ $Apert2_1 = 4.848$ $SlewR_1 = 0.62$



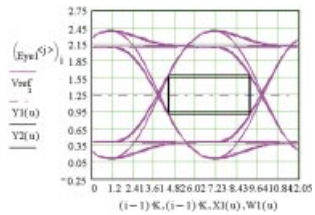
5,5 $ISI_1 = 124$ $Apert2_1 = 4.955$ $SlewR_1 = 0.70$



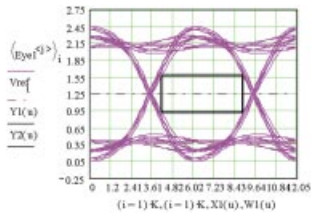
9,5 $ISI_1 = 19$ $Apert2_1 = 4.921$ $SlewR_1 = 0.64$



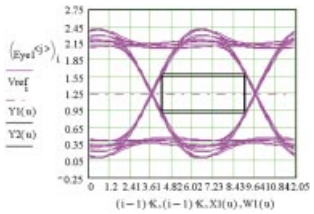
18,5 $ISI_1 = 160$ $Apert2_1 = 4.653$ $SlewR_1 = 0.55$



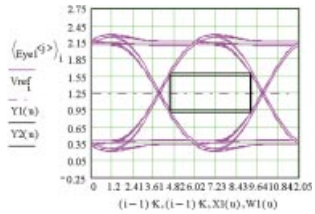
5,9 $ISI_1 = 226$ $Apert2_1 = 4.643$ $SlewR_1 = 0.58$



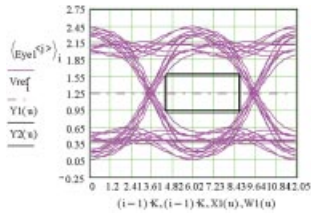
9,9 $ISI_1 = 126$ $Apert2_1 = 4.742$ $SlewR_1 = 0.60$



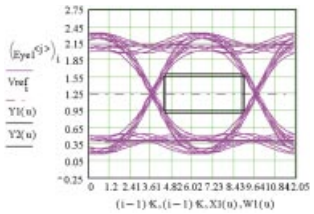
18,9 $ISI_1 = 133$ $Apert2_1 = 4.576$ $SlewR_1 = 0.53$



5,18 $ISI_1 = 418$ $Apert2_1 = 4.221$ $SlewR_1 = 0.43$



9,18 $ISI_1 = 283$ $Apert2_1 = 4.476$ $SlewR_1 = 0.46$



18,18 $ISI_1 = 65$ $Apert2_1 = 4.422$ $SlewR_1 = 0.44$

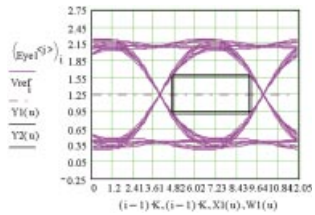
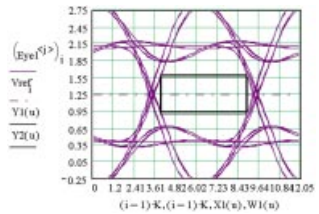


Figure 18. Compensated, 1T cycle, Slot 2

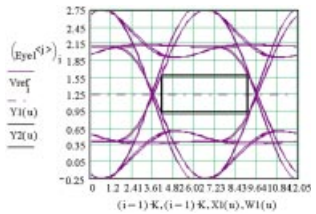
0,5

ISI_1 = 326
$Apert2_1$ = 4.907
$SlewR_1$ = 0.76



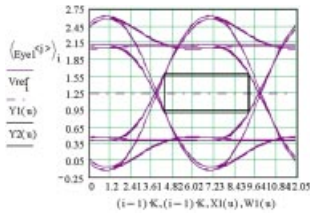
0,9

ISI_1 = 148
$Apert2_1$ = 4.955
$SlewR_1$ = 0.69



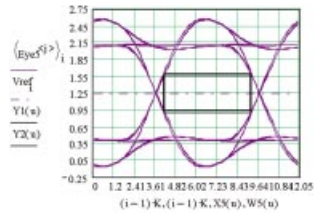
0,18

ISI_1 = 133
$Apert2_1$ = 4.809
$SlewR_1$ = 0.60



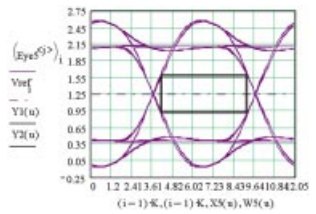
5,5

ISI_5 = 45
$Apert2_5$ = 4.971
$SlewR_5$ = 0.67



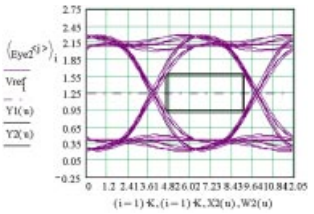
9,5

ISI_{10} = 199
$Apert2_{10}$ = 4.723
$SlewR_{10}$ = 0.61



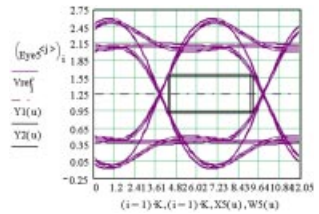
18,5

ISI_2 = 333
$Apert2_2$ = 4.397
Slew2 = 0.51



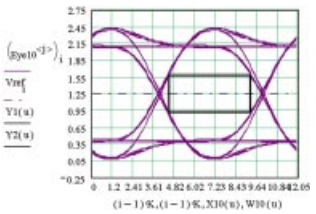
5,9

ISI_5 = 127
$Apert25_1$ = 4.747
$SlewR5_1$ = 0.59



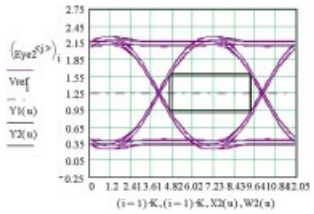
9,9

ISI_{10} = 186
$Apert2_{10}$ = 4.666
$SlewR_{10}$ = 0.56



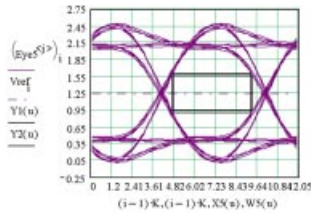
18,9

ISI_2 = 174
$Apert2_2$ = 4.531
$SlewR_2$ = 0.54



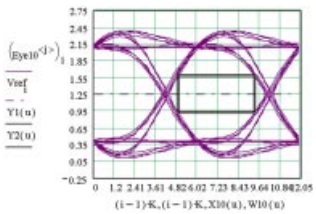
5,18

ISI_5 = 291
$Apert2_5$ = 4.503
$SlewR_5$ = 0.51



9,18

ISI_{10} = 369
$Apert2_{10}$ = 4.320
$SlewR_{10}$ = 0.47



18,18

ISI_2 = 274
$Apert2_2$ = 4.217
$SlewR_2$ = 0.45

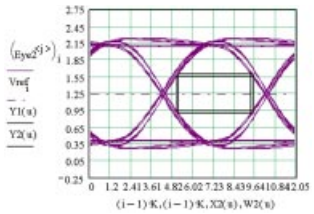
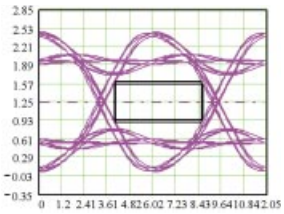


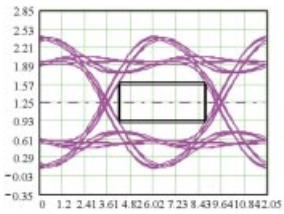
Figure 19. Compensated, 1T cycle, Slot 1
(Ron = 25, to reduce excessive overshoot in lightly loaded cases)

Slot 1

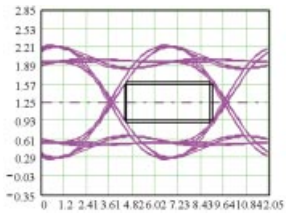
5,0 ISI_1 = 414
$Apert2_1$ = 4.547 $SlewR_1$ = 0.59



9,0 ISI_1 = 382
$Apert2_1$ = 4.505 $SlewR_1$ = 0.53

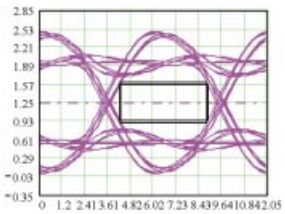


18,0 ISI_1 = 264
$Apert2_1$ = 4.426 $SlewR_1$ = 0.46

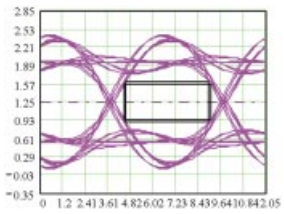


Slot 2

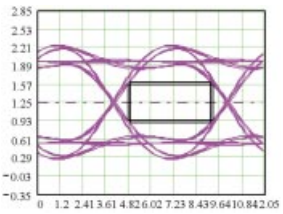
0,5 ISI_1 = 453
$Apert2_1$ = 4.519 $SlewR_1$ = 0.54



0,9 ISI_1 = 361
$Apert2_1$ = 4.433 $SlewR_1$ = 0.48



0,18 ISI_1 = 204
$Apert2_1$ = 4.247 $SlewR_1$ = 0.42



__Justin Sykes__ has ten years experience in the computer industry. He joined Micron four years ago and is currently an applications engineer. Justin holds a Bachelor of Science degree in Computer Engineering from California State University, Chico.

Micron Technology, Inc., Headquarters
8000 S. Federal Way • P.O. Box 6 • Boise, Idaho 83707-0006 • Tel: 208-368-3900 •Fax: 208-368-4617 • E-mail: prodmktg@micron.com
Customer Comment Line: 800-932-4992 • Customer Comment Fax Line: 01-208-368-5018

www.micron.com