AR #25056 - MIG v1.72 - Release Notes and Known Issues for 9.1i IP Update 3 (9.1i_IP3)

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Description

Keywords: CORE Generator, ISE, installation, IP, update, Memory, Interface, MIG, Controller, DDR, SDRAM, QDRAM

This Release Notes and Known Issues Answer Record is for the Memory Interface Generator, MIG, v1.72 released in 9.1i IP Update 3, and contains the following information:

- General Information
- Software Requirements
- New Features
- Bug Fixes
- Known Issues

For installation instructions, general CORE Generator known issues, and design tools requirements, see (Xilinx Answer 24847).

Solution

General Information

- MIG is no longer provided as a separate download, but is now incorporated into IP Updates. MIG 1.72 is the first MIG release included in an IP Update and is available through 9.1i IP Update 3. MIG 1.72 is the MIG 1.7 release brought into the IP Update with a few bug fixes that are noted below.

Software Requirements

- ISE 9.1.01i
- Windows XP (32 bit)

New Features

MIG 1.7 New Features

General New Features and Changes
- Supports "Create New Memory Part" for all the designs.
- DDR and DDR2 SDRAM designs for Spartan-3A.
- DDR SDRAM is supported for Virtex-5.
- VHDL is supported for Virtex-5 DDR2 SDRAM and QDR II SRAM.
- MIG now pops up the design notes specific to the generated design.
- Supports Pin Out compatibility with MIG 1.5 and MIG 1.6 for Spartan-3 and Spartan-3E designs.
- ECC check box changed to Combo box to support Pipelined and Unpipelined modes.
- Supports differential and nondifferential strobes for Spartan-3A DDR2 and Virtex-4 DDR2.
- Pops up an information note if user selects the invalid data width or unsupported data width for a particular FPGA of Spartan-3/-3E/-3A.
- Generates a script file for running MIG designs through Project Navigator GUI. This is supported only when the flow vendor is "XST."
- Default setting "DCI for Address and Control " is changed to "unChecked."
- Frequency slider is changed to editable box in the GUI.
- Supports only alphanumeric characters and underscore ('_') for the module name and also for the New Name in Edit Signal Names.
- Removed console window when running MIG through CORE Generator.
- WASSO table (Set Advanced Options) accepts only numeric characters.

- The maximum frequency for Spartan-3, -5 is set to 133 MHz if the data width is greater than 32.
- Provided web links for all Application Notes in the documents folder of the designs.
- Provided link to Data Sheet instead of Log Sheet in the output window.
- Support of Constraint "CONFIG PROHIBIT" while reading the UCF in the reserve pins window.
- WASSO limits the number of pins to be used in a bank per controller. For example, in multi controller design, if WASSO is set to 10 in a bank, tool allocates 10 pins for each controller in that bank.
- The designs are independent of the memory part package; consequently, the package part of the memory component name is replaced with XX or XXX, where XX or XXX indicates "don't care" condition.

Virtex-5 New Features and Changes

DDR2 SDRAM
- New controller with several high-performance features. All the features are described in detail in the Application Notes.
- Enhanced data calibration algorithms for higher reliability.
- Bank Management feature is supported.
- Supports VHDL.
- The user is no longer required to set address A10 (and skip this bit in their memory space) when issuing a command to the controller in order to prevent an auto-precharge from occurring on the DDR2 bus. The controller now always forces this bit to 0 on the DDR2 bus, and the memory space presented to the user is now linear.
- The user Interface bus has been modified. The command (read/write) is now presented on a separate bus from the address. See the MIG User Guide for a definition of the User I/F bus.
- Several enhancements have been made to the pin allocation algorithms which causes the pin-outs to be different between MIG1.7 and previous versions:
-- Increased efficiency when DCI is not used. MIG now allocates VRP and VRN pins for other signals.
-- WASSO is applied to all the memory interface signals.
-- Signals such as "Error" outputs are not part of the WASSO count.

DDR SDRAM
- This is a new design for MIG. Supports Verilog and VHDL.
- Bank Management feature is supported.
- The user is no longer required to set address A10 (and skip this bit in their memory space) when issuing a command to the controller in order to prevent an auto-precharge from occurring on the DDR bus. The controller now always forces this bit to 0 on the DDR bus and the memory space presented to the user is now linear.

QDRII SRAM
- Added support for VHDL.
- Added support for 72-bit designs.
- Added first level of calibration. This includes a dummy write of 1s and 0s to the memory. This pattern helps to calibrate for the CQ/Q delay.
- Moved the pattern generation to the phy_write module. This was in the test_data_gen in MIG 1.6.
- A user_qr_valid signal is now being generated to the backend. This signal helps generate the User_qen_n signal to the read data FIFOs. The MIG 1.6 code used the user_qr_empty from all the read data FIFOs. This change was done for timing reasons.
- Several enhancements have been made to the pin allocation algorithms, causing the pin-outs to be different between MIG v1.7 and previous versions:
-- Increased efficiency when DCI is not used. MIG now allocates VRP and VRN pins for other signals.
-- WASSO is applied to the output signals only.

Virtex-4 New Features and Changes
DDR2 SDRAM Direct Clocking
- Calibration logic now centers and deskews each bit of data. This change improves the frequency performance of the design.
- Independent clock pins are generated for each load in deep designs. This change reduces the load on clock pins.
- There is a new option for the user to select the reset polarity. This option is in the parameter file. The parameter reset_active_low can be changed for active high reset. By default, this is set to 1.
- ECC check box changed to combo box to support Pipelined and Unpipelined ECC options.
- DQS# Enable, burst type and ODT of 50 ohm are selectable from GUI through Mode registers.
- Removed all TIGs in UCF. The reset signal is now registered in every module.
- The IDELAY module now uses CLK0, instead of CLK50. CLK0 is used for the refresh counter. Previously, a divide clock was used for refresh logic.
- SYS_RESET_IN changed to SYS_RESET_IN_N, to follow standard convention for active low signal.
- Removed XC_PROPS. The "defparams" that are defined for simulation will now work for both XST and Synplicity.
- Replaced "defines with localparams" for Verilog.
- Read enable in the pattern calibration logic is now generated after comparing two positive edge data and two negative edge data. This removes any spurious read enables.
- Several state machines now use "One-Hot Encoding."
- Reset generation logic has been modified to make it synchronous with DCM Lock and DCM output clocks.
- Signal INIT_DONE is brought to top module.
- Removed the UniSim primitive components declaration from VHDL modules.
- All multiples of 8-bit data widths even for x16 memory devices are now supported.
- Memory devices of speed grades -3 and -667 are now supported.

- Several enhancements have been made to the pin allocation algorithms, causing the pin-outs to be different between MIG v1.7 and previous versions:
-- Increased efficiency when DCI is not used. MIG now allocates VRP and VRN pins for other signals.
-- WASSO is applied to all the memory interface signals.
-- Signals such as "Error" outputs are not part of the WASSO count.

DDR2 SDRAM SERDES Clocking
- Implemented a new calibration scheme. This new algorithm reduces the DCM utilization and improves the timing analysis. More details can be found in the Application Note.
- There is a new option for the user to select the reset polarity. This option is in the parameter file. The parameter reset_active_low can be changed for active high reset. By default, this is set to 1.
- Support for ODT.
- DQS# Enable is selectable from GUI through Mode registers.
- Removed all TIGs in UCF. The reset signal is now registered in every module.
- The IDELAY module now uses CLK0, instead of CLK50. CLK0 is used for the refresh counter. Previously, a divide clock was used for refresh logic.
- SYS_RESET_IN changed to SYS_RESET_IN_N, to follow standard convention for active low signal.
- Removed XC_PROPS. The "defparams" that are defined for simulation will now work for both XST and Synplicity.
- Replaced "defines with localparams" for Verilog.
- Reset generation logic has been modified to make it synchronous with DCM Lock and DCM output clocks.
- Removed the UniSim primitive components declaration from VHDL modules.
- We now support all multiples of 8-bit data widths, even for x16 memory devices.
- Signal INIT_COMPLETE is brought to top module.
- Memory devices of speed grades -5E and -40E are now supported.
- Several enhancements have been made to the pin allocation algorithms, causing the pin-outs to be different between MIG v1.7 and previous versions:
-- Increased efficiency when DCI is not used. MIG now allocates VRP and VRN pins for other signals.
-- Signals such as "Error" outputs are not part of the WASSO count.

DDR SDRAM
- There is a new option for the user to select the reset polarity. This option is in the parameter file. The parameter reset_active_low can be changed for active high reset. By default, this is set to 1.
- Removed all TIGs in UCF. The reset signal is now registered in every module.
- The IDELAY module now uses CLK0, instead of CLK50. CLK0 is used for the refresh counter. Previously, a divide clock was used for refresh logic.
- SYS_RESET_IN changed to SYS_RESET_IN_N, to follow standard convention for active low signal.
- Removed XC_PROPS. The "defparams" that are defined for simulation will now work for both XST and Synplicity.
- Replaced "defines with localparams" for Verilog.
- Read enable in the pattern calibration logic is now generated after comparing two positive edge data and two negative edge data. This removes any spurious read enables.
- Modified the reset generation logic to make it synchronous with DCM Lock and DCM output clocks.
- Removed the UniSim primitive components declaration from VHDL modules.
- We now support all multiples of 8-bit data widths, even for x16 memory devices.
- The signal "init_done" is now a port in the top module.
- Several enhancements have been made to the pin allocation algorithms, causing the pin-outs to be different between MIG v1.7 and previous versions:
-- Increased efficiency when DCI is not used. MIG now allocates VRP and VRN pins for other signals.
-- WASSO is applied to all the memory interface signals.
-- Signals such as "Error" outputs are not part of the WASSO count.

RLDRAM II
- There is a new option for the user to select the reset polarity. This option is in the parameter file. The parameter reset_active_low can be changed for active high reset. By default, this is set to 1.
- Removed all TIGs in UCF. The reset signal is now registered in every module.
- The design now uses CLK0, instead of CLK50 and div16clk.
- CLK200 is changed to differential clocks in mem_interface_top module (Design top).
- The signal sysReset is changed to sysReset_n, to follow standard convention for active low signal.
- Removed unused parameters from the parameter file.
- Removed XC_PROPS. The "defparams" that are defined for simulation will now work for both XST and Synplicity.
- Replaced "defines with localparams" for Verilog.
- Modified the reset generation logic to make it synchronous with DCM Lock and DCM output clocks.
- Removed the UniSim primitive components declaration from VHDL modules.
- The signal "INIT_DONE" is now a port in the top module.
- Test bench: The bank address sequence in backend_rom has been modified so that generation sequence starts with bank 0,1,.....,6,7. The command generation in the testbench is also pipelined for BL = 2,4,8.
- Replaced "tac" with "Q to data output" instead of "Q to any data output" in the timing spread sheets.
- The INITCNT that was hard coded in rld_rst module is parameterized according to frequency by adding a new parameter "INITCNT" in parameter file.
- Several enhancements have been made to the pin allocation algorithms, causing the pin-outs to be different between MIG v1.7 and

previous versions:
-- Increased efficiency when DCI is not used. MIG now allocates VRP and VRN pins for other signals.
-- WASSO count is applied on output signals only for SIO memory types.
-- QVLD, which is an input signal, is included in WASSO count for CIO memory types. This is the limitation of the current tool.

QDRII SRAM
- There is a new option for the user to select the reset polarity. This option is in the parameter file. The parameter reset_active_low can be changed for active high reset. By default, this is set to 1.
- Timing for the signal USER_QEN_n has been changed - it is one cycle late. A register for this signal has moved from the controller to the user logic.
- Supports generation of designs without DCM.
- Part CY7C1526AV18-250BZC has been removed from Memory part list and added the CY7C1526V18-250BZC.
- Removed all TIGs in UCF. The reset signal is now registered in every module.
- The IDELAY module now uses CLK0, instead of CLK50. CLK0 is used for the refresh counter. Previously, a divide clock was used for refresh logic.
- Removed XC_PROPS. The "defparams" that are defined for simulation will now work for both XST and Synplicity.
- Replaced "defines with localparams" for Verilog.
- Modified the reset generation logic to make it synchronous with DCM Lock and DCM output clocks.
- Removed the UniSim primitive components declaration from VHDL modules.
- The signal "DLY_CAL_DONE" is now a port in the top module.
- The I/O Standard generated for system signals are LVCMOS18. Users can change this as applicable.
- Added support for DDR Byte writes.
- Several enhancements have been made to the pin allocation algorithms, causing the pin-outs to be different between MIG v1.7 and previous versions:
-- Increased efficiency when DCI is not used. MIG now allocates VRP and VRN pins for other signals.
-- WASSO is applied to the output signals only.
-- K/K# clocks, which are outputs, are not included in WASSO count. This is a limitation of the current tool.

DDRII SRAM
- There is a new option for the user to select the reset polarity. This option is in the parameter file. The parameter reset_active_low can be changed for active high reset. By default, this is set to 1.
- Timing for the signal USER_QEN_n has been changed -- it is one cycle late. A register for this signal has moved from the controller to the user logic.
- Supports generation of designs without DCM.
- Part CY7C1526V18-250BZC has been removed from Memory Parts list.
- Removed all TIGs in UCF. The reset signal is now registered in every module.
- The IDELAY module now uses CLK0, instead of CLK50. CLK0 is used for the refresh counter. Previously, a divide clock was used for refresh logic.
- Removed XC_PROPS. The "defparams" that are defined for simulation will now work for both XST and Synplicity.
- Replaced "defines with localparams" for Verilog.
- Modified the reset generation logic to make it synchronous with DCM Lock and DCM output clocks.
- Removed the UniSim primitive components declaration from VHDL modules.
- The signal "DLY_CAL_DONE" is now a port in the top module.
- The IO Standard generated for system signals are LVCMOS18. Users can change this as applicable.
- Added support for DDR Byte writes.
- Several enhancements have been made to the pin allocation algorithms, causing the pin-outs to be different between MIG v1.7 and previous versions:
-- Increased efficiency when DCI is not used. MIG now allocates VRP and VRN pins for other signals.
-- WASSO is applied to all the memory interface signals.
-- Signals such as "Error" outputs are included in WASSO count.

Spartan-3, Spartan-3E, Spartan-3A New Features and Changes
- There is a new option for the user to select the reset polarity. This option is in the parameter file. The parameter reset_active_low can be changed for active high reset. By default, this is set to 1.
- Removed all TIGs in UCF. The reset signal is now registered in every module.
- Removed XC_PROPS. The "defparams" that are defined for simulation will now work for both XST and Synplicity.
- Replaced "defines with localparams" for Verilog.
- Removed the UniSim primitive components declaration from VHDL modules.
- We now support all multiples of 8-bit data widths, even for x16 and x4 memory devices.
- The signal "cntrl0_data_valid_out" is now a port in the top module.
- DQS# Enable, burst type and ODT can be selected from the MIG GUI through the Mode registers.
- Board files for Spartan-3E starter kit provided in VHDL and Verilog.
- Implemented several changes to the controller to improve timing.
- Changed the Spartan-3/-3E pin allocation rule for increased efficiency. The previous rule was that DQs corresponding to a particular DQS could be within 5 tiles above and five tiles below the DQS. Now, the DQs can be five tiles above and six tiles below the DQS.
- Support for Spartan-3A.

Bug Fixes

Bug Fixes for MIG 1.72
- CR 437333: ECC unpiplined mode calibrates correctly in DDR2 SDRAM Virtex-4 Direct Clocking design. ECC write data is enabled with the correct control signal.
- CR 437149: DDR II SRAM V4 design generates the correct width for the "USER_BWH_n" byte write enable signal for memory component "CY7C1916BV18-250BZC."
- CR 437148: Virtex-4 QDRII SRAM design assigns appropriate widths for signals IDATA_LSB_0 and IDATA_MSB_0 in the write_data_fifo.v module.
- CR 437016: DDR SDRAM component design for VHDL/XST includes the correct reset signal in the UCF (SYS_RESET_IN_N) which allows for proper generation of the bitfile.
- CR 436879: The ML461 board files for the DDR2 SDRAM Virtex-4 Direct Clocking design correctly set the jumper location 'P10' specified in the ChipScope (.cpj) and Readme.txt files output.
- CR 436693: Virtex-5 DDR SDRAM design correctly finds optimal calibration point during stage 4 calibration and completes successfully.
- CR 436872: Corrected issues in read data timing analysis and write data timing analysis for Spartan-3/3E/3A DDR and DDR2 SDRAM designs.
- CR 436874: MIG properly allocates pins in the Spartan-3 top/bottom banks for larger data widths.
- CR 436876: The VHDL DDR SDRAM design for Spartan-3/3E/3A does not use any asynchronous resets.
- CR 438283: All DQ bits are routed correctly in Spartan-3E designs.
- CR 438284: All DQ bits are routed correctly in Spartan-3A and Spartan-3E Starter kit designs.
- CR 436878: Removed unwanted false paths defined in the .sdc file for DDR and DDR2 SDRAM designs for Spartan-3/-3E/-3A families.
- Corrected memory timing parameter values in DDR SDRAM memories.
- Updated FIFOs in RLDRAMII design to v3.3 FIFO Generator.
- MIG does not request additional pins for System Control signals when the exact number is selected in all Spartan designs.
- Spartan-3E slice location constraints corrected in ucf file to ensure the template router is used.
- When Mentor Graphics HDL is set as Folw Vendor, MIG defaults to XST. Mentor Graphics HDL is currently not supported by MIG.

Known Issues

- See (Xilinx Answer 24979) for general CORE Generator support items.
- See (Xilinx Answer 25232) for information on the Virtex-5 DDR2 SDRAM controller hanging during the third stage (read enable) of calibration.
- See (Xilinx Answer 24432) for information on mapping the user interface address to account for the auto-precharge bit A10 for Virtex-4 DDR/DDR2 SDRAM controllers and general information on mapping the user interface address for Virtex-5 DDR/DDR2 SDRAM controllers.
- See (Xilinx Answer 25261) for information on properly simulating the bank management feature for the Virtex-5 DDR2 SDRAM controller.
- Spartan-3/-3E/-3A x4 designs are only supported for data widths up to 72-bits. Wider interfaces implement with incorrect local clock routes when top/bottom banks are selected. This issue is observed only for x4 memory component and for top/bottom banks. This will be fixed in MIG 1.8.
- In Spartan-3/-3E/-3A designs, users can select "Wrtie Pipe Stages" from "Set Advanced Options." The default value of "Write Pipe Stages" is 4. If any other value (3,2,1,0) is selected, the test_bench module should include the extra pipe stages on the write data and data mask signals. This is missing in the design. There is no issue for the default Write Pipe Stage of 4. This will be fixed in MIG 1.8.
- See (Xilinx Answer 24964) for information on the "Verify My UCF" option in the MIG GUI.
- You should know the stepping level of your target Spartan-3 devices and how it affects the maximum frequency achievable for the memory component that is generated. The MIG tool does not adjust the frequency for any particular stepping level in use. Consult the relevant device data sheets or errata for more information on stepping. These documents are located at: http://www.xilinx.com/support/library.htm.

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