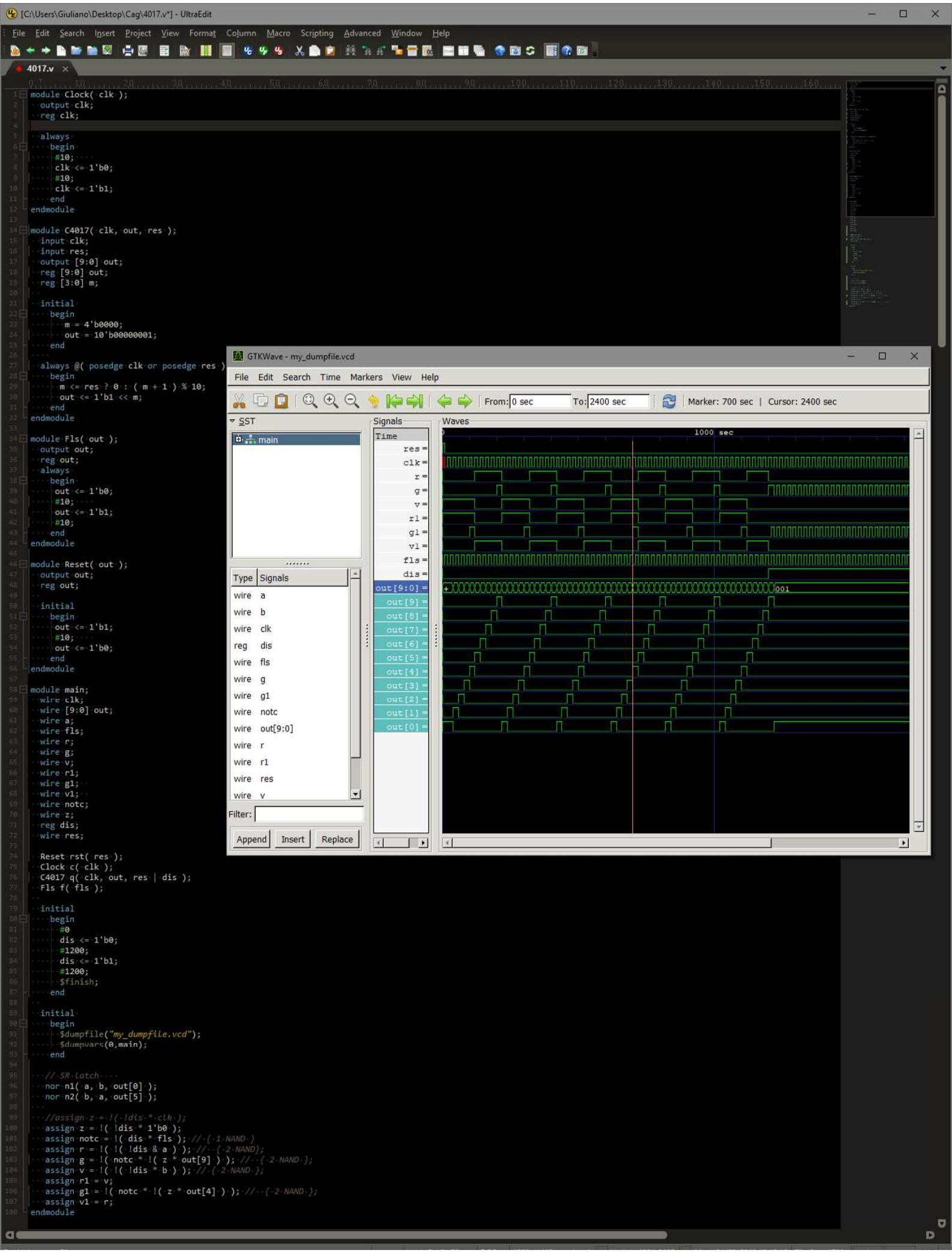
[C:\Users\Giuliano\Desktop\Cag\4017.v*] - UltraEdit
File Edit Search Insert Project View Format Column Macro Scripting Advanced Window Help
4017.v
module Clock(clk);
output clk;
reg clk;
always
begin
#10;
clk <= 1'b0;
#10;
clk <= 1'b1;
end
endmodule
module C4017(clk, out, res);
input clk;
input res;
output [9:0] out;
reg [9:0] out;
reg [3:0] m;
initial
begin
m = 4'b0000;
out = 10'b00000001;
end
always @(posedge clk or posedge res)
begin
m <= res ? 0 : (m + 1) % 10;
out <= 1'b1 << m;
end
endmodule
module Fls(out);
output out;
reg out;
always
begin
out <= 1'b0;
#10;
out <= 1'b1;
#10;
end
endmodule
module Reset(out);
output out;
reg out;
initial
begin
out <= 1'b1;
#10;
out <= 1'b0;
end
endmodule
module main;
wire clk;
wire [9:0] out;
wire a;
wire fls;
wire r;
wire g;
wire v;
wire r1;
wire g1;
wire v1;
wire notc;
wire z;
reg dis;
wire res;
Reset rst(res);
Clock c(clk);
C4017 q(clk, out, res | dis);
Fls f(fls);
initial
begin
#0
dis <= 1'b0;
#1200;
dis <= 1'b1;
#1200;
$finish;
end
initial
begin
$dumpfile("my_dumpfile.vcd");
$dumpvars(0,main);
end
//SR Latch
nor n1(a, b, out[0]);
nor n2(b, a, out[5]);
//assign z = !(!dis * clk);
assign z = !(!dis * 1'b0);
assign notc = !(dis * fls); //{1 NAND}
assign r = !(!(!dis & a)); //{2 NAND};
assign g = !(notc * !(z * out[9])); //{2 NAND};
assign v = !(!(!dis * b)); //{2 NAND};
assign r1 = v;
assign g1 = !(notc * !(z * out[4])); //{2 NAND};
assign v1 = r;
endmodule
GTKWave - my_dumpfile.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 2400 sec
Marker: 700 sec | Cursor: 2400 sec
SST
main
Type Signals
wire a
wire b
wire clk
reg dis
wire fls
wire g
wire g1
wire notc
wire out[9:0]
wire r
wire r1
wire res
wire v
Filter:
Append Insert Replace
Signals
Time
res
clk
r
g
v
r1
g1
v1
fls
dis
out[9:0]
out[9]
out[8]
out[7]
out[6]
out[5]
out[4]
out[3]
out[2]
out[1]
out[0]
Waves
1000 sec
001