Quantum Circuit Compilation for Trapped-Ion Processors with the Drive-Through Architecture

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Introduction: Quantum Computing and Trapped-Ion Processors

- Quantum computing exploits superposition and entanglement.
- Trapped-ion systems are one of the leading hardware platforms.
- Ions are confined in traps and manipulated with lasers.
- High-fidelity gates and long coherence times.

Introduction: Scalability Challenges

- Single ion chains slow down as they grow.
- Modular approach: QCCD architecture shuttles ions between traps.
- Ion shuttling introduces latency, heat, and error.

Motivation: Drive-Through Architecture

- Static qubits in traps, mobile communication qubits circulate on a racetrack.
- Reduces motional heating and re-cooling time.

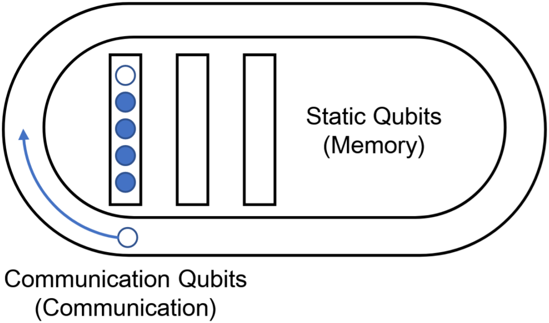


Figure: The "drive-through" architecture with static qubits in traps and communication qubits on the racetrack. Some qubits may be information-free (colored in white)

Limitations and Challenges

- Communication ions only connect to trap boundaries.
- Information must be swapped in and out.

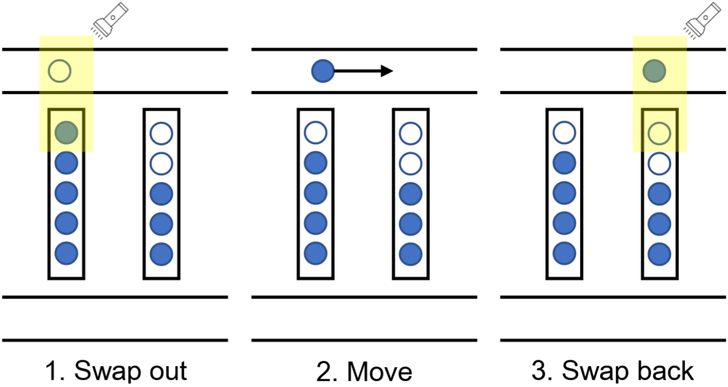


Figure: Methods for transporting the information of a static qubit to another trap.

Architecture graph

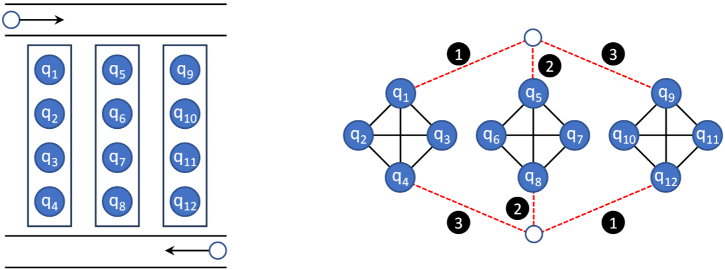


Figure: The drive-through architecture. Note that the communication edges in the drive-through architecture are available in specific orders.

- Circuit $\rightarrow$ DAG $\rightarrow$ Gate partitioning $\rightarrow$ Qubit placement.
- Layer-wise processing with look-ahead.
- Optimize placement for fidelity and transport cost.

Gate Partitioning

- Cluster qubits per layer using min-cut.
- Look-ahead mechanism for future gates. Adaptive window depth.

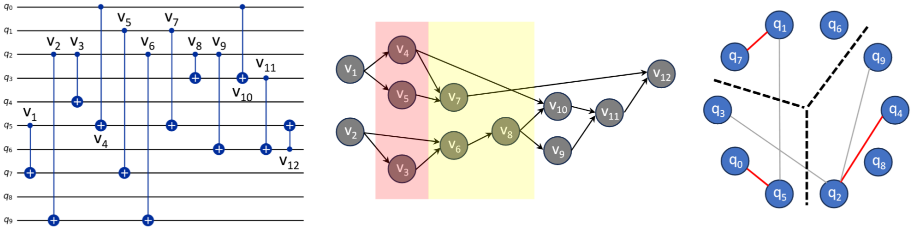


Figure: An illustration of circuit DAG generation and the gate partitioning at $\ell = 1$

Dynamic Qubit Placement

- Simulated annealing to minimize placement cost.
- Cost = Gate distance + 3*Swap penalty + Pull force.

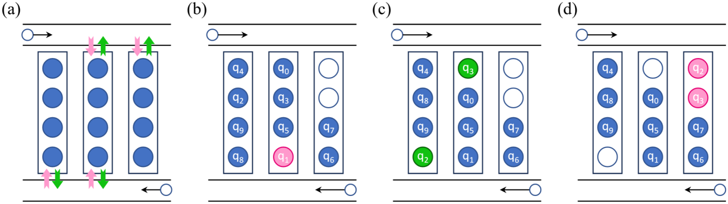


Figure: An illustration of layer-wise placement

Distance function

- The gate distance measures how far apart the qubits involved in two-qubit gates are within a trap.

$$\mathrm{gd}(\pi_{\ell,j}) = \sum_{q_m,q_n \in P_{\ell,j},(q_m,q_n)\in V_{G_\ell}} |\pi_{\ell,j}(q_m) - \pi_{\ell,j}(q_n)|$$

- The swap distance measures the number of swaps needed to transform the initial configuration $\pi_{\ell,j,0}$ to the optimized configuration $\pi_{\ell,j}$.

$$\mathrm{sd}(\pi_{\ell,j}, \pi_{\ell,j,0}) = \frac{1}{2}\sum_{i} |\pi_{\ell,j,0}(i) - \pi_{\ell,j}(i)|$$

- The boundary leaving cost.

Benchmark Circuits

- Evaluated on QNN, QAOA, QFT, Quantum Volume, Random circuits.
- Compared against SABRE and t$|$ket$\rangle$.

Reduced Inter-Trap Communication

- Example: Random circuit
- SABRE-ext: 10118 moves $\rightarrowtail$ 5979 moves.
- 40% reduction.

Circuit	#Qubit	#Gate	Depth	#Trap	#Inter-trap transport SABRE-ext	tlket⟩-ext	Ours
QNN	51	392	140	2	44	18	**6**
KNN	67	264	168	3	70	46	**21**
Adder 64	64	455	180	3	118	78	**26**
QFT 63	63	3400	245	3	558	286	**100**
Multiplier	75	6510	3555	3	1254	1578	**406**
QV	40	6000	300	2	1110	856	**614**
Supremacy	80	8500	421	3	1352	1912	**1037**
QAOA	80	7900	277	3	906	630	**397**
Random M	100	3000	189	4	2988	2790	**1735**
Random L	100	10000	319	4	10118	9492	**5979**

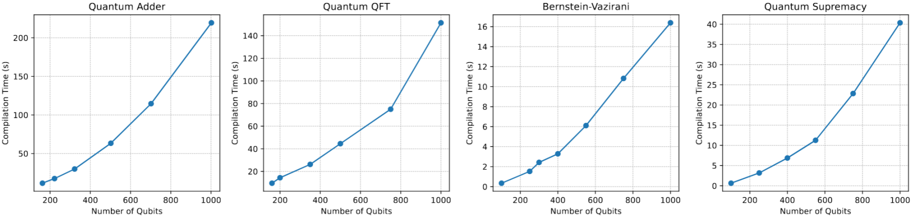
Fidelity Improvements

- Drive-through-aware compiler improves fidelity.
- Fewer ion swaps, reduced gate distance.

Circuit	SABRE-ext		t|ket⟩-ext		Ours	
	$TD(GD, SD)$	Fidelity	$TD(GD, SD)$	Fidelity	$TD(GD, SD)$	Fidelity
QNN	5537 (4100, 479)	0.9648	3400 (3066, 167)	0.9678	3233 (2795, 146)	**0.9681**
KNN	4142 (2678, 488)	0.9630	4050 (3004, 523)	0.9673	2450 (1787, 221)	**0.9677**
Adder 64	7022 (4442, 860)	0.9411	6662 (4942, 860)	0.9459	4712 (3068, 548)	**0.9488**
QFT 63	66347 (43334, 7671)	0.6633	51136 (42400, 4368)	0.6813	49541 (43031, 2170)	**0.6871**
Multiplier	101682 (63864, 12606)	0.3755	97295 (66909, 15193)	0.3619	74999 (55922, 6359)	**0.4057**
QV	129669 (69285, 20128)	0.6377	106472 (68586, 18943)	0.6480	84353 (50720, 11211)	**0.6508**
Supremacy	130018 (83038, 15660)	0.2629	128331 (71809, 28261)	0.2421	71928 (56079, 5283)	**0.2781**
QAOA	77124 (73620, 1168)	0.3090	47039 (35627, 5706)	0.3331	17317 (15940, 459)	**0.3515**
Random M	175641 (33933, 47236)	0.3491	137226 (36996, 50115)	0.3607	105203 (32123, 24360)	**0.4168**
Random L	599695 (112540, 162385)	0.0300	463461 (123489, 169986)	0.0322	367787 (107621, 86722)	**0.0504**
Avg. Ratio	1.4379 (2.2872, 1.7464)	0.9019	1.3345 (2.4926, 1.4190)	0.9125	1.0000 (1.0000, 1.0000)	1.0000

Scalability and Efficiency

- Handles 100+ qubit circuits with thousands of gates.
- Quadratic scaling with circuit size.



Conclusion

- Drive-through architecture enables low-overhead communication.
- Compiler maps circuits with higher fidelity and lower transport cost.