IEEE TCAD BBI ARTICLE

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***Abstract*—This is the abstract.**
Orange text is for undecided wording/words.
Red text is for important messages.
Cyan text is for future bib references to add.

***Index Terms*—Article submission, IEEE, IEEEtran, journal, LaTeX, paper, template, typesetting.**

I. Introduction

SEVERAL researches have studied Body Biasing Injection (BBI) in the past few years. While this injection method had been paused/forgotten for a few years, it has recently regained some interest. Among the latest studies, a modeling and simulation flow has been proposed, alongside better platforms allowing to achieve greater reproducibility and a deeper analysis of the mechanisms at works in digital integrated circuits subjected to BBI. In addition to that

II. Body biasing injection platforms modeling

THIS section approaches the electrical modeling of BBI platforms and integrated circuits. As it has been proposed in Cosade2022Chancel, FDTC2022&2023Chancel, it is possible to model BBI ICs using transistor-less models. It has the advantage of providing a somewhat precise evaluation of the mechanisms at work, while allowing for large simulations in reasonable times. Within this context, we decided

III. Logic path under BBI

For the purpose of analyzing the effects og BBI on actual logic, this section is dedicated in modeling and simulating a more complex logic path, integrating one or more sequential elements. This implies the use of a clock, governing these elements. The considered logic path is constituted of inverters, a buffer, and a D Flip-Flop (DFF). The detailed electrical schematics of each component are described in Fig. III, and III.

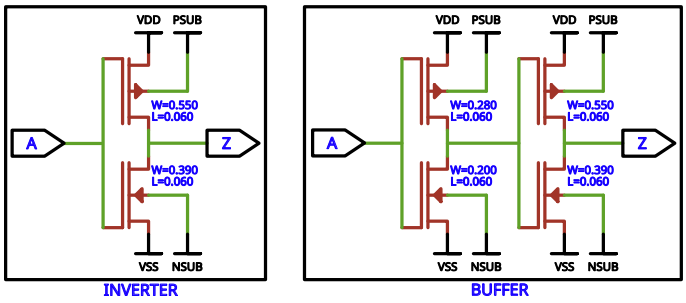

Fig. 1. IVX MOS SCH A-T-ON LE DROIT DE METTRE CE SCHÉMA ?

The study is conducted in two scenarios:

- When the logic path is static;

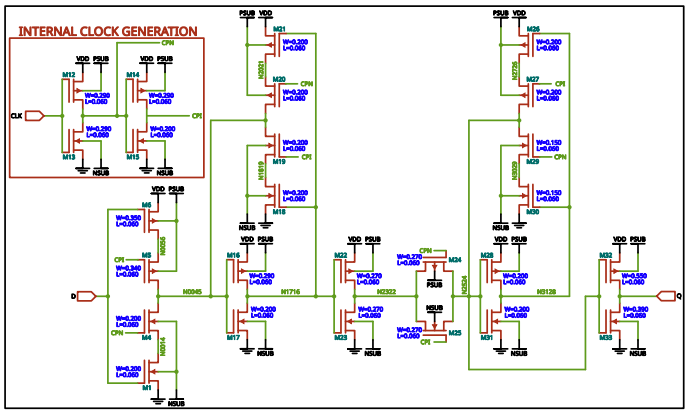

Fig. 2. DFF MOS SCH A-T-ON LE DROIT DE METTRE CE SCHÉMA ?

- When the logic path is dynamic.

The inverters model an arbitrary combinatorial logic path tackling the input of a DFF, used to sample the logic path output. The DFF clock is buffered to achieve an isolation from the ideal voltage source. Then, the DFF output is injected into a final 4-IVX chain, loaded with a 5 pF capacitor. The resulting schematic is described in Fig. III.

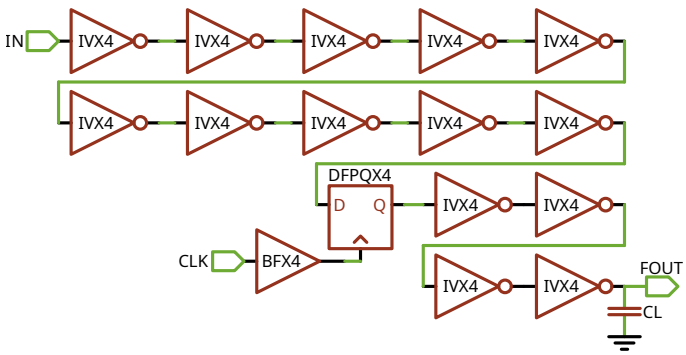

Fig. 3. DFFCHAIN

IV. Body biasing injection platforms overhaul

THIS second section is dedicated in analyzing the various improvements we set up to enhance BBI reproducibility. In the first place, we are going to analyze the various platforms proposed in the state-of-the art, then confront them to the proposed platform.

V. Conclusion