

IEEE TCAD BBI ARTICLE (MAX 14 PAGES)

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Abstract—This is the abstract.

Orange text is for undecided wording/words.

Red text is for important messages.

Cyan text is for future bib references to add.

Index Terms—Article submission, IEEE, IEEETran, journal, L^AT_EX, paper, template, typesetting.

I. INTRODUCTION

SEVERAL researches have studied Body Biasing Injection (BBI) in the past few years. While this injection method had been **paused/forgotten** for a few years, it has recently regained some interest. Among the latest studies, a modeling and simulation flow has been proposed, alongside better platforms allowing to achieve greater reproducibility and a deeper analysis of the mechanisms at works in digital integrated circuits subjected to BBI. In addition to that

II. BODY BIASING INJECTION PLATFORMS MODELING

THE objective of this first section is to present the work done concerning electrical modeling of integrated circuits in a BBI context. Developing IC models in that specific case is not an easy task. Indeed, modern digital ICs contains billions of transistors, and even considering microcontrollers where the transistor count is less important, with current technologies, it is impossible to evaluate circuits at a transistor level.

A. The hybrid simulation flow: introduction

To tackle these limitations, we decided to adopt an hybrid approach, combining transistor-less models and local logic gates simulations. This approach is a compromise between accuracy and computational cost/time, and allows simulating relatively big circuits under BBI disturbances.

The resulting simulation flow is divided in three consecutive steps:

- The simulation of an IC under BBI using a transistor-less model, allowing for a purely electrical analysis;
- The extraction of significant disturbed signals from the previous simulation;
- The simulation of functional logic gates under BBI thanks to the previously extracted signals.

The first step allows analyzing IC macro-electrical behavior when subject to BBI, and at a lower computational cost compared to a functional model including transistors and internal transmission lines, even if it could be done in a reasonable time constraint for millions of transistors. Then, by extracting useful signals such as the power delivery and the transistor substrate voltages, we can evaluate what would be the behavior of actual logic gates subject to BBI.

B. The hybrid simulation flow : building the models

The transistor-less model, also called standard-cell model, is developed thanks to the internal structure of integrated circuits, including:

- Their power supply network;
- Their standard-cells properties;
- Their silicon substrate.

These three elements and their internal structure allow elaborating average models, able to represent their macro behavior. Fig. II-B illustrates the base symbolic diagram used for our design. It represents a standard-cell segment, composed of logic gates and decoupling elements, with a fixed height of 5 μm and a variable width. For simplicity, two levels of metals for the power distribution are represented, the highest level MTOP in green and the first level M1 in blue.

Then, because the previous analysis does not consider the substrate on which the transistors lie, it is required to extend the model. To that end, we represent in Fig. II-B the cross-sectional view of a CMOS inverter in a triple-well and dual-well substrate. The parasitic silicon diodes formed between the substrate and the N-well, and between the N-well and the P-well are shown, in addition to the wells access electrical resistances R_C .

Thanks to these preliminary analysis and former work on the subject [mathieuEMFI, fdtc20222023](#), we set up an elementary transistor-less model, considering every presented aspect. This model, shown in Fig. II-B for a triple-well substrate, represents a column portion of an IC, being 30 μm wide, 5 μm deep, and t_{Sub} μm thick. The schematic is divided into 6 sections:

-  The substrate model, an array of equally distributed resistors;
-  The P-N substrate-well silicon junction;
-  The N-P well-well silicon junction;
-  The MOS average electrical model;
-  The substrate model, an array of equally distributed resistors;
-  The substrate model, an array of equally distributed resistors;

III. HYBRID SIMULATION RESULTS

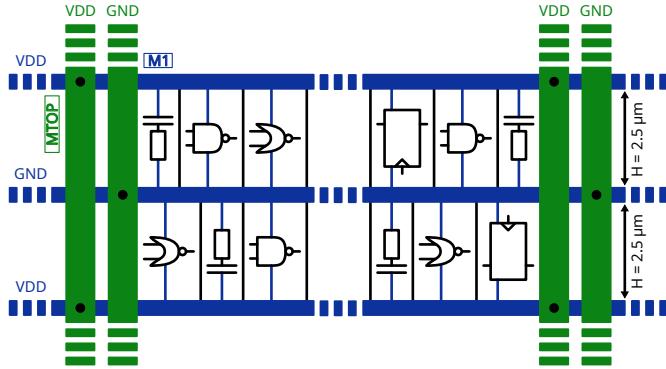


Fig. 1. A Standard-Cell Segment and its power delivery network.

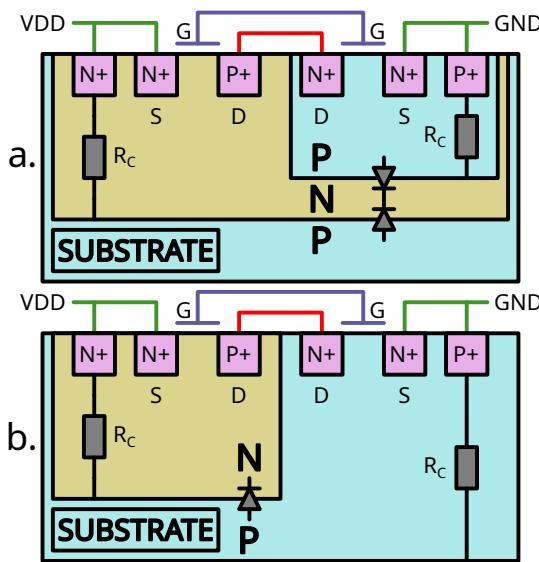


Fig. 2. Triple-well (a.) and Dual-well (b.) inverter cross-sectional view.

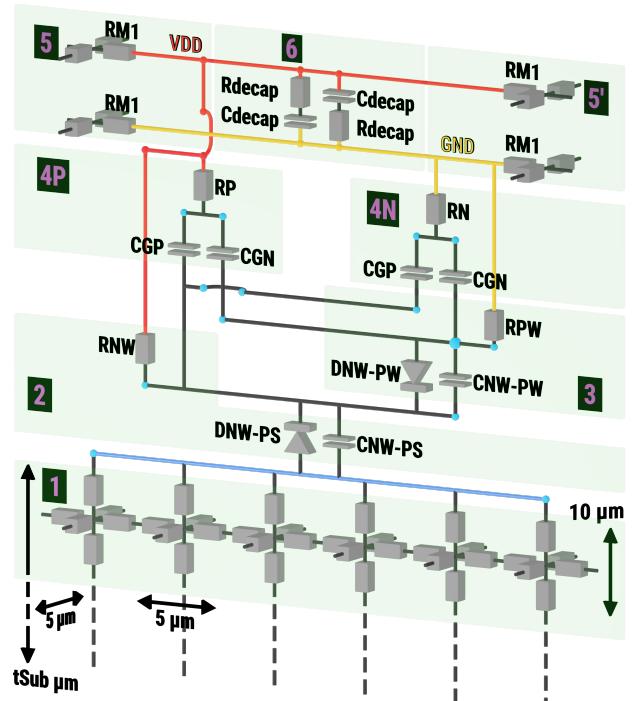


Fig. 3. Triple well std cell