IEEE TCAD BBI ARTICLE (MAX 14 PAGES)

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***Abstract*—This is the abstract.**
Orange text is for undecided wording/words.
Red text is for important messages.
Cyan text is for future bib references to add.

***Index Terms*—Article submission, IEEE, IEEEtran, journal, LaTeX, paper, template, typesetting.**

I. Introduction

SEVERAL researches have studied Body Biasing Injection (BBI) in the past few years. While this injection method had been paused/forgotten for a few years, it has recently regained some interest. Among the latest studies, a modeling and simulation flow has been proposed, alongside better platforms allowing to achieve greater reproducibility and a deeper analysis of the mechanisms at works in digital integrated circuits subjected to BBI. In addition to that

II. Body biasing injection platforms modeling

THE objective of this first section is to present the work done concerning electrical modeling of integrated circuits in a BBI context. Developing IC models in that specific case is not an easy task. Indeed, modern digital ICs contains billions of transistors, and even considering microcontrollers where the transistor count is less important, with current technologies, it is impossible to evaluate circuits at a transistor level.

Therefore, and as it has been proposed in FDTC2022 and FDTC2023, we approach the problem using transistor-less models. These are developed thanks to the internal structure of integrated circuits, including:

- The power supply network;
- The standard-cells;
- The silicon substrate.

These three elements, and their internal structure, allow to elaborate average models able to represent their macro behavior. Fig. II illustrates the base symbolic diagram used for our design. It represents a standard-cell segment, composed of logic gates and decoupling elements, with a fixed height of 5 µm and a variable width.

III. Logic path under BBI

For the purpose of analyzing the effects og BBI on actual logic, this section is dedicated in modeling and simulating a more complex logic path, integrating one or more sequential elements. This implies the use of a clock, governing these elements. The considered logic path is constituted of inverters, a buffer, and a D Flip-Flop (DFF). The detailed electrical schematics of each component are described in Fig. III, and III.

The study is conducted in two scenarios:

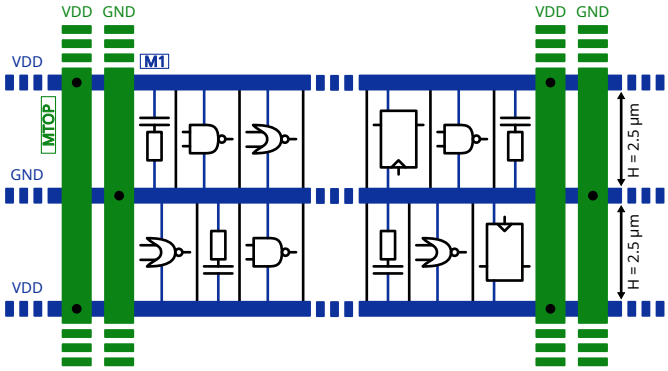

Fig. 1. A Standard-Cell Segment and its power delivery network.

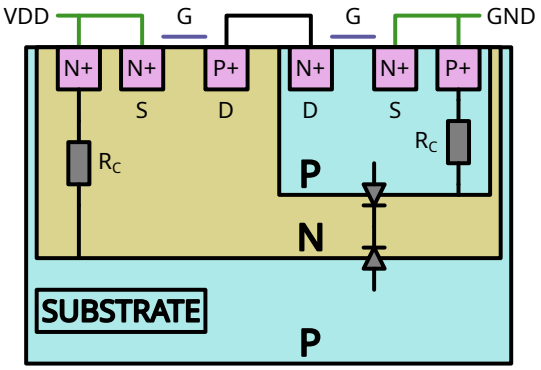

Fig. 2. Triple-well inverter cross-sectional view.

- When the logic path is static;
- When the logic path is dynamic.

The inverters model an arbitrary combinatorial logic path tackling the input of a DFF, used to sample the logic path output. The DFF clock is buffered to achieve an isolation from the ideal voltage source. Then, the DFF output is injected into a final 4-IVX chain, loaded with a 5 pF capacitor. The resulting schematic is described in Fig. III.

IV. Body biasing injection platforms overhaul

THIS second section is dedicated in analyzing the various improvements we set up to enhance BBI reproducibility. In the first place, we are going to analyze the various platforms proposed in the state-of-the art, then confront them to the proposed platform.

V. Conclusion

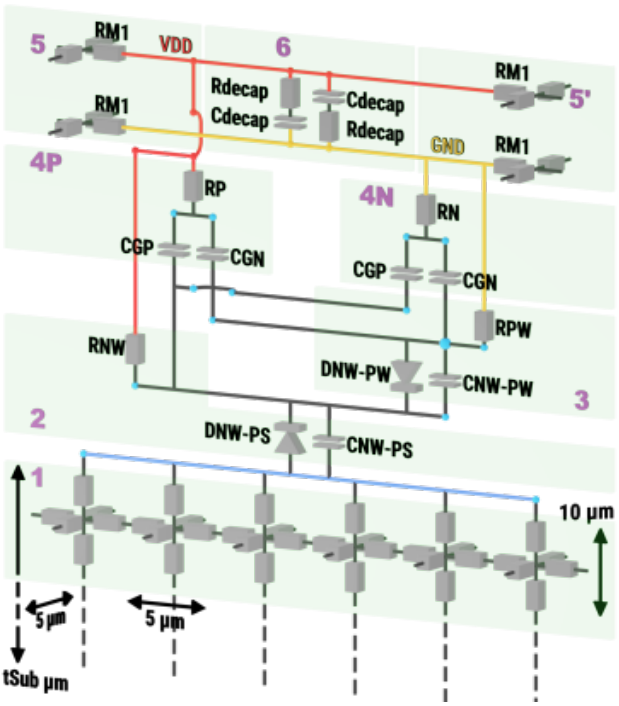

Fig. 3. Triple well std cell

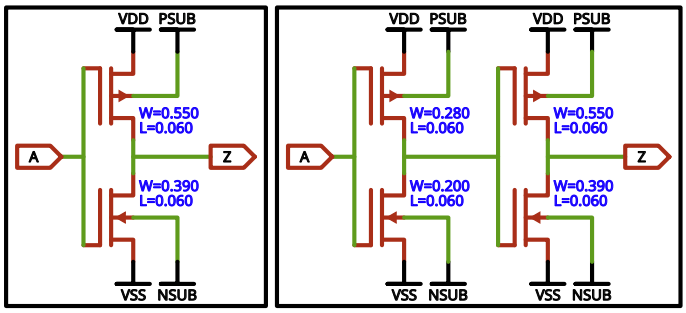

Fig. 4. IVX MOS SCH A-T-ON LE DROIT DE METTRE CE SCHÉMA ?

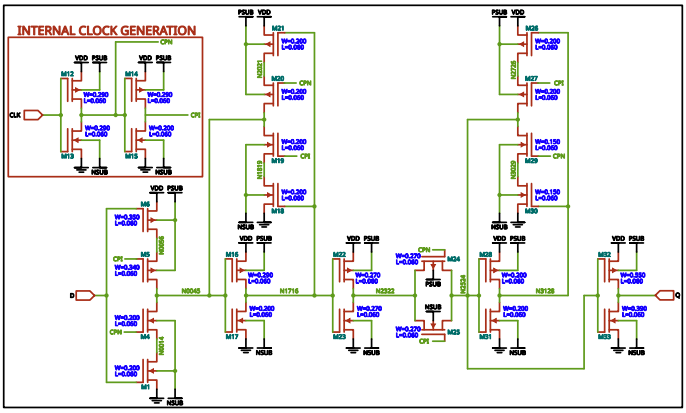

Fig. 5. DFF MOS SCH A-T-ON LE DROIT DE METTRE CE SCHÉMA ?

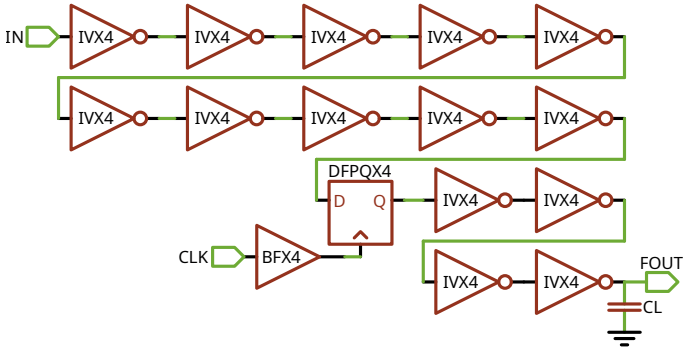

Fig. 6. DFFCHAIN