IEEE TCAD BBI ARTICLE (MAX 14 PAGES)

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***Abstract*—This is the abstract.**
Orange text is for undecided wording/words.
Red text is for important messages.
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***Index Terms*—Article submission, IEEE, IEEEtran, journal, LaTeX, paper, template, typesetting.**

I. Introduction

SEVERAL researches have studied Body Biasing Injection (BBI) in the past few years. While this injection method had been paused/forgotten for a few years, it has recently regained some interest. Among the latest studies, a modeling and simulation flow has been proposed, alongside better platforms allowing to achieve greater reproducibility and a deeper analysis of the mechanisms at works in digital integrated circuits subjected to BBI. In addition to that

II. Body biasing injection platforms modeling

THE objective of this first section is to present the work done concerning electrical modeling of integrated circuits in a BBI context. Developing IC models in that specific case is not an easy task. Indeed, modern digital ICs contains billions of transistors, and even considering microcontrollers where the transistor count is less important, with current technologies, it is impossible to evaluate circuits at a transistor level.

A. The hybrid simulation flow: introduction

To tackle these limitations, we decided to adopt an hybrid approach, combining transistor-less models and local logic gates simulations. This approach is a compromise between accuracy and computational cost/time, and allows simulating relatively big circuits under BBI disturbances.

The resulting simulation flow is divided in three consecutive steps:

- The simulation of an IC under BBI using a transistor-less model, allowing for a purely electrical analysis;
- The extraction of significant disturbed signals from the previous simulation;
- The simulation of functional logic gates under BBI thanks to the previously extracted signals.

The first step allows analyzing IC macro-electrical behavior when subject to BBI, and at a lower computational cost compared to a functional model including transistors and internal transmission lines, even if it could be done in a reasonable time constraint for millions of transistors. Then, by extracting useful signals such as the power delivery and the transistor substrate voltages, we can evaluate what would be the behavior of actual logic gates subject to BBI.

B. The hybrid simulation flow : building the models

Building these models requires a correct understanding on integrated circuits internal structures, such as:

- The power supply network, composed of various stacked metal wires;
- The standard-cells, made of logic gates, and thus transistors, being pre-characterized cells used as building blocks;
- The silicon substrate, which can be of various type depending on the technology.

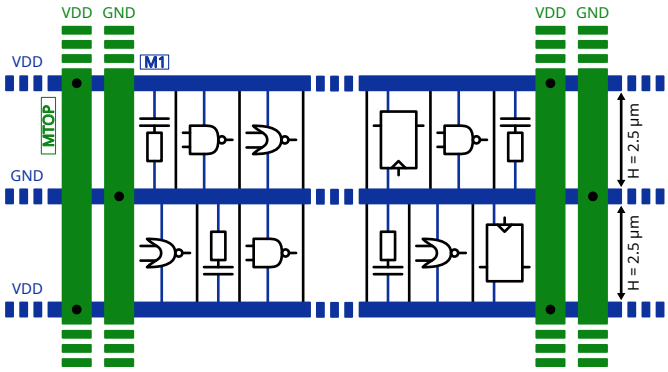

Fig. 1. A Standard-Cell Segment and its power delivery network.

1) Power supply rails and standard-cell segments: The power distribution inside an IC is typically made with a grid-like structure, composed of metal wires stacked on top of each other on planes. The uppermost layer forms a ring surrounding the core. In each layer, the metal wires are equally spaced and have a dedicated width, which becomes thinner the deeper they are. The lowest layer brings the power directly to the transistors.

Within these metal lines are located standard-cell segments (SCS), created by the power planning, as illustrated in Fig. 1. SCS are pre-characterized by foundries and classified according to their performance in timing and power consumption. Their height is fixed, while their width vary depending on their complexity, and are commonly made of logic gates, sequential, and decoupling elements.

2) Silicon substrate structure: Another important element of an IC is the substrate, and most importantly its type. We can mainly distinguish bulk and FD-SOI substrates.

On the one hand, in bulk substrates, the transistor channel forms directly inside the P-substrate, and the depletion layer thickness is difficult to control. On the other hand, in FD-SOI substrates, a silicon oxide layer is created between the channel and the P-substrate, thus constraining the channel thickness.

In this paper, we are focusing only on bulk substrates, and in this family, we can distinguish two substrate types:

dual-well (DW) and triple-well (TW). The main difference between DW and TW substrates lies in how are lithographed NMOS transistors. In DW substrates, NMOS are located directly inside the P-doped substrate, and PMOS inside a N-doped well, called the N-well. However, in the case of a TW substrate, the PMOS are still inside the N-well, but the NMOS are located inside an additional P-doped well, made inside the N-well.

These manufacturing differences are illustrated in Fig. 2, representing the cross-sectional view of an inverter made with a bulk technology. The PN and NP diodes formed between the substrate and the wells are represented, and the electrical resistances R_C represent the access resistance of the substrate and the wells.

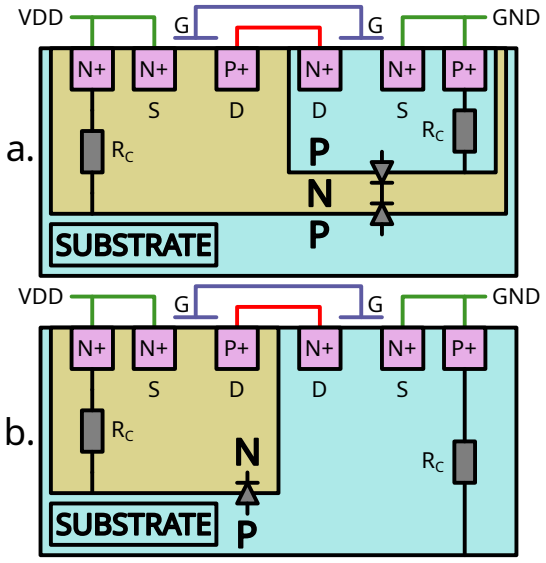

Fig. 2. Triple-well (a.) and Dual-well (b.) inverter cross-sectional view.

Dual-well substrates are found in moderately old ICs, while triple-well ones are common in more recent ICs, often coupled with dual-well substrate on the same die. The combination of both allows for cross-coupling noise reduction, in addition to electrical insulation between transistors located on different domains (DW and TW).

3) Designing an elementary building-block for mass simulation: Thanks to the previously analyzed elements and models, we can now design elementary standard-cell blocks composed of the power delivery, the logic gates and the substrate, for each substrate type. As it has been said before, we are developing an hybrid simulation flow, therefore the designed elementary block is transistor-less. Eventually, our work is based on previous works on the subject []mathieuEMFI, FDTC2022, FDTC2023].

The model we propose is shown in Fig. II-B3 both for a triple-well and a dual-well substrate. The models are extremely similar, but their difference is what is important. It represents an entire standard-cell segment, including a two levels power delivery network, average models of a hundred of logic gates, silicon junctions, and the silicon substrate. For better clarity, we divided the model into 6 sections, each representing a specific building block:

- 1 The substrate: modeled with 6 blocks of 6 resistors;
- 2 The P-N substrate-well silicon junction;
- 3 The N-P well-well silicon junction (TW), or the substrate access resistance (DW);
- 4N 4P The MOS average electrical model;
- 5 5' The power distribution metals;
- 6 The power supply decoupling.

The component values are calculated according to the target technology, in our case 90 nm, and are shown in Table I.

4) Effectively using these building-blocks: Because the SCS models we previously presented do not represent an entire IC, rather a column portion of one, it is needed, to use them, to replicate and interconnect them as much as needed to model an entire IC. All the models were written in the SPICE language, and simulated using HSPICE. Interconnecting each model instance was done using an automated script. It allowed us to reduce human errors by validating the generation process rather than the netlists themselves. Our generation script allows us to set the following parameters:

- The final IC size;
- The BBI probe size and location;
- The substrate thickness;
- The substrate type (TW or DW);
- The backside voltage pulse characteristics.

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5) Validating the generated circuits:

III. Hybrid simulation results

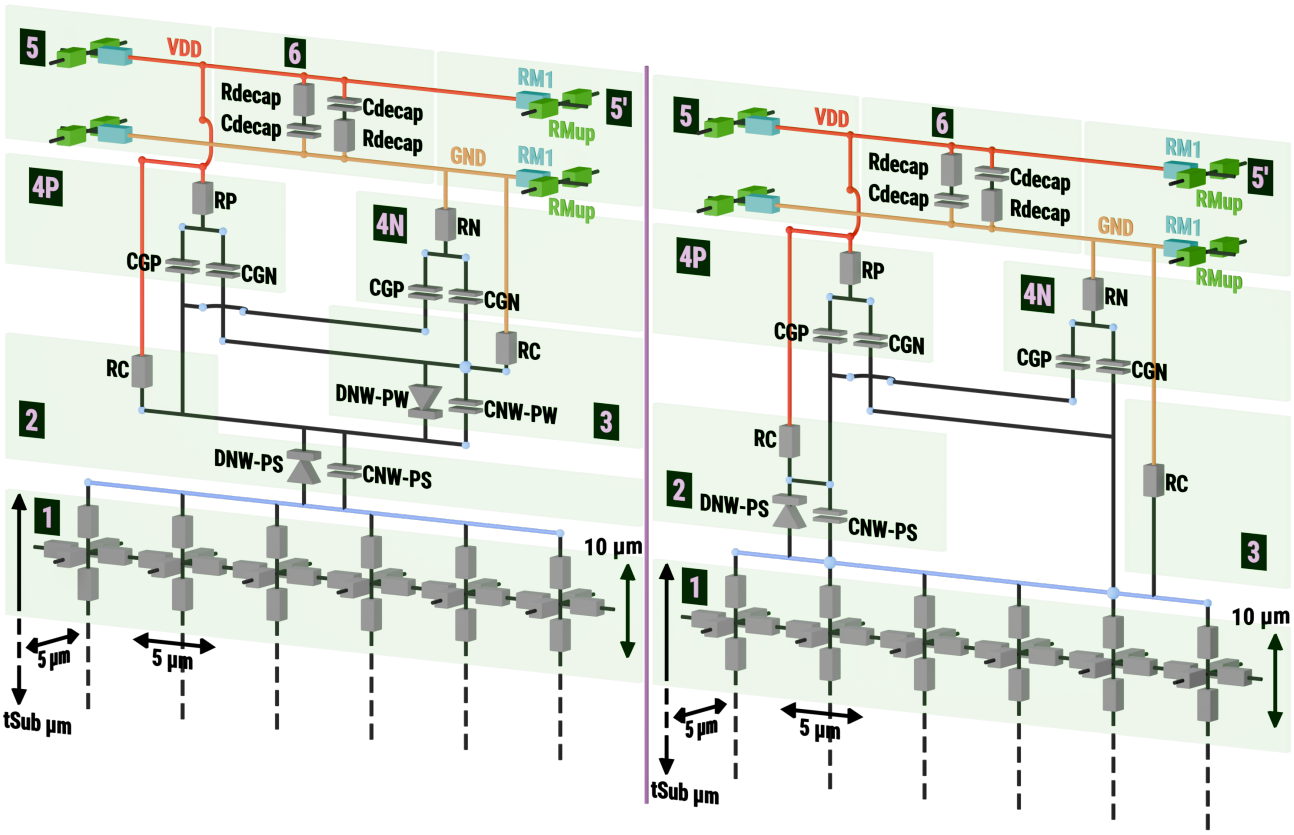

Fig. 3. Triple well (left) and dual well (right) std cell (PEUT ETRE FAIRE DES SOUS-FIGURES)

Component	Rmup	RM1	Cdecap	Rdecap	CGP	CGN	ρ_{SUB}	RP	RN	CNW	RC
Description	Metal top Resistance	Metal 1 Resistance	Power Decoupling Capacitance	Power Decoupling Resistance	Equivalent PMOS Gate capacitance	Equivalent NMOS Gate capacitance	Silicon Substrate Resistivity	PMOS Channel Resistance	NMOS Channel Resistance	Wells Diode Capacitance	Substrate/wells Access Resistance
Value	26 Ω	5 Ω	2.25 fF	2 Ω	35.2 fF	25.2 fF	0.01 Ω·m	9.57 Ω	5.3 Ω	20 fF	3.1 kΩ

TABLE I
STANDARD-CELL MODEL PASSIVE COMPONENT VALUES.