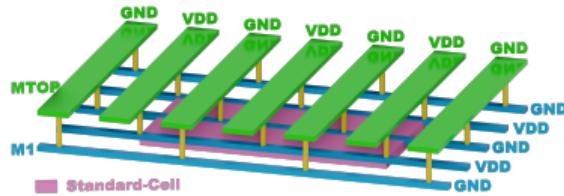
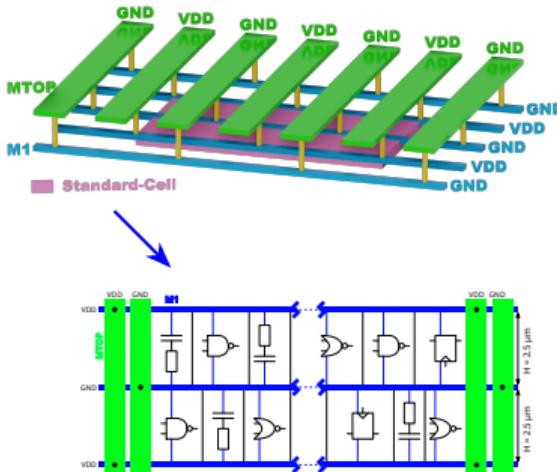


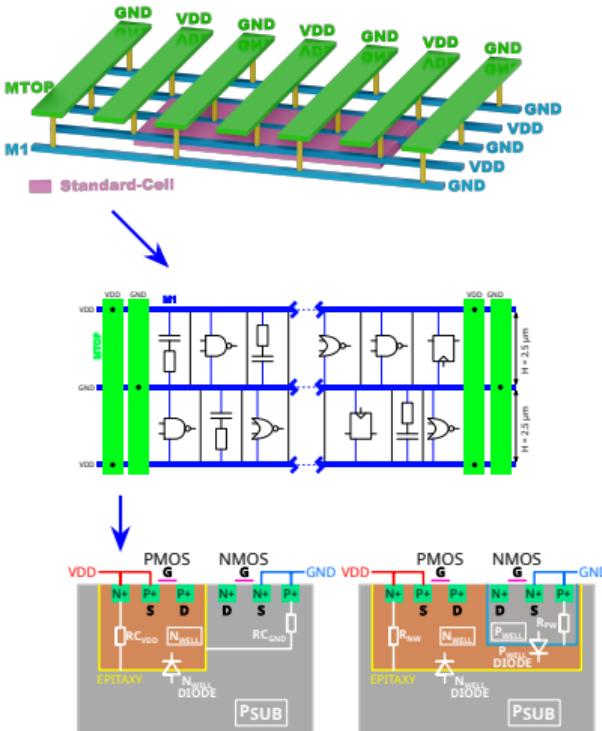
Simulation models



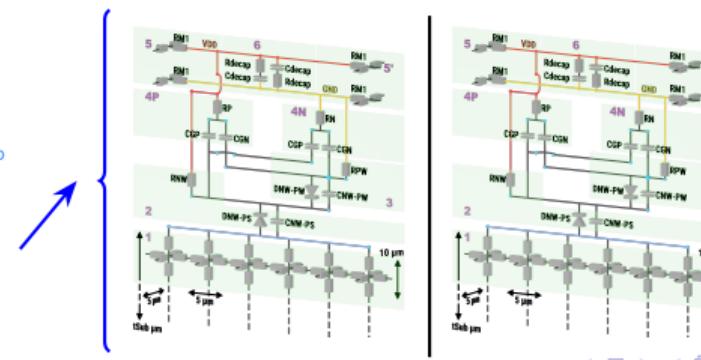
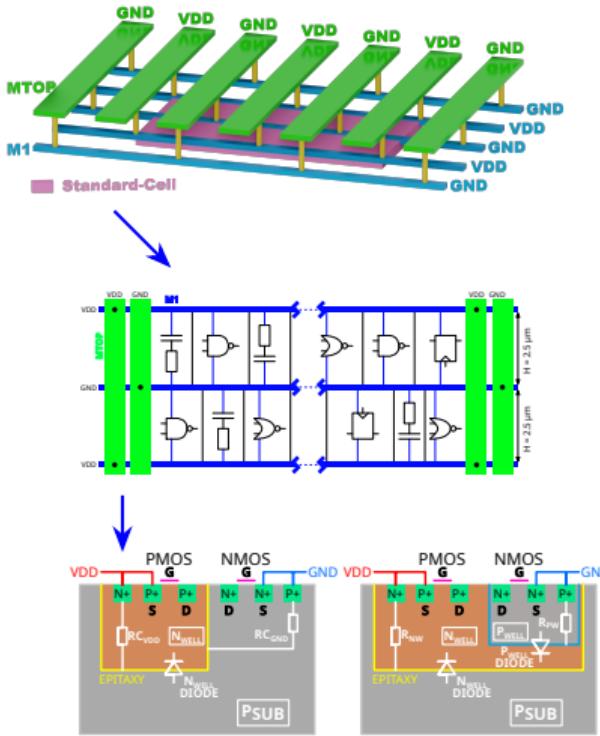
Simulation models



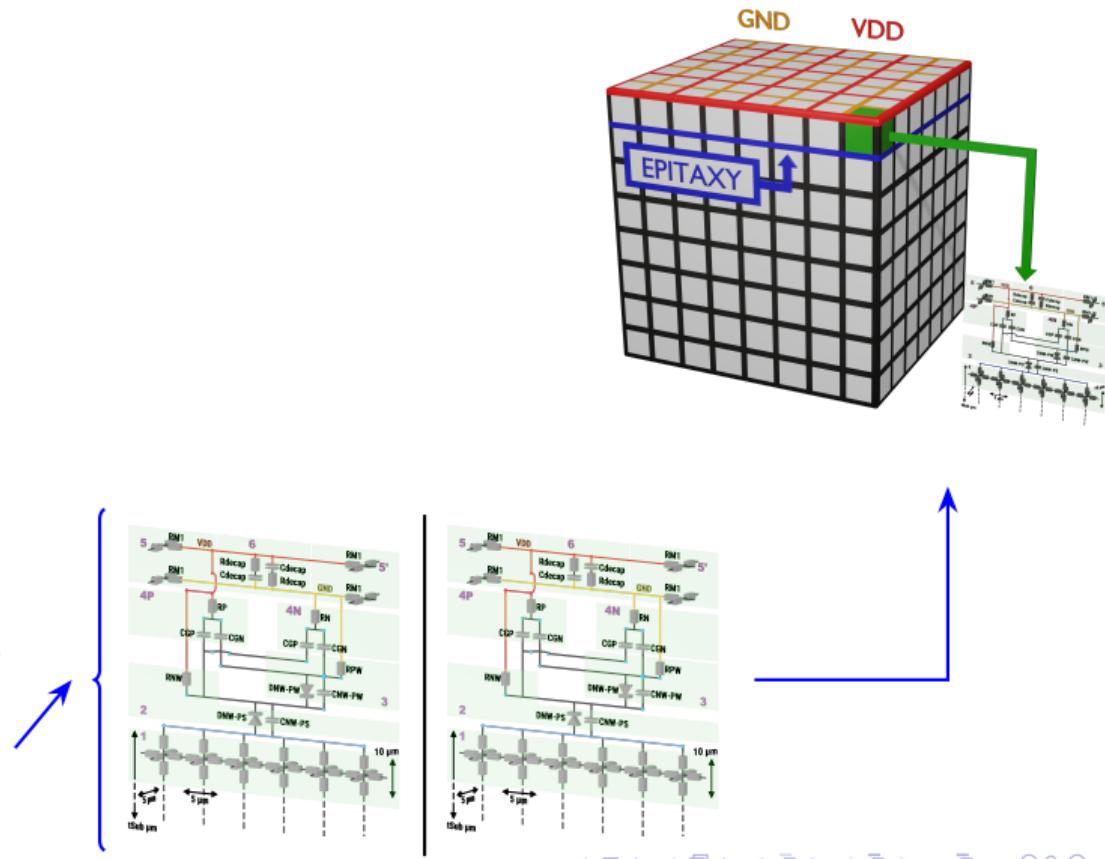
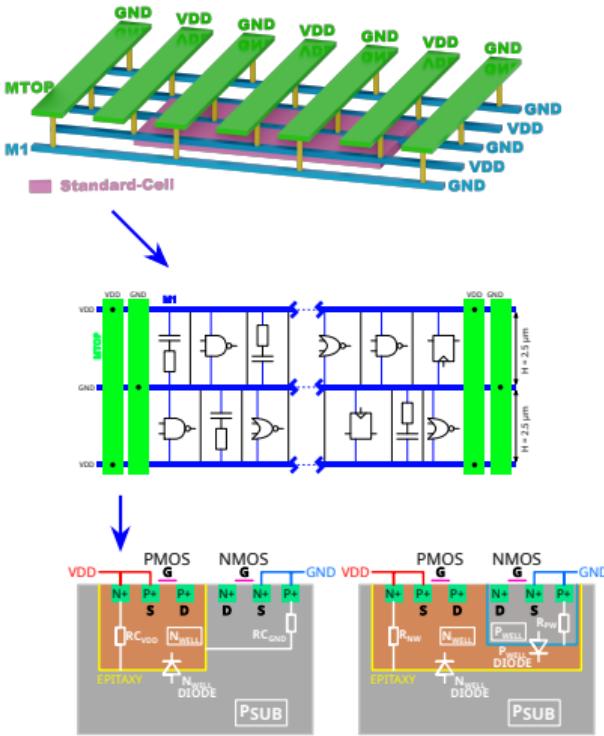
Simulation models



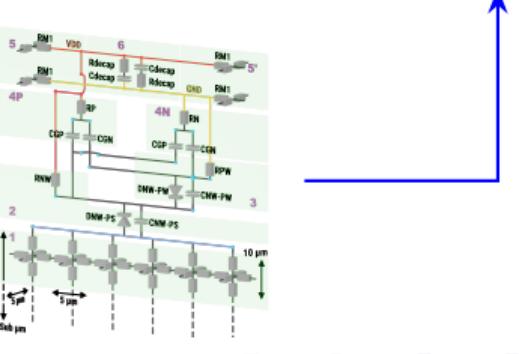
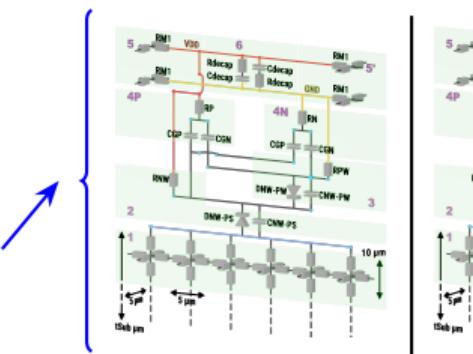
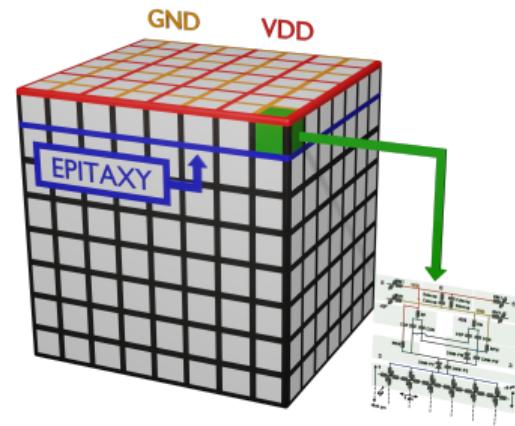
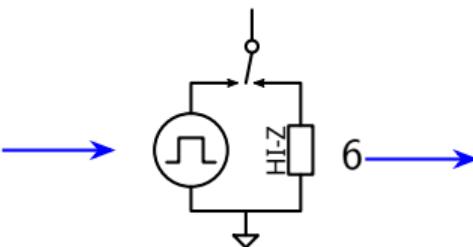
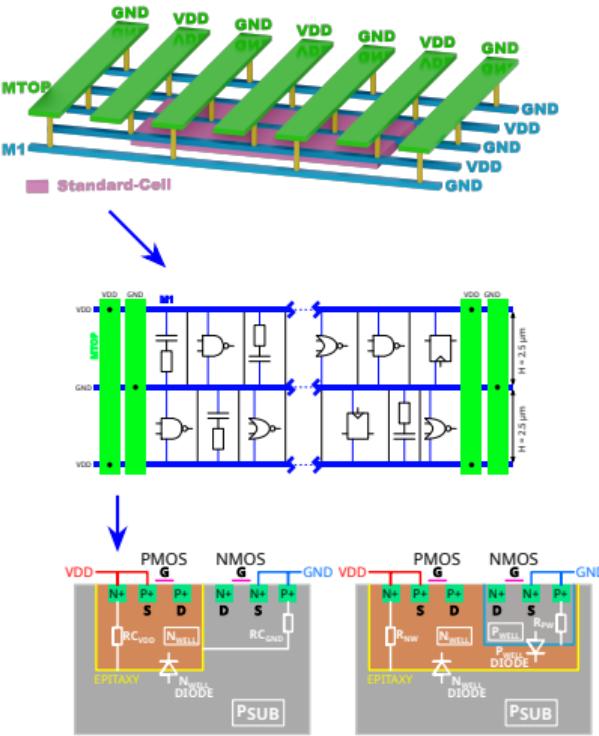
Simulation models



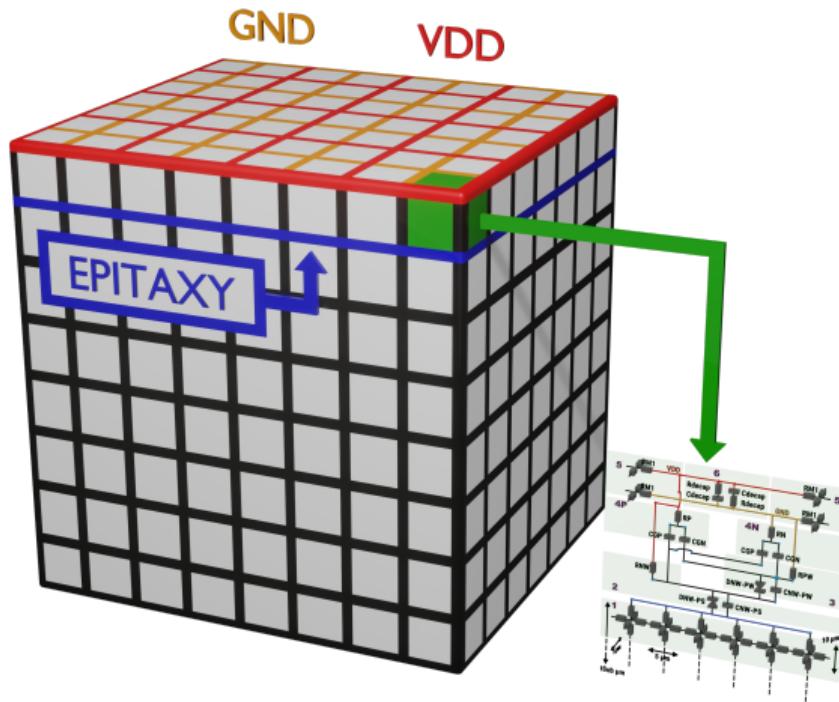
Simulation models



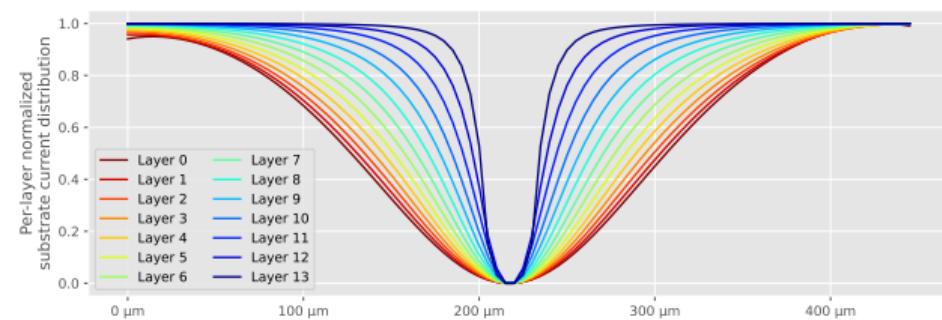
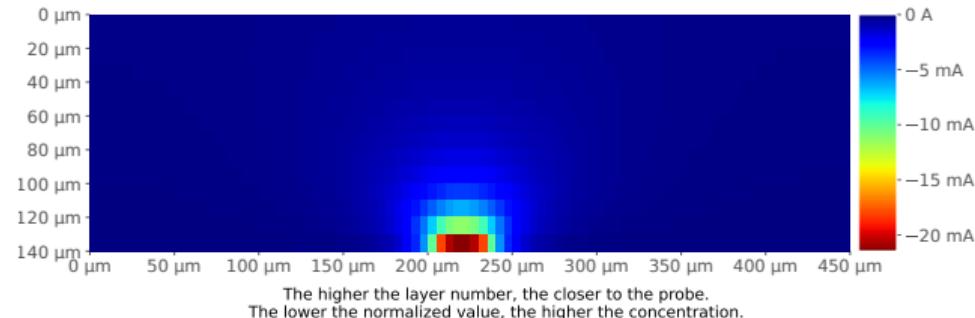
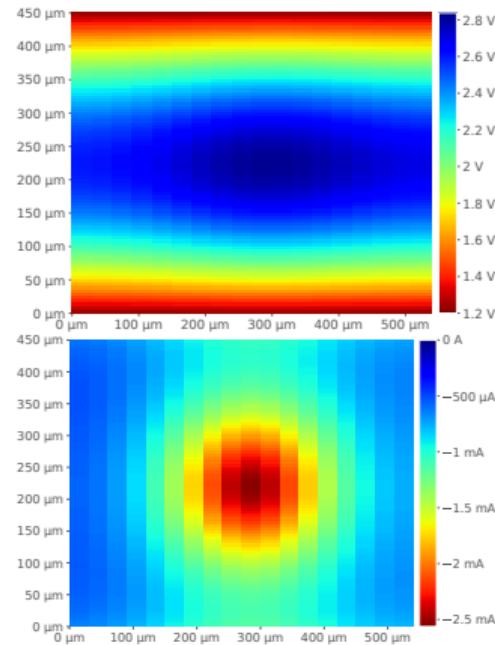
Simulation models



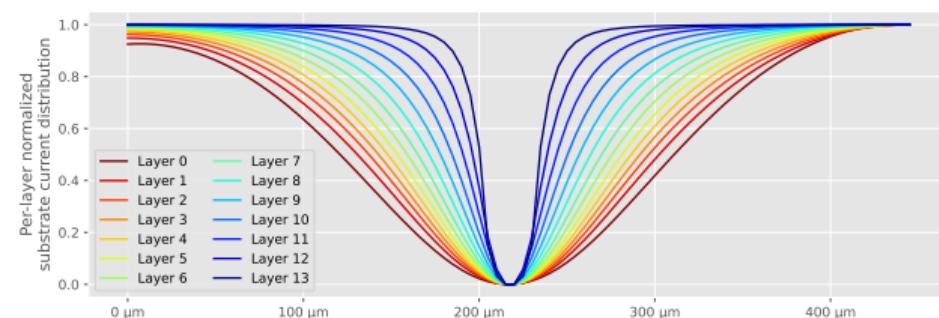
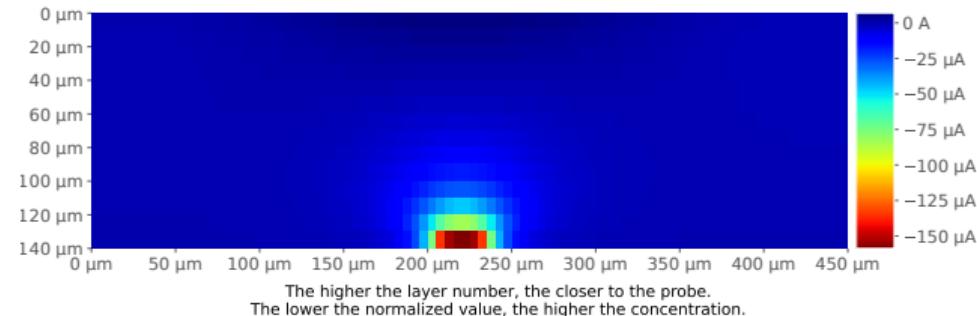
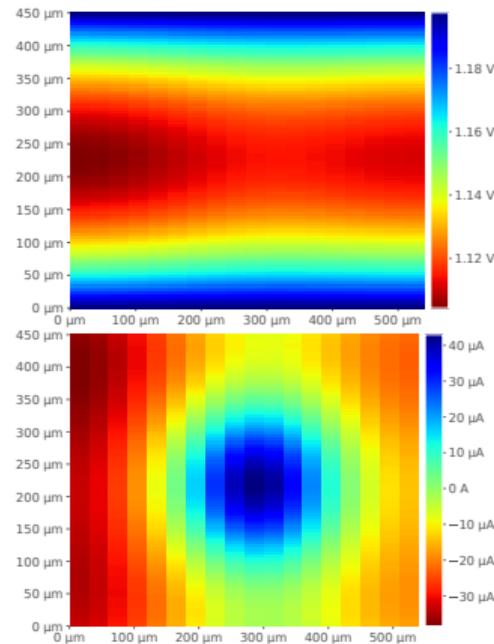
Simulation models



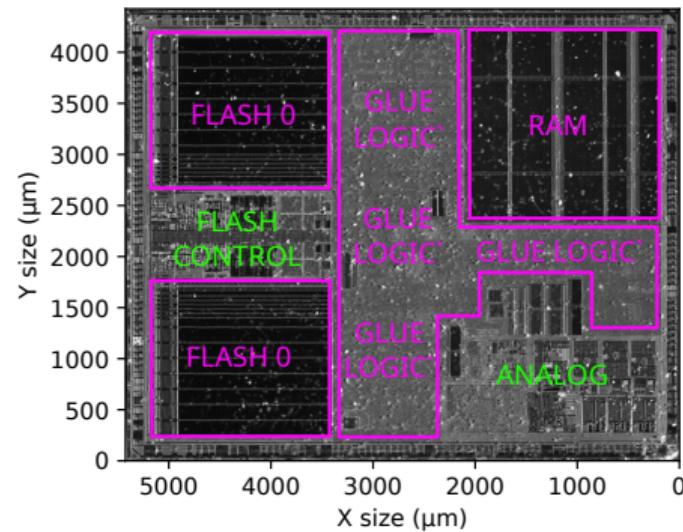
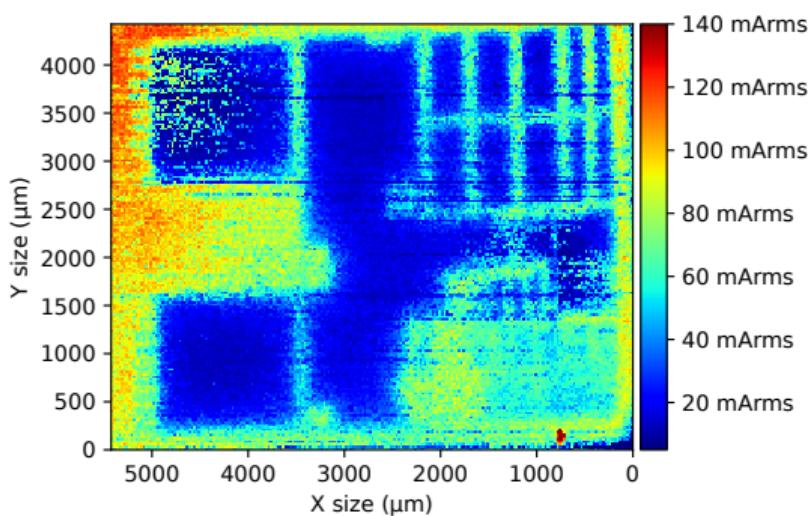
Simulation results: Dual-Well



Simulation results: Triple-Well



Dual-Well and Triple-well ICs in practice



SIMULATION FLOW FOLLOW-UP

Logic gates simulations under BBI: models

