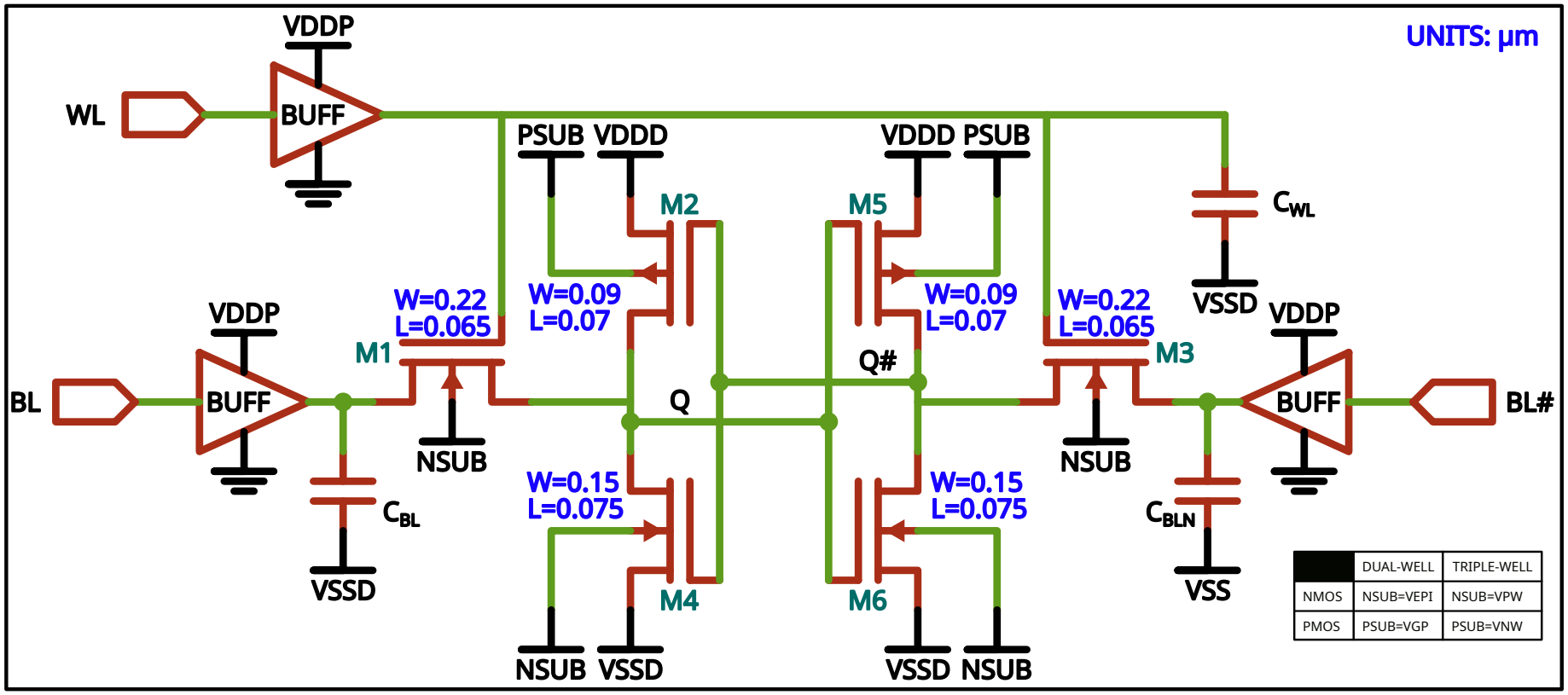
SRAM cells under BBI / IC thermal analysis

Geoffrey Chancel

2024/03/25

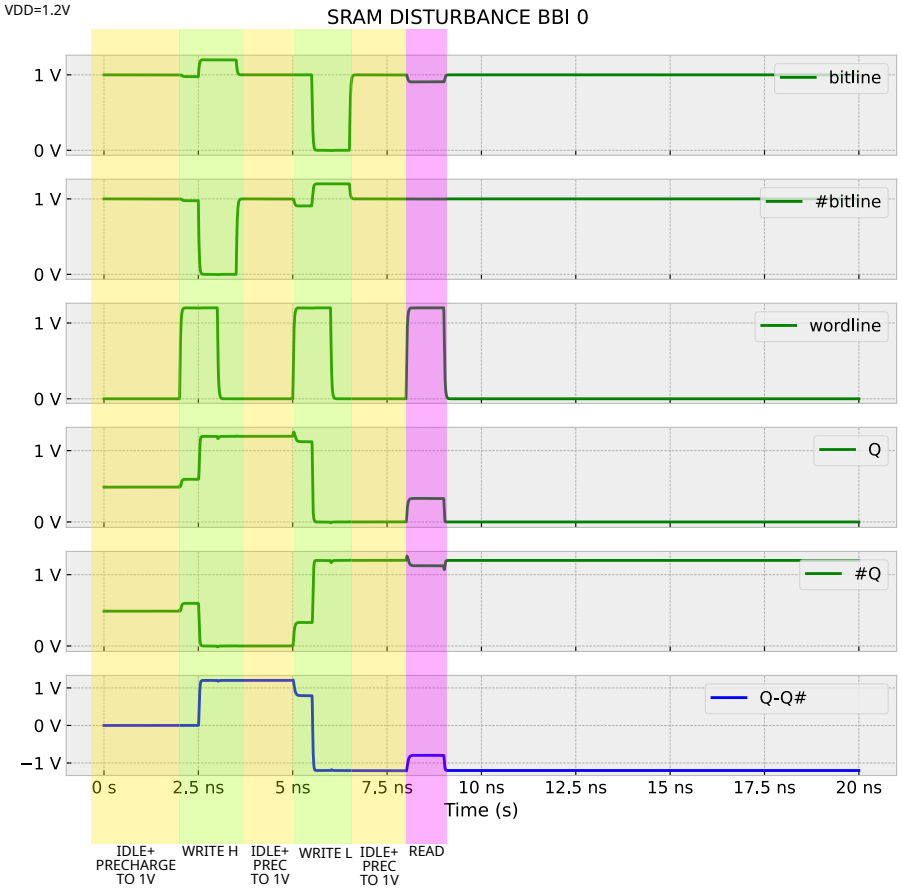
6T SRAM CELL CMOS_065

6T SRAM CELL CMOS_065 schematics

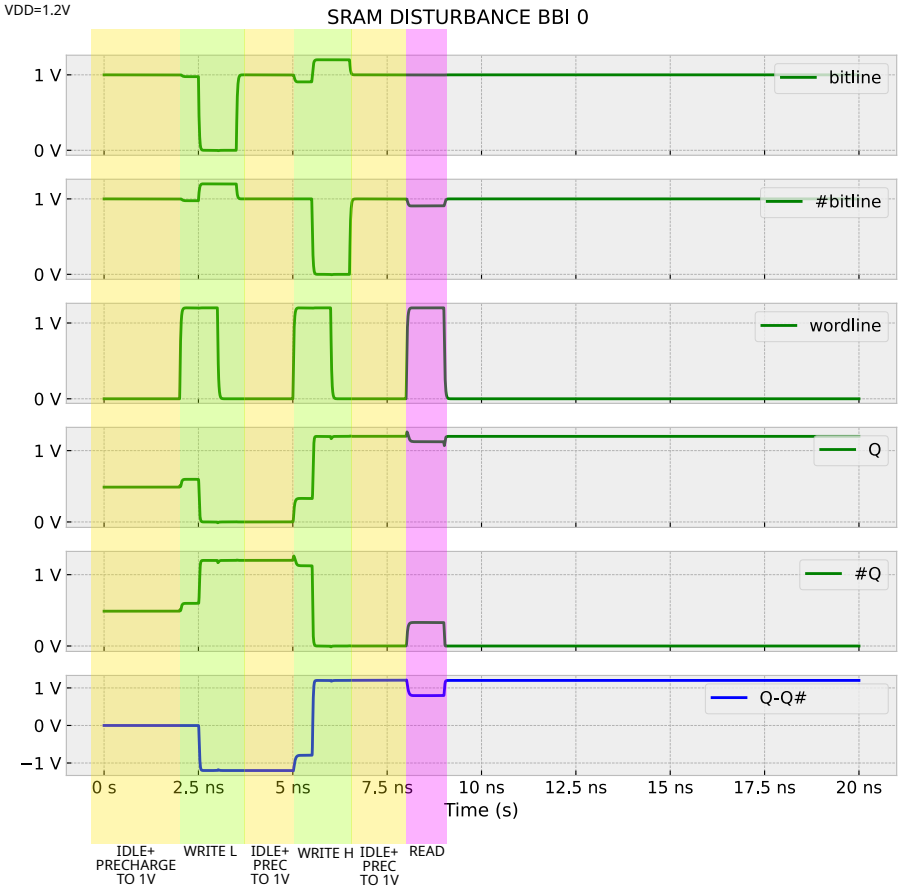


6T SRAM CELL CMOS_065 functioning signals

$(Q - \bar{Q})_{INIT} = L$

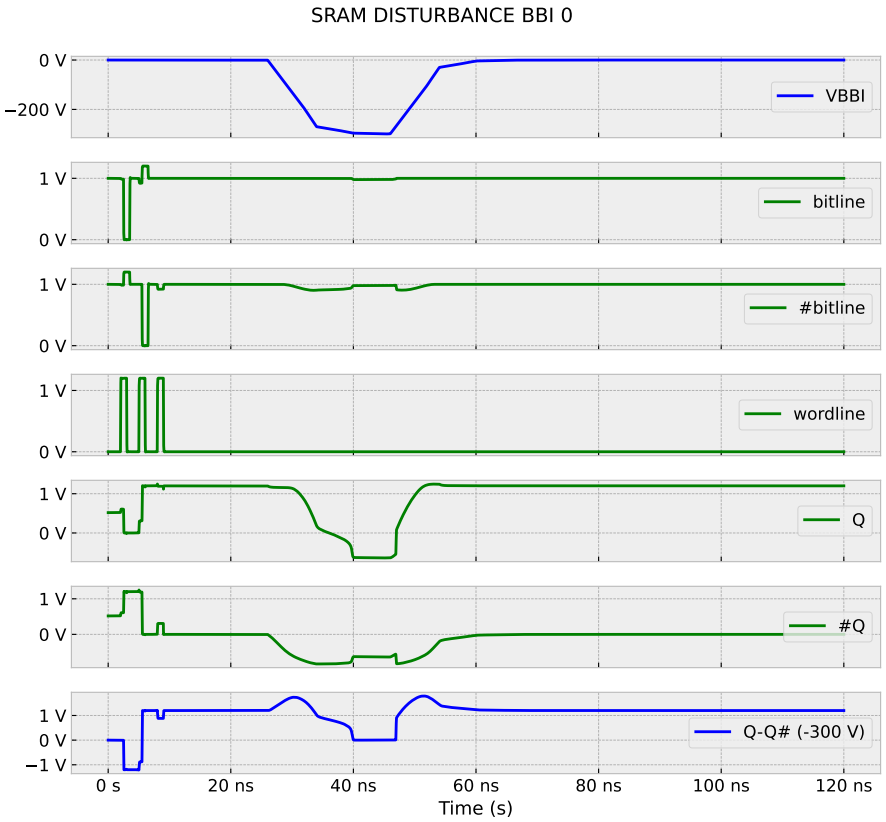


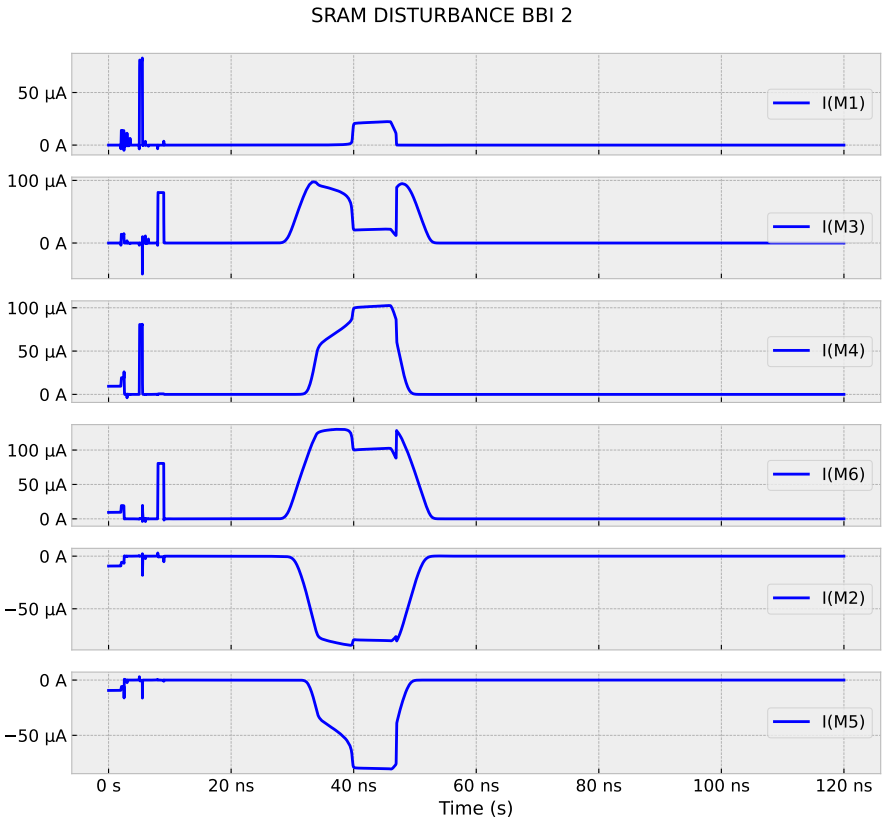
$(Q - \bar{Q})_{INIT} = H$



DUAL-WELL SUBSTRATE: OUT=H

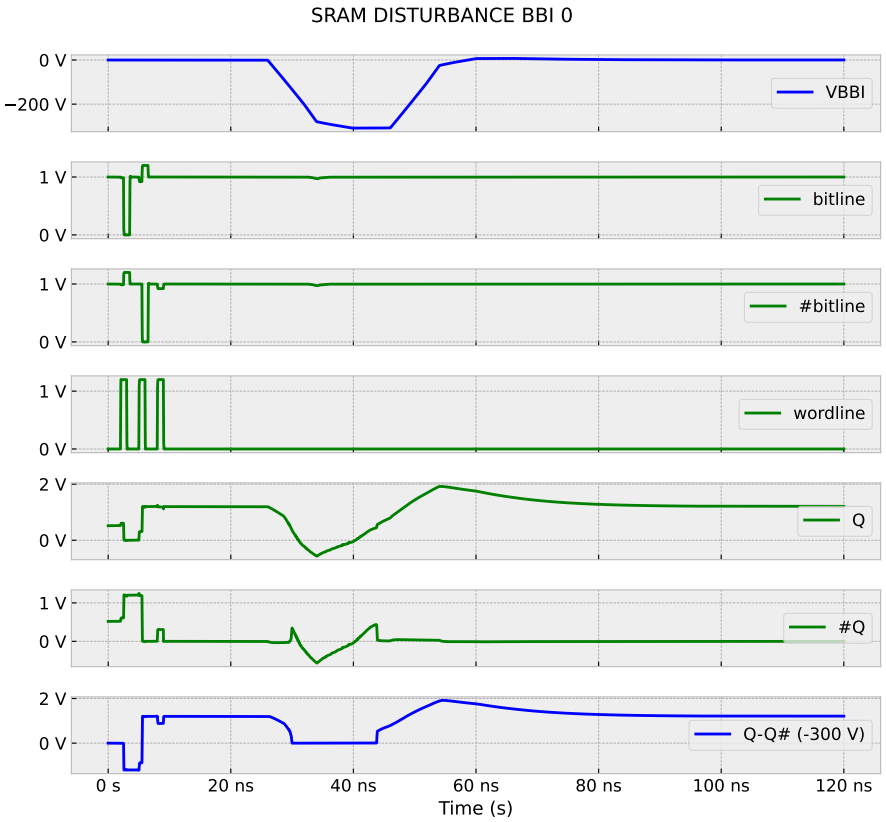
$$(Q - \bar{Q})_{INIT} = H$$

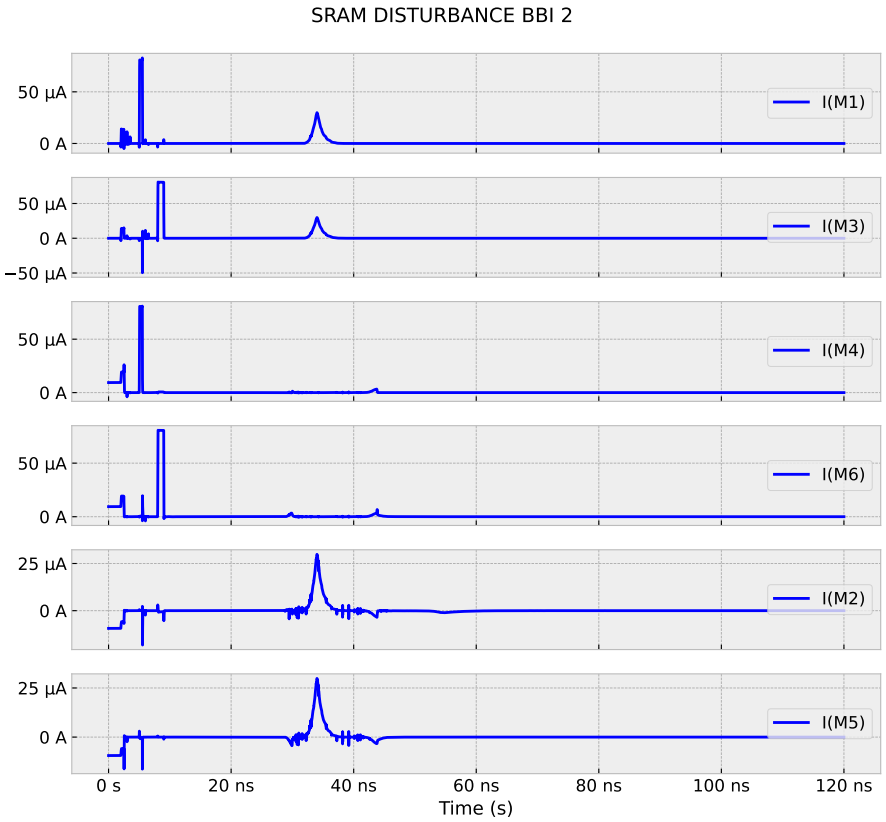




TRIPLE-WELL SUBSTRATE: OUT=H

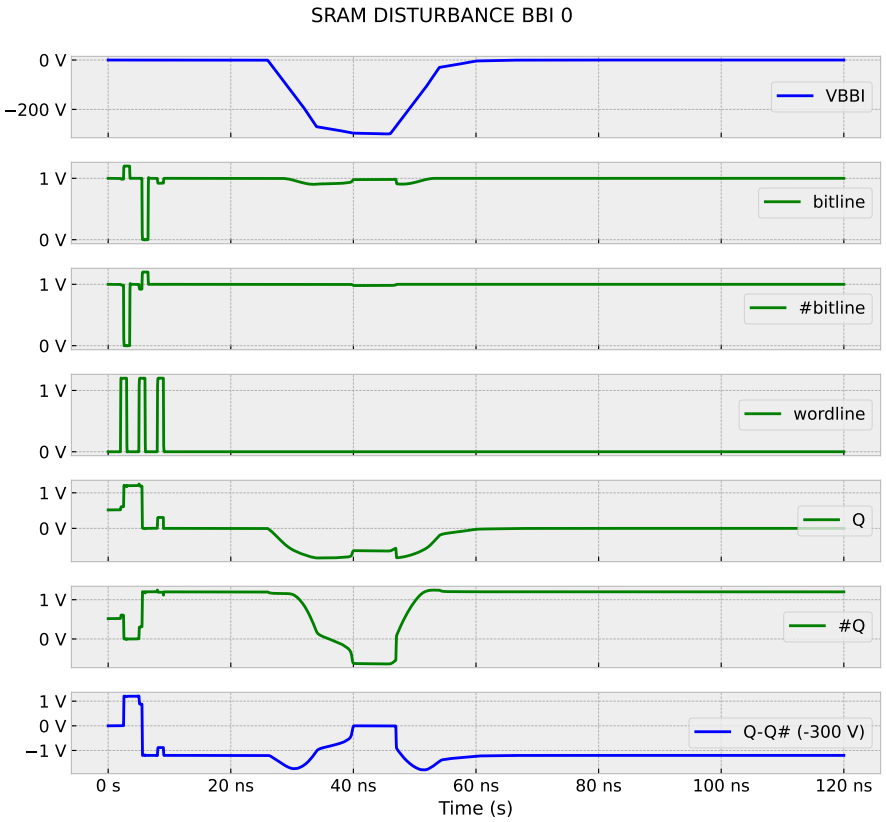
$$(Q - \bar{Q})_{INIT} = H$$

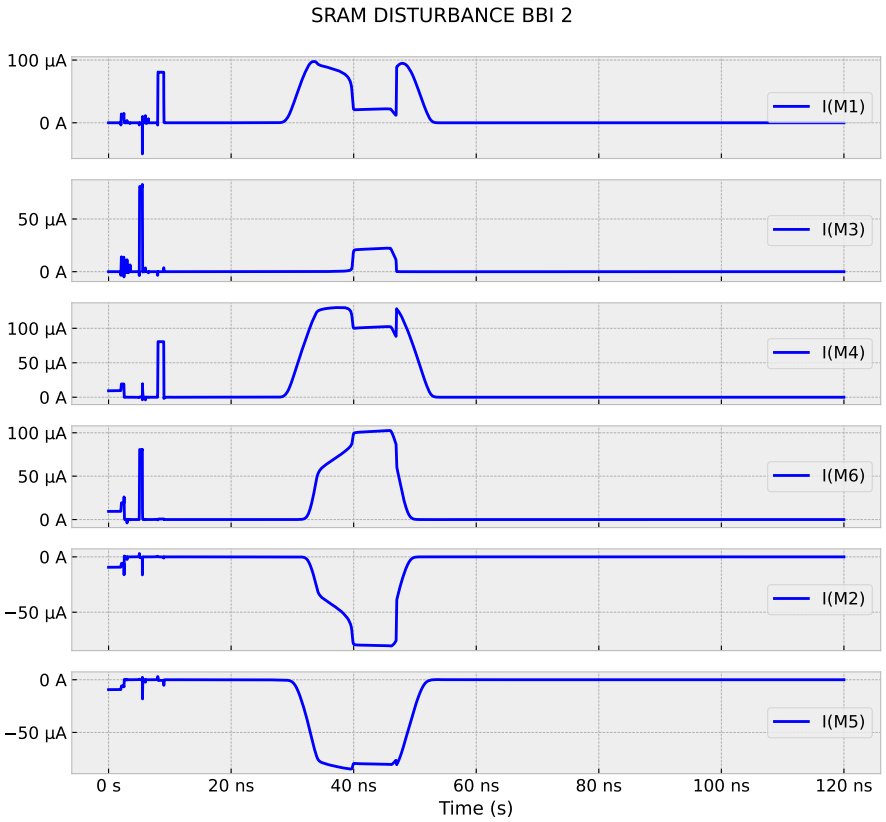




DUAL-WELL SUBSTRATE: OUT=L

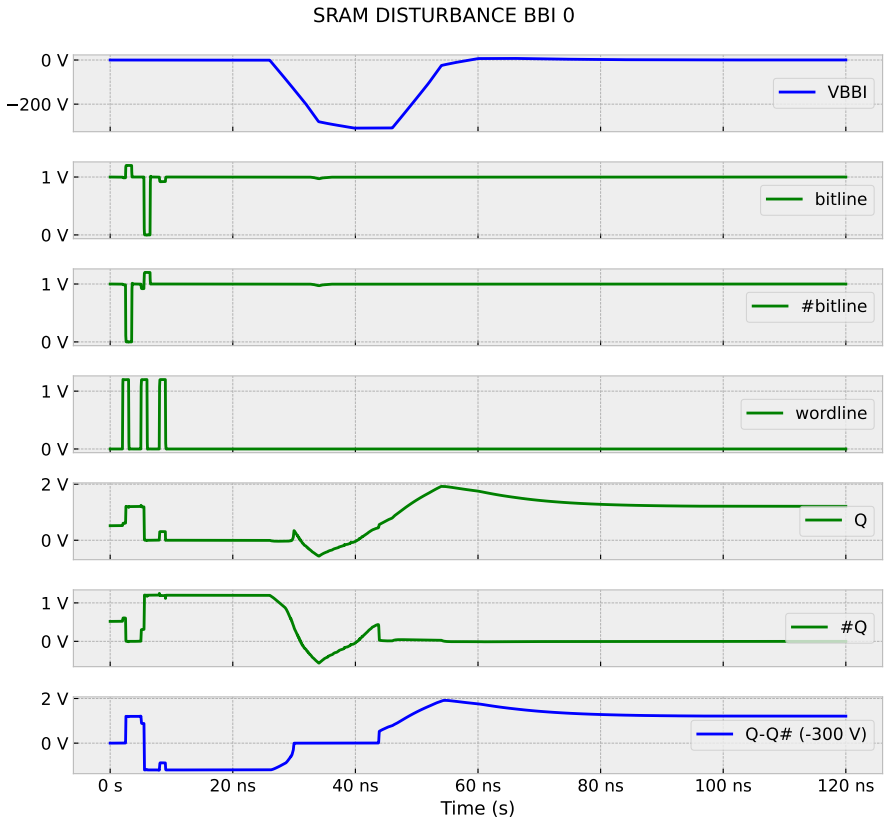
$$(Q - \bar{Q})_{INIT} = L$$

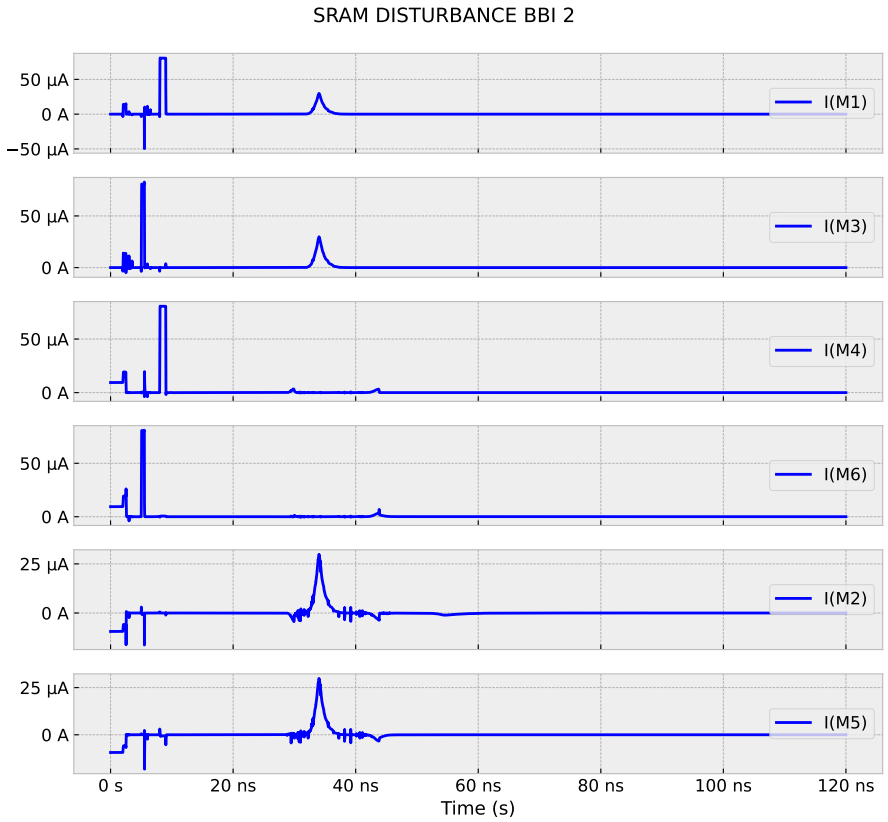




TRIPLE-WELL SUBSTRATE: OUT=L

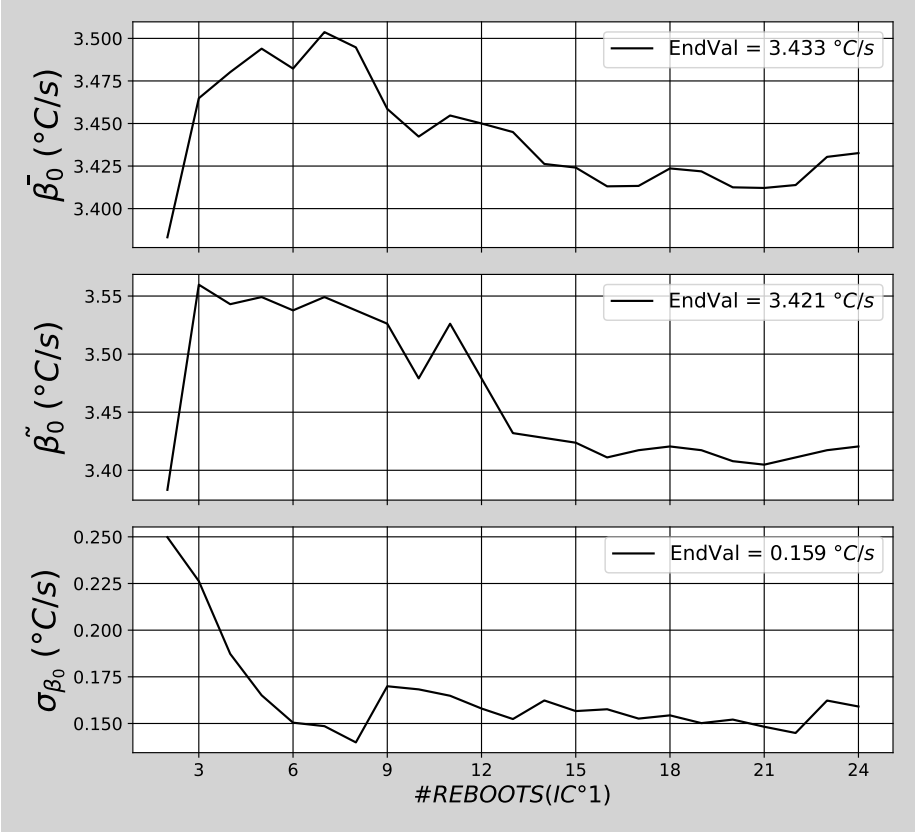
$$(Q - \bar{Q})_{INIT} = L$$

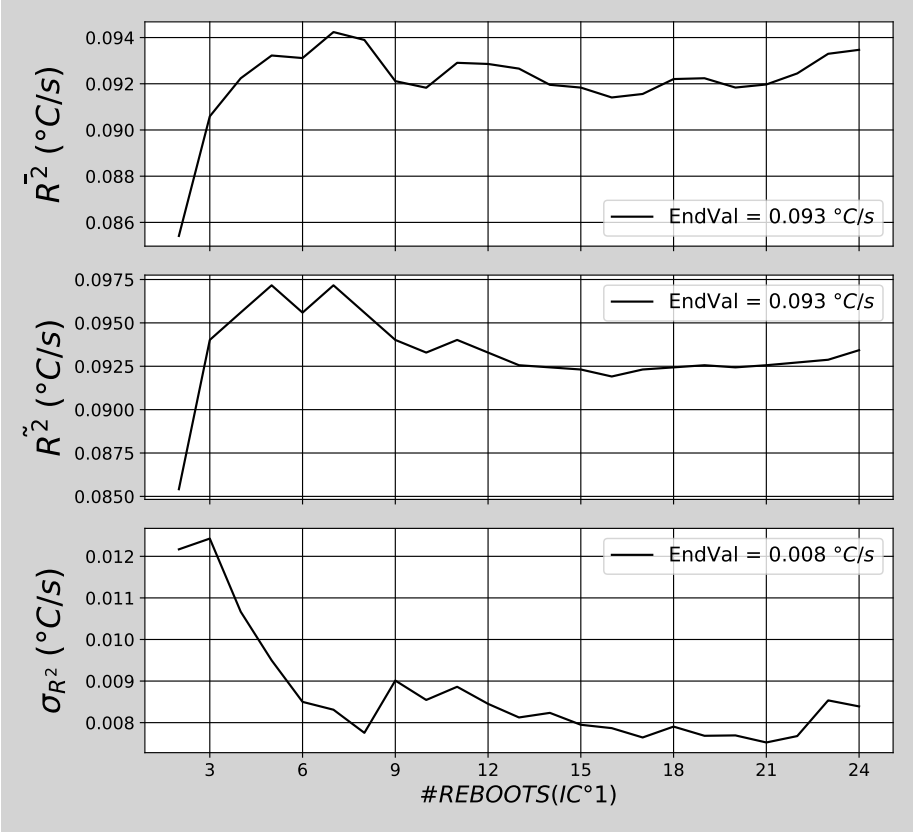




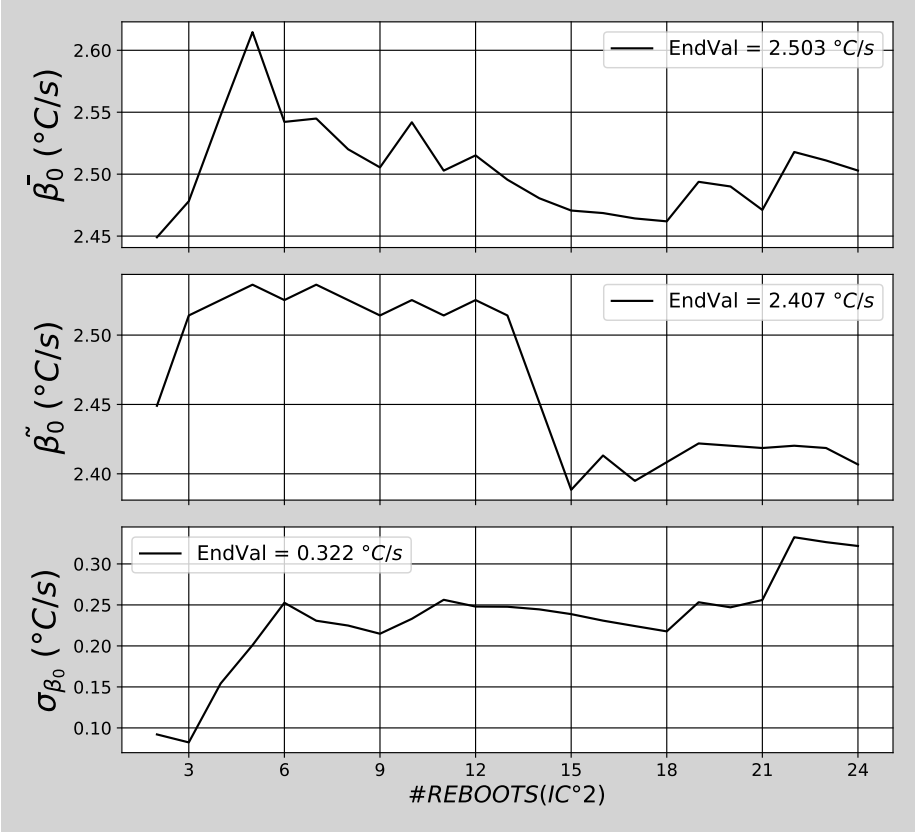
IC THERMAL ANALYSIS

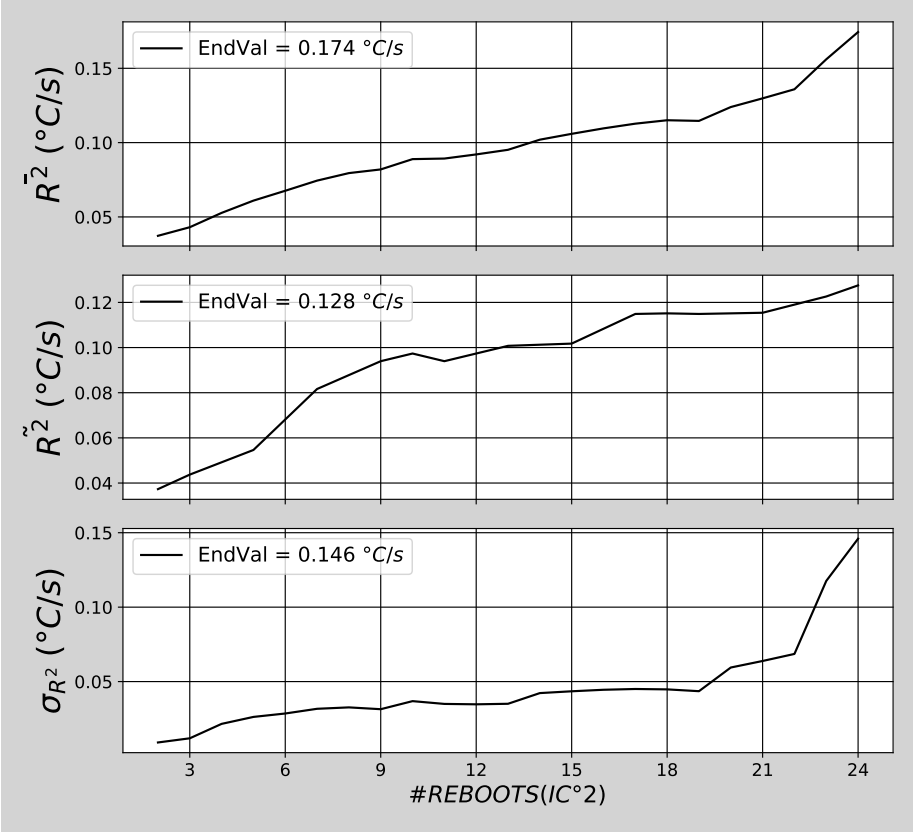
STM32 boot: IC1 → Opened



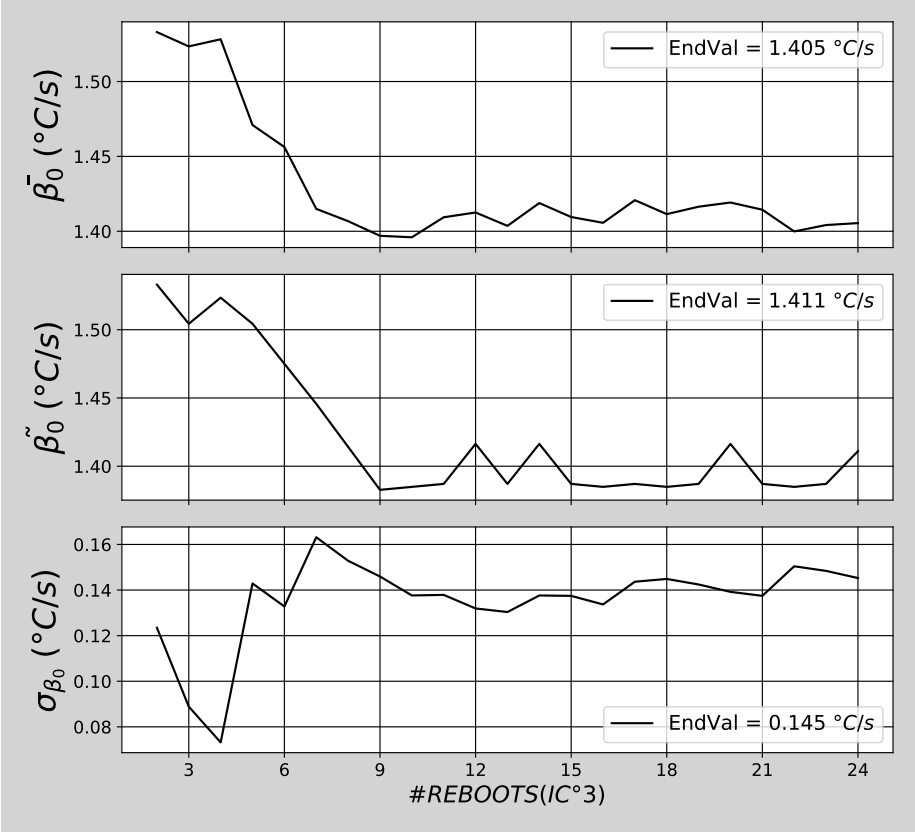


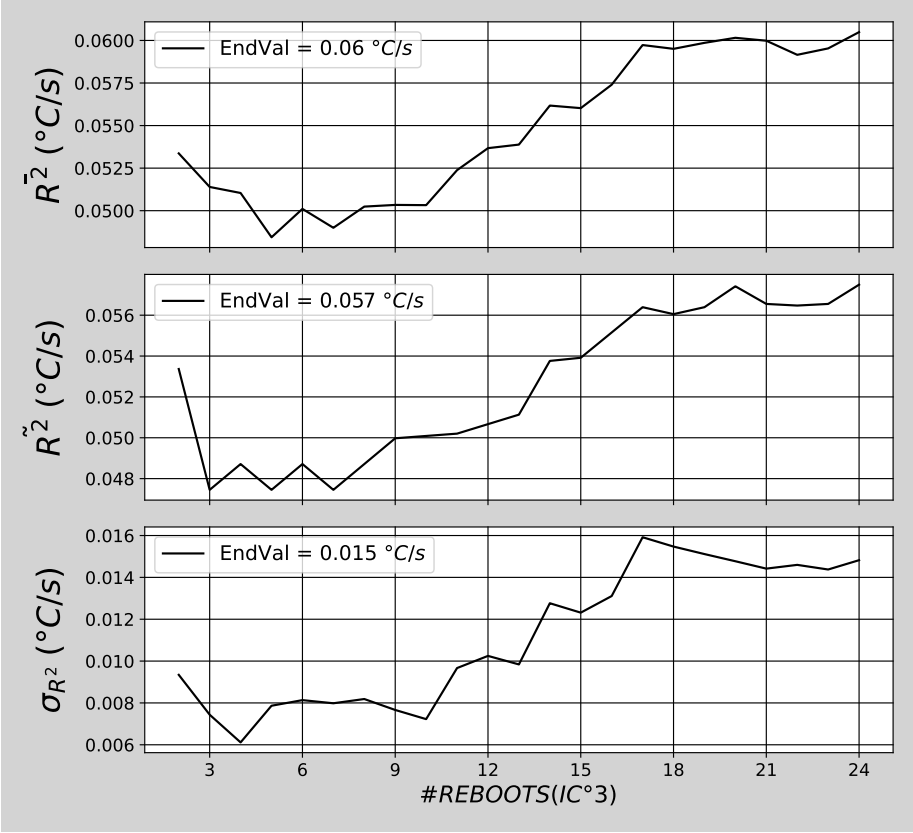
STM32 boot: IC2 → Normal



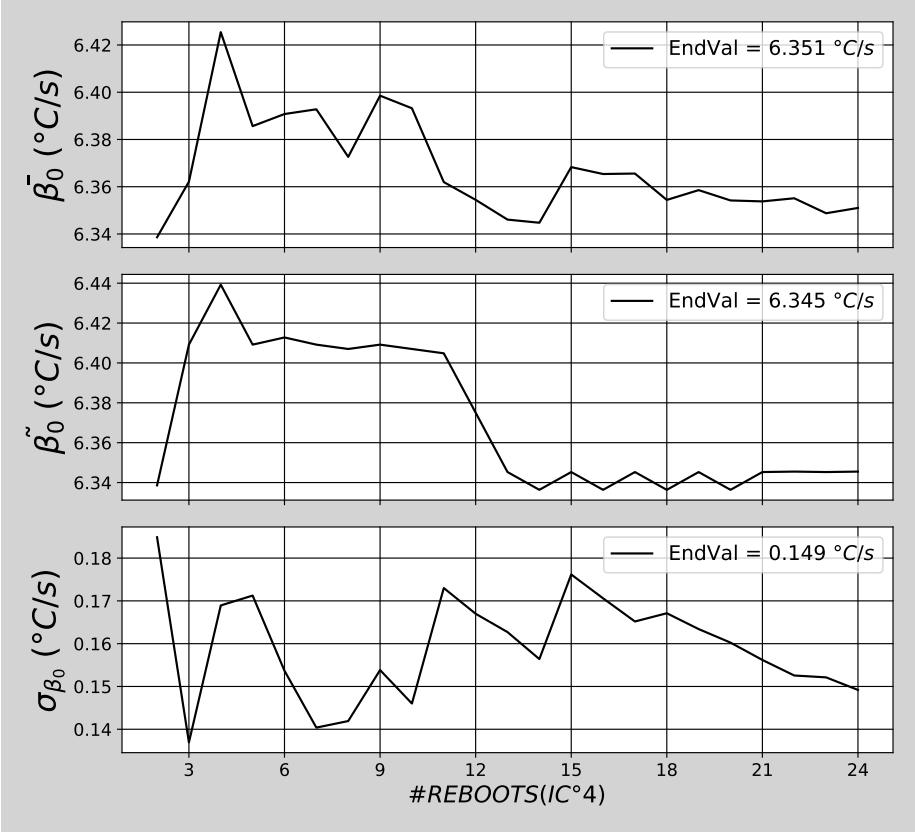


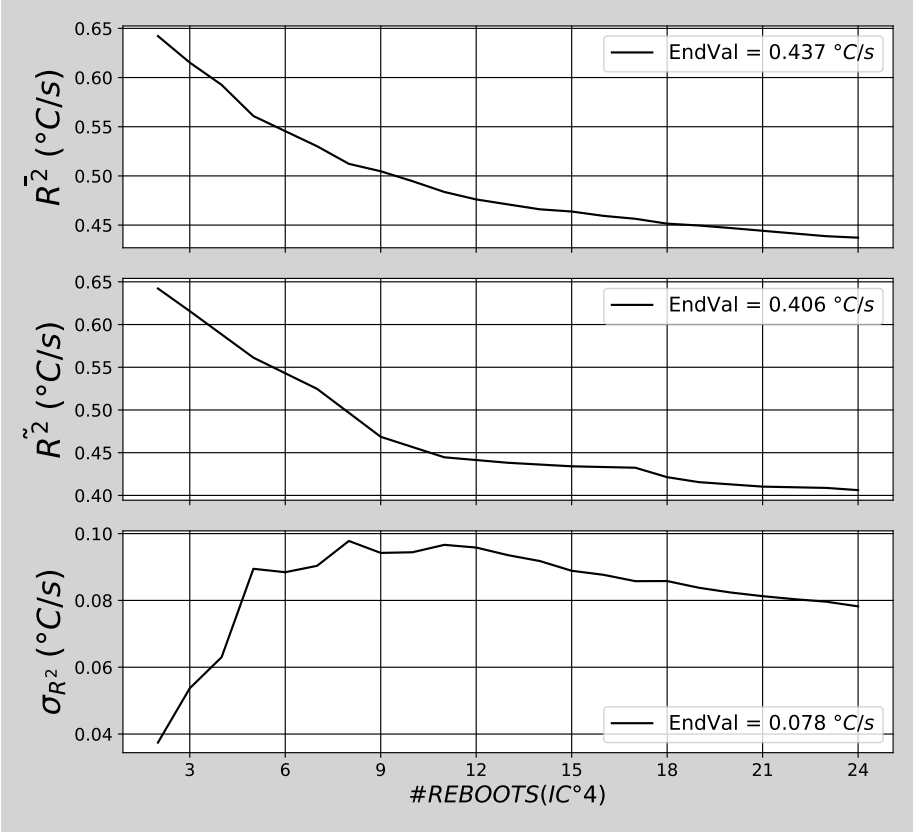
STM32 boot: IC3 → Closed



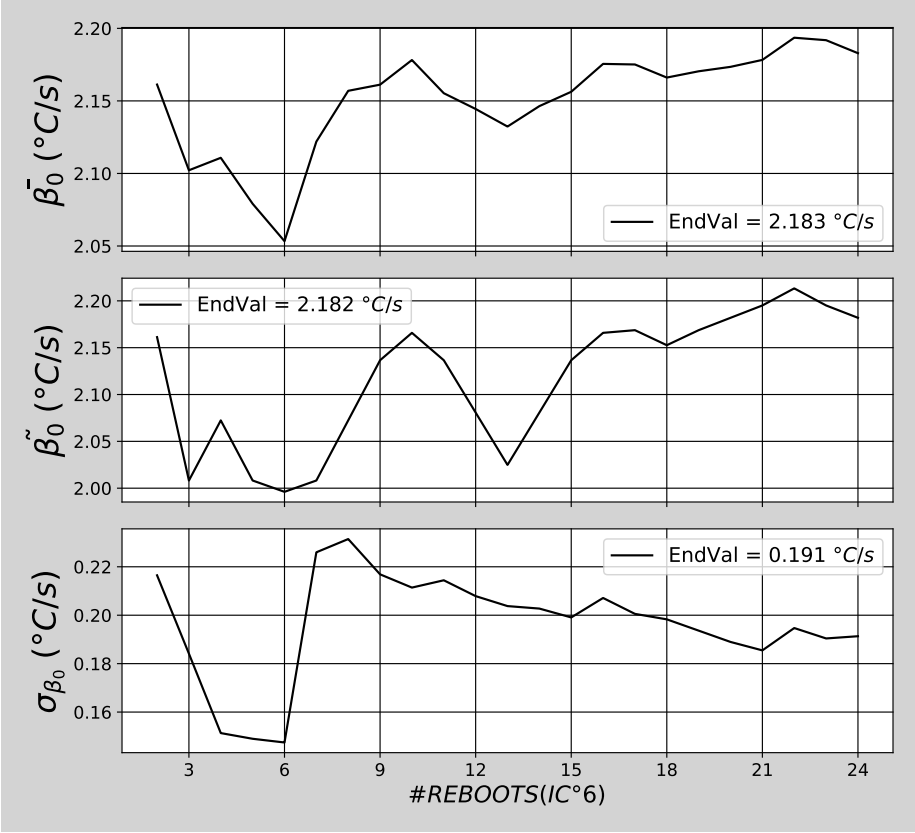


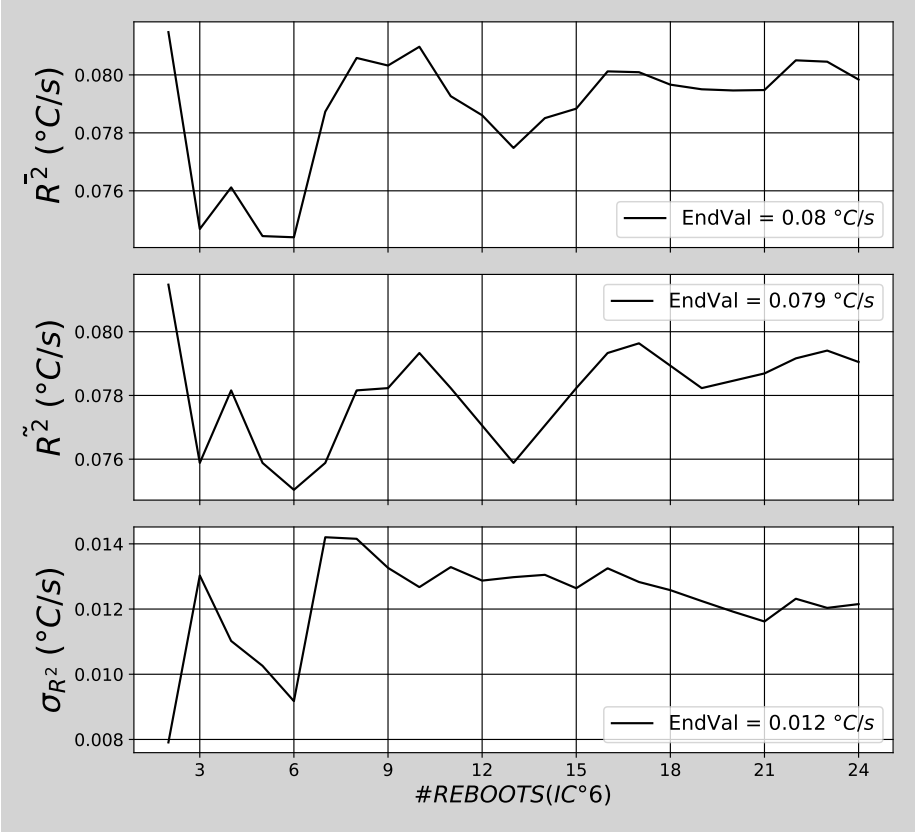
STM32 boot: IC4 → Opened



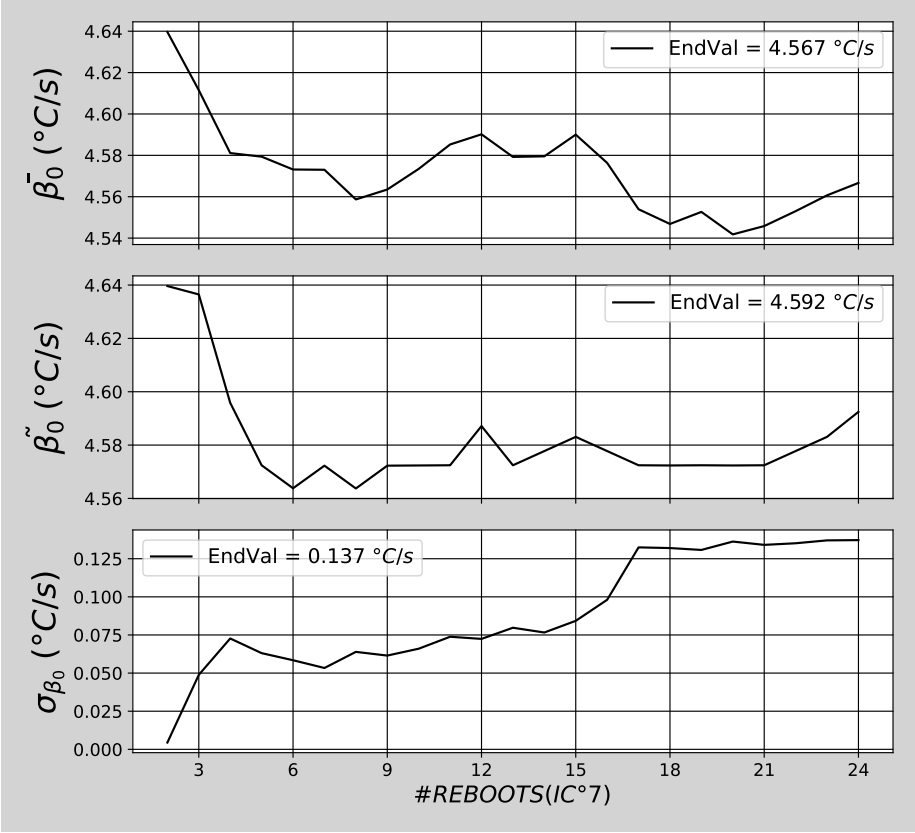


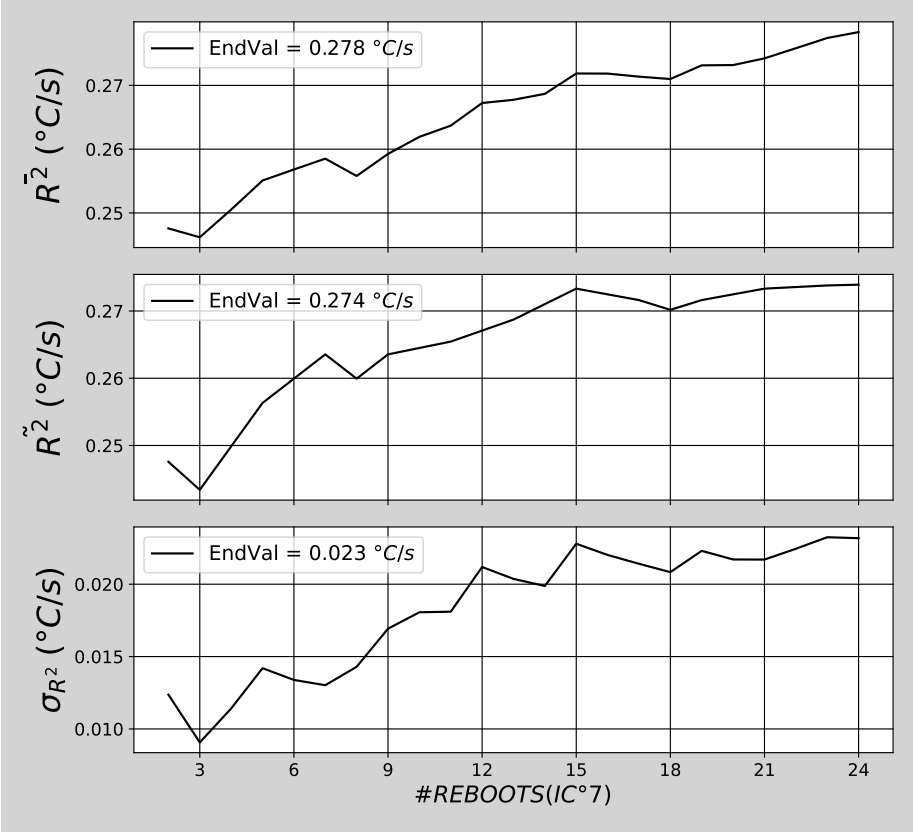
STM32 boot: IC6 → Closed



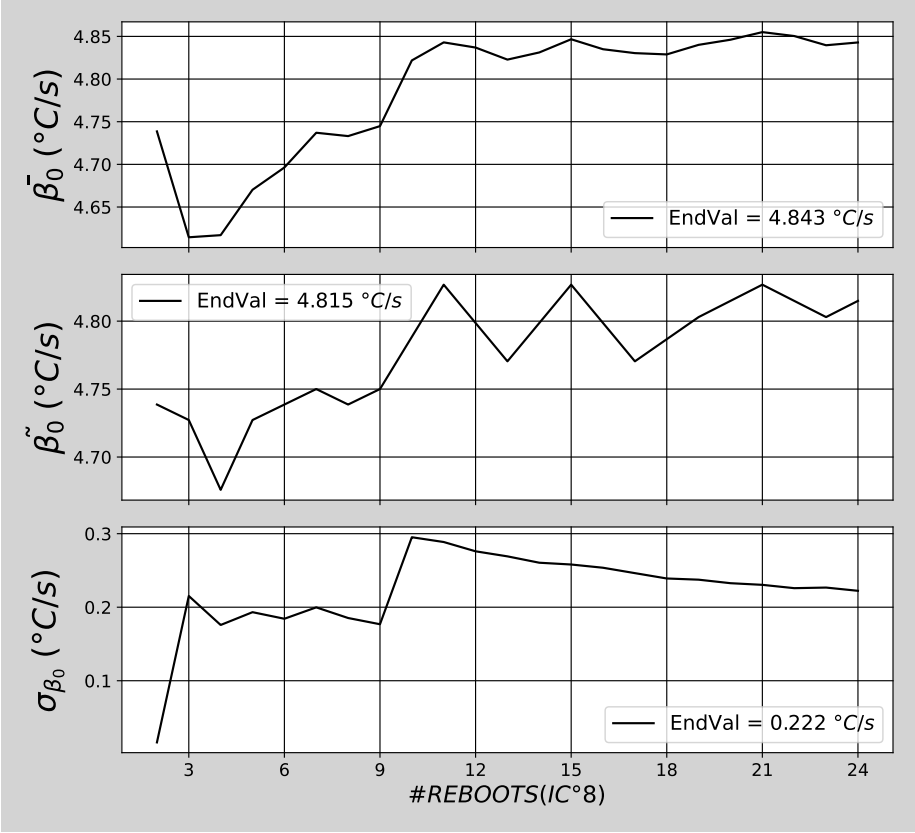


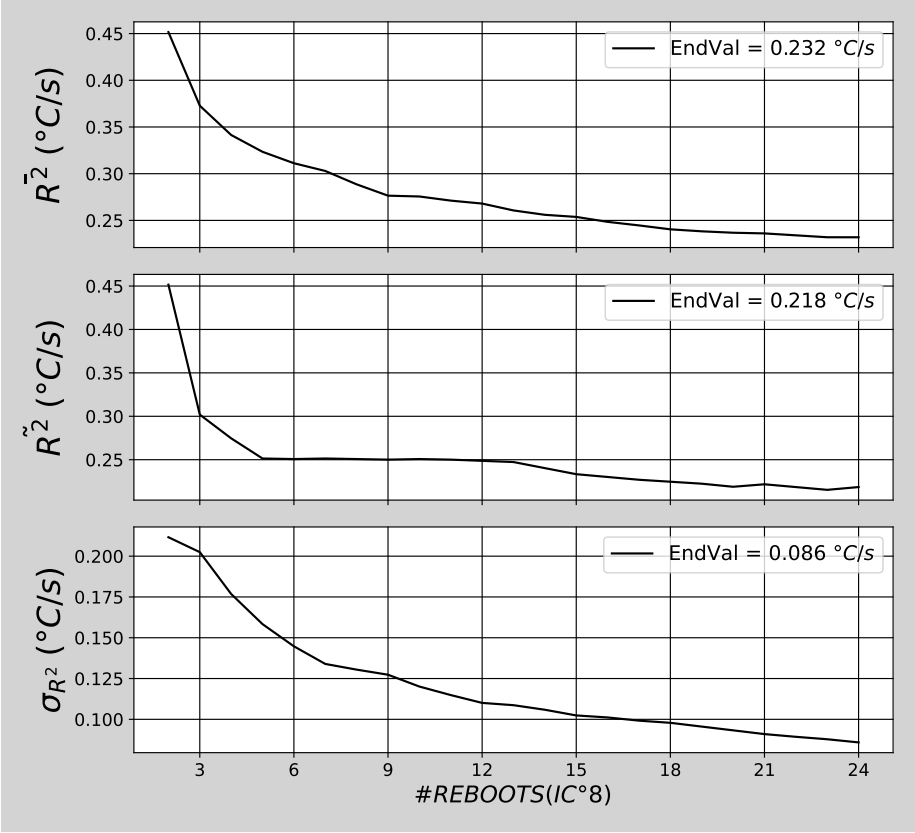
STM32 boot: IC7 → Opened



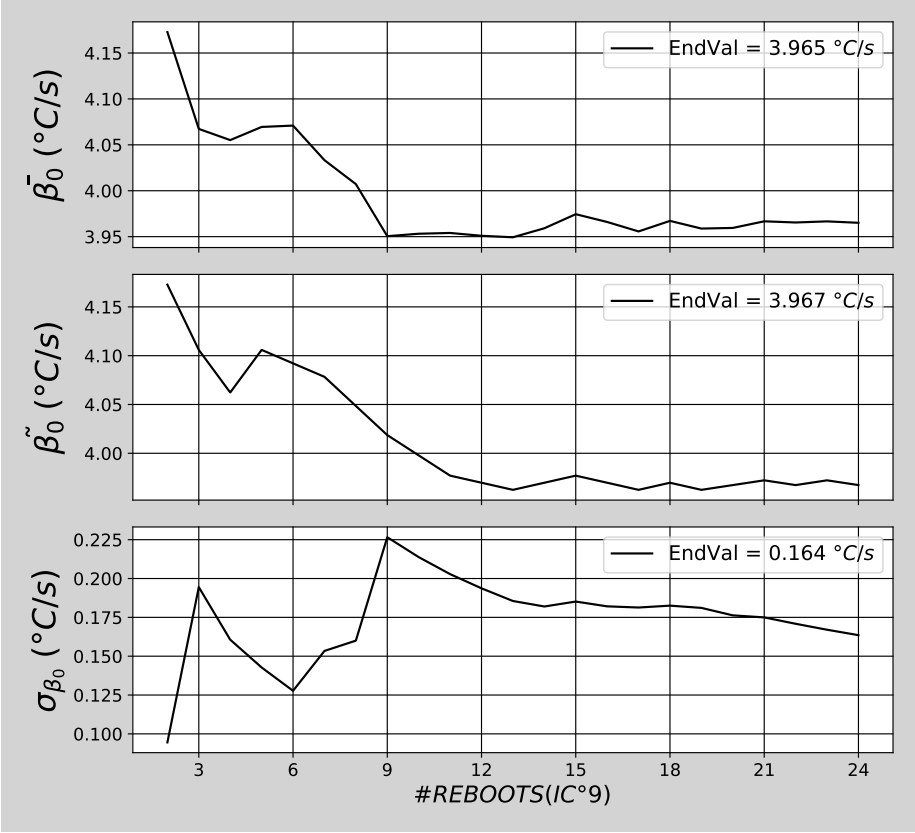


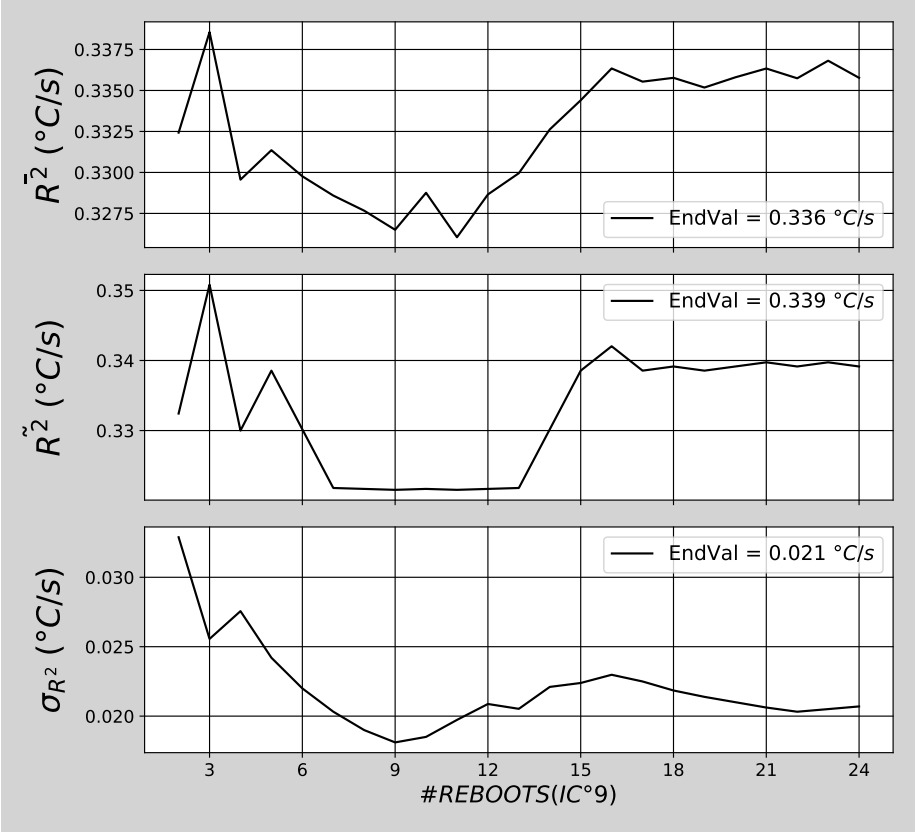
STM32 boot: IC8 → Opened



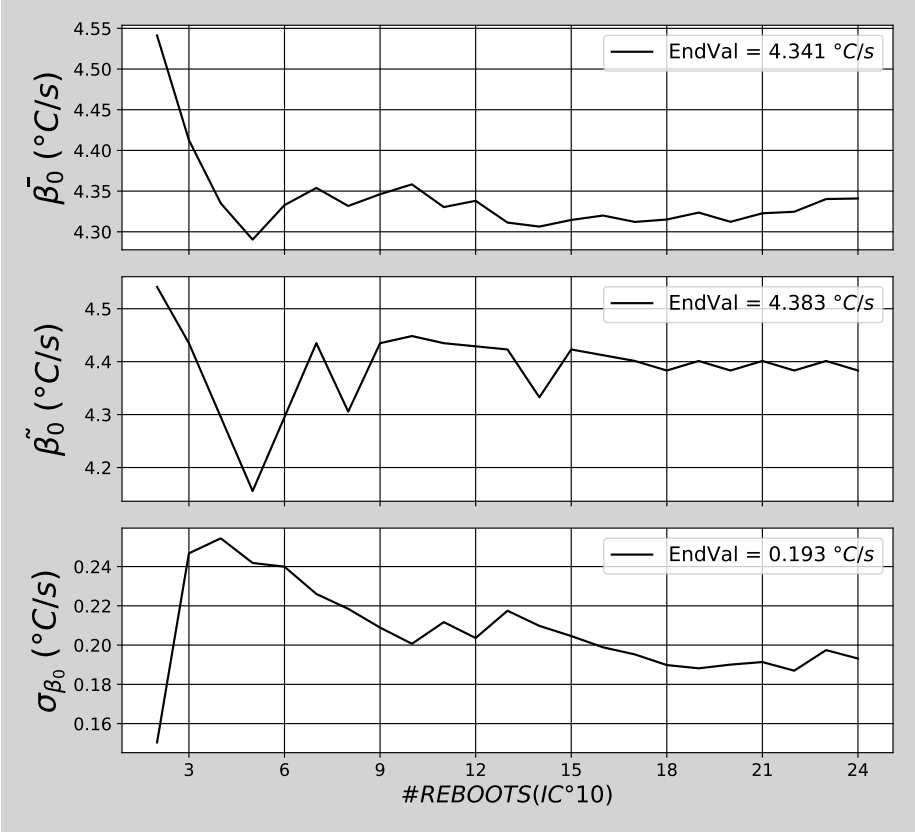


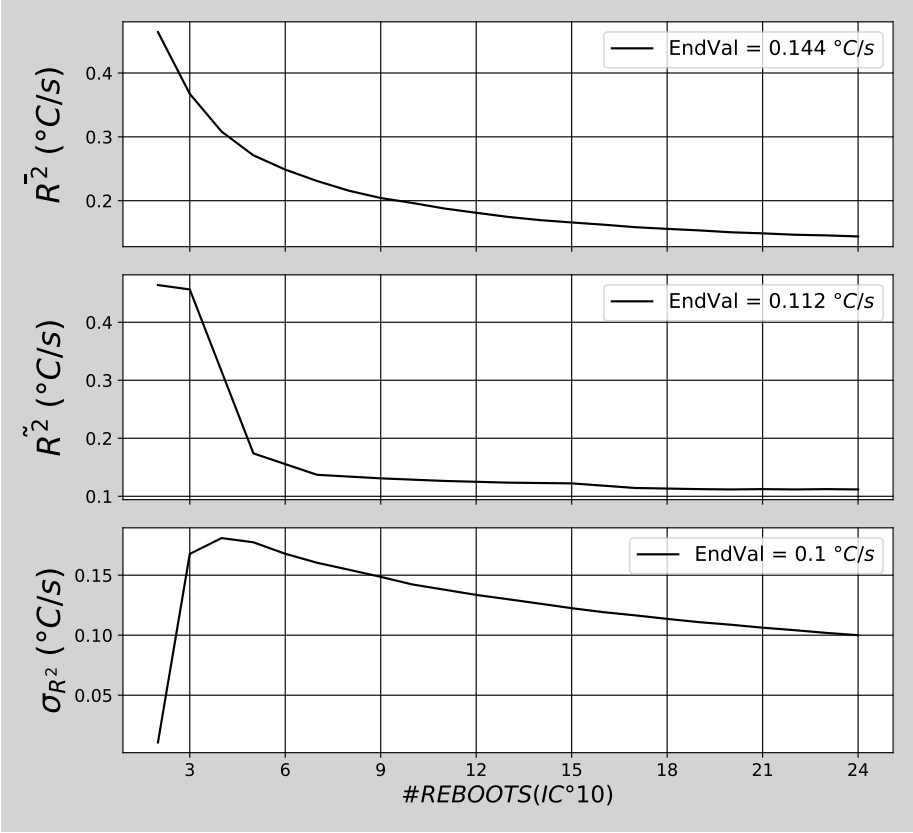
STM32 boot: IC9 → Opened



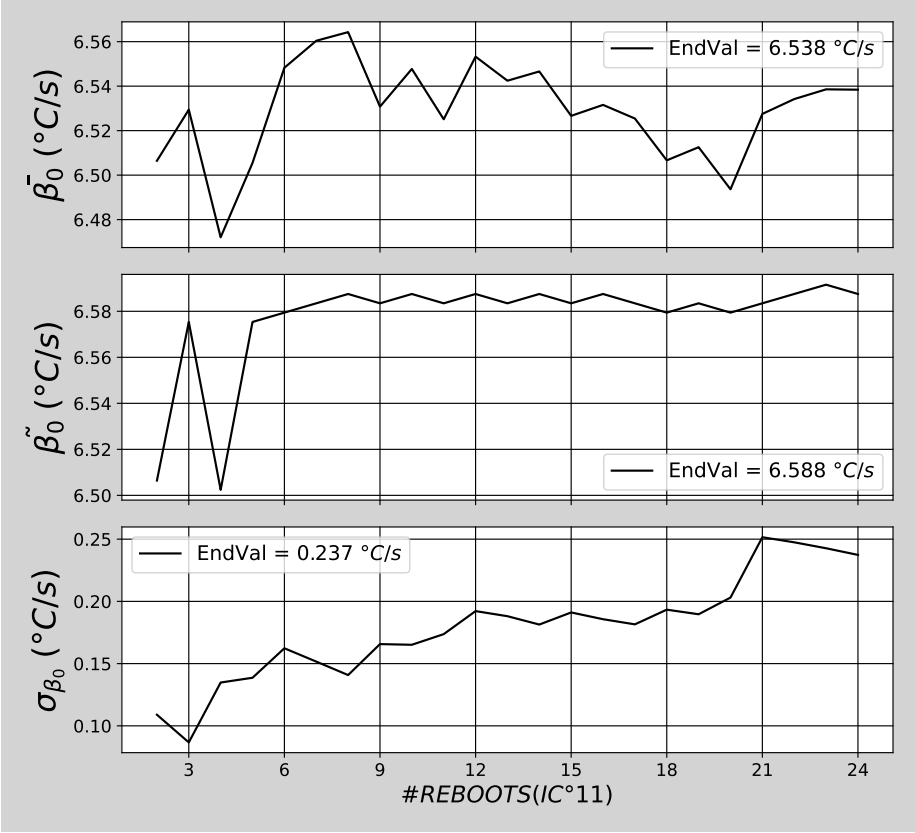


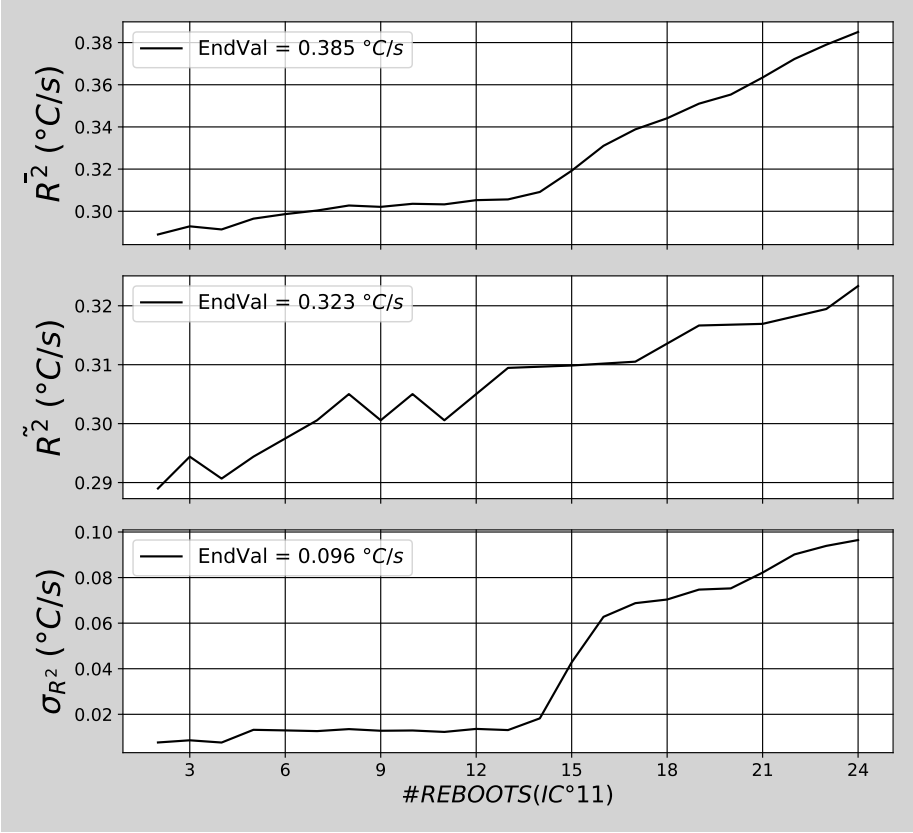
STM32 boot: IC10 → Opened



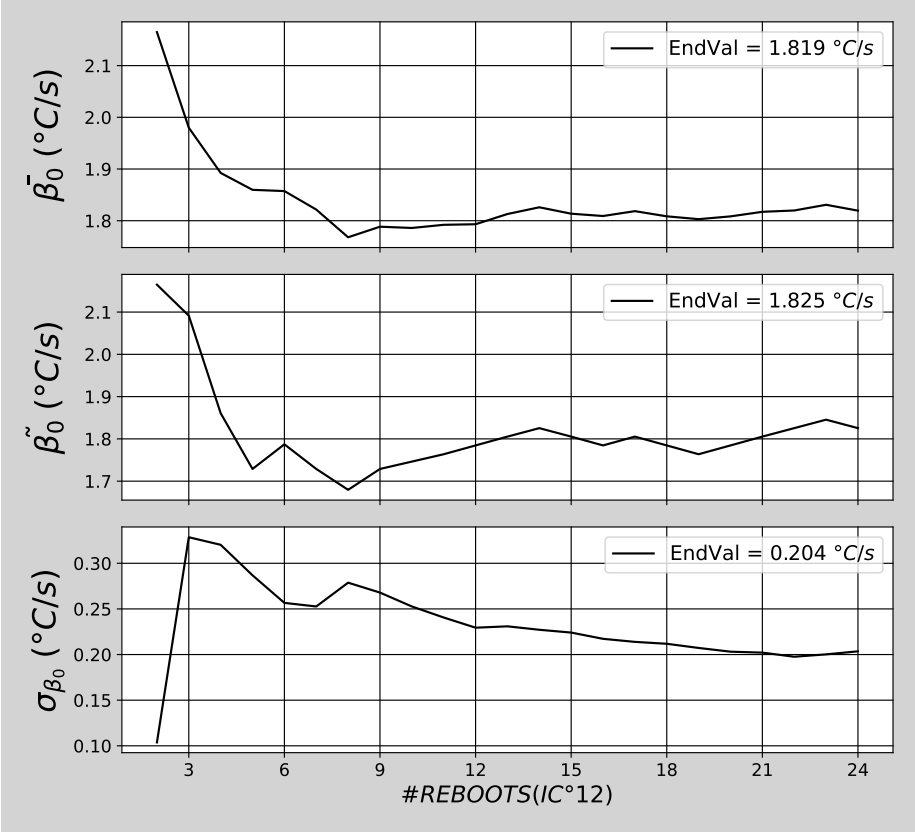


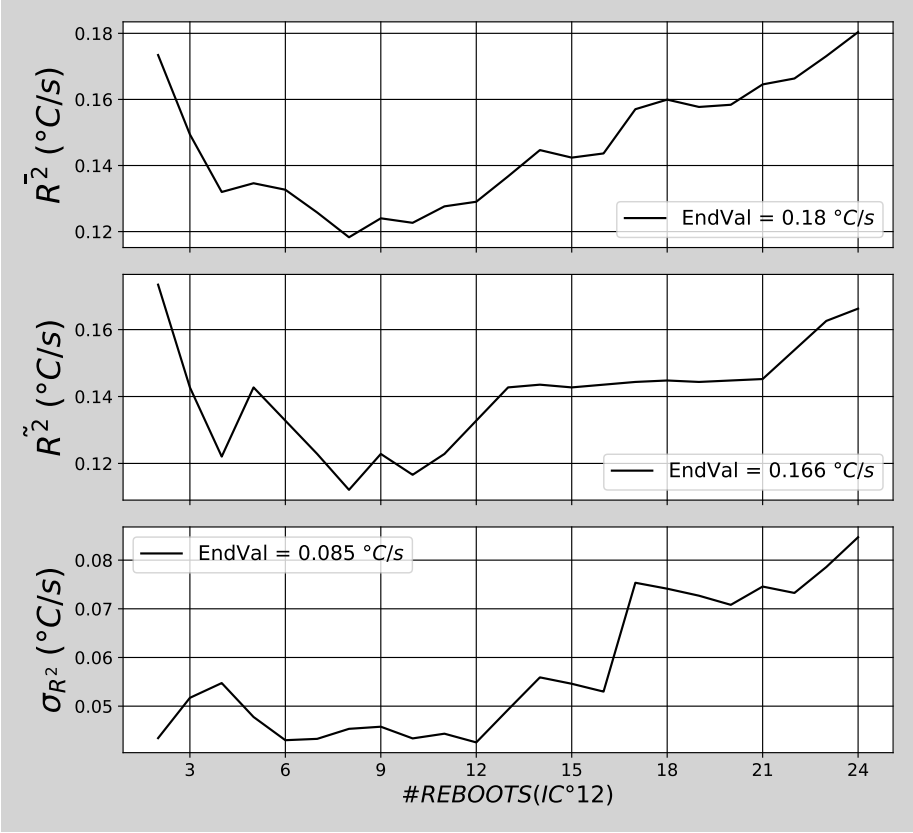
STM32 boot: IC11 → Opened



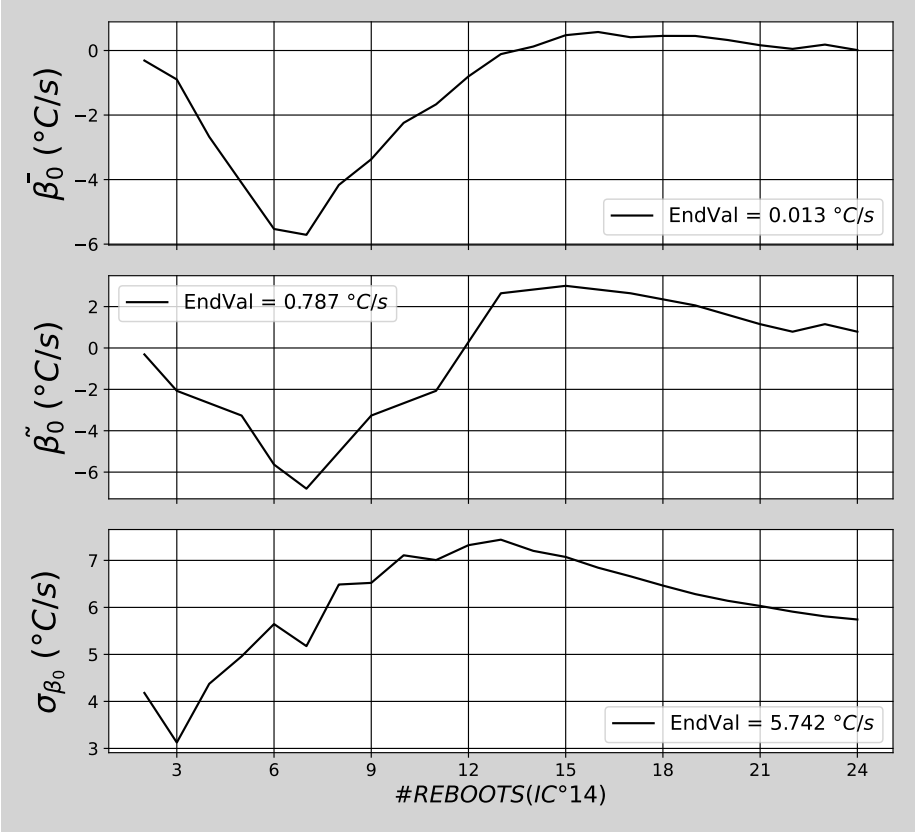


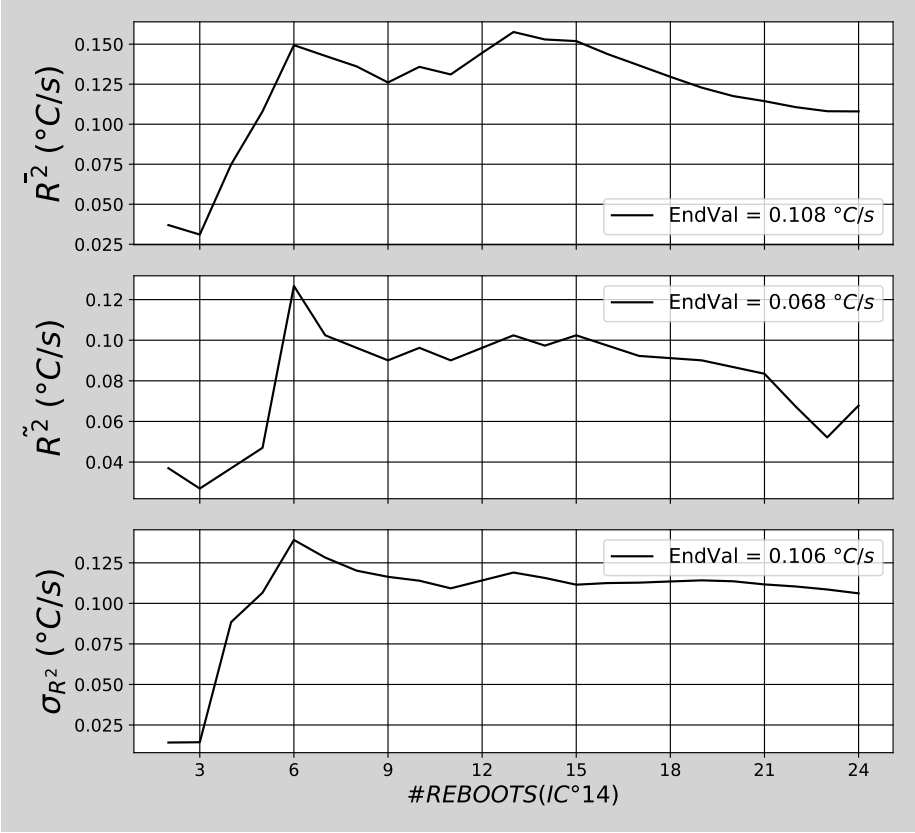
STM32 boot: IC12 → Closed



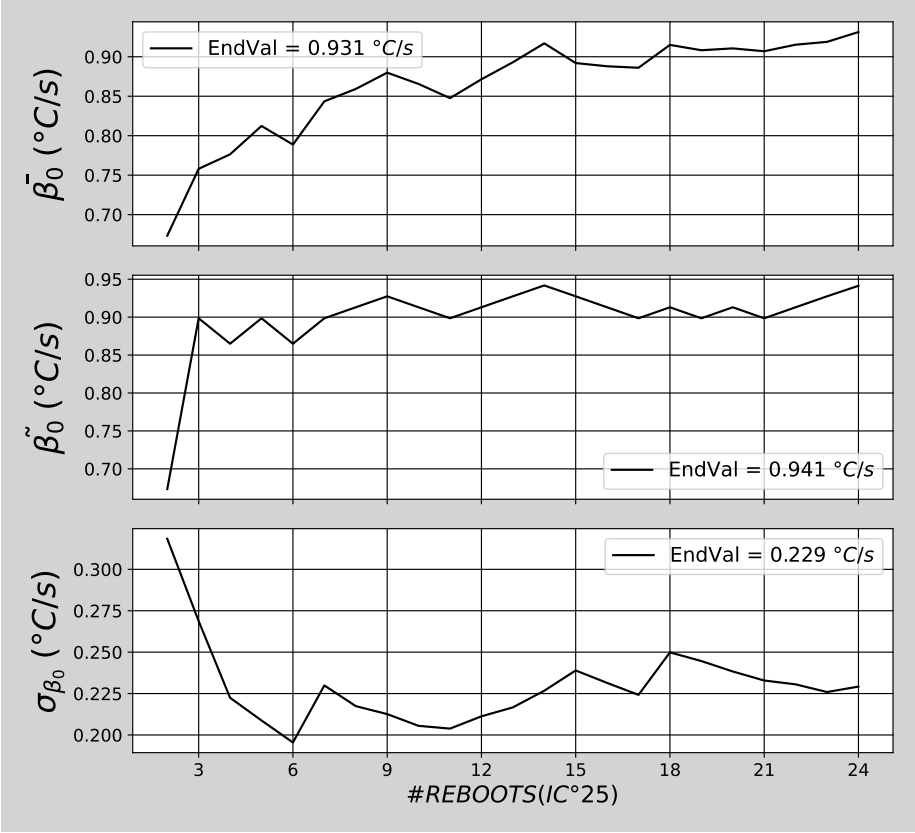


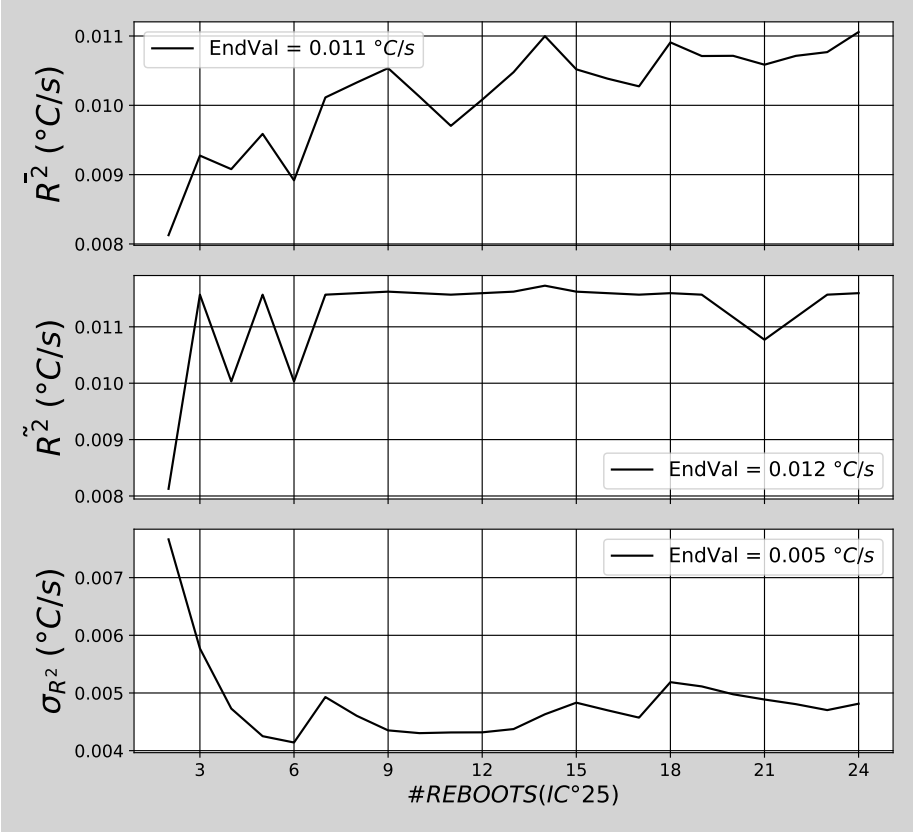
STM32 boot: IC14 → Opened → Faulty, discarded



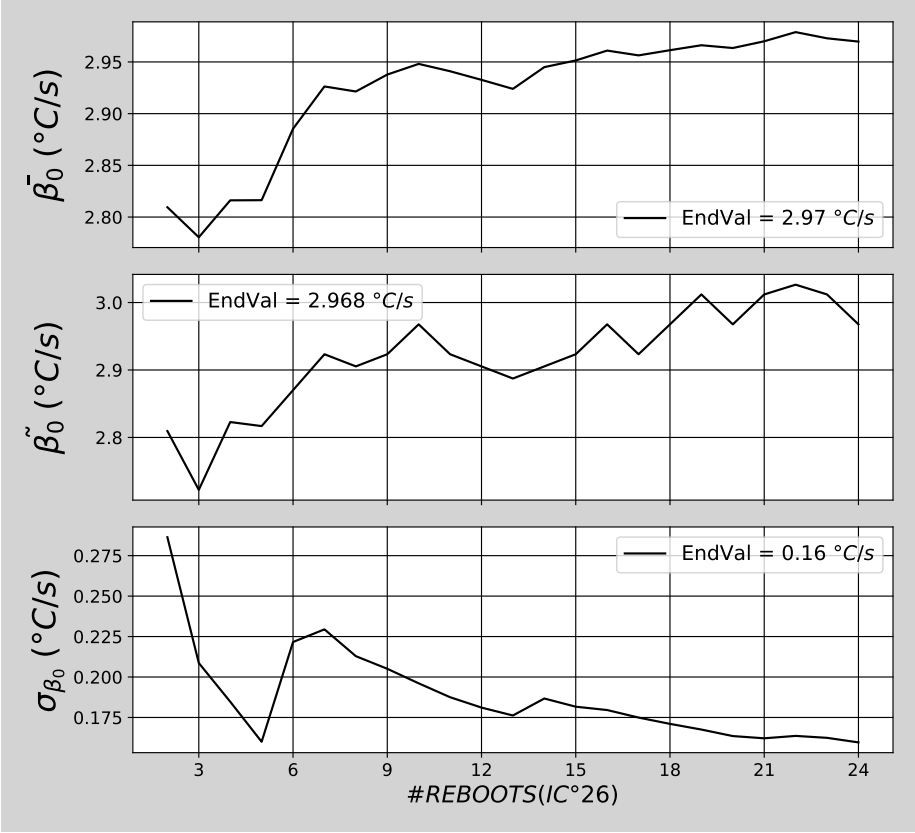


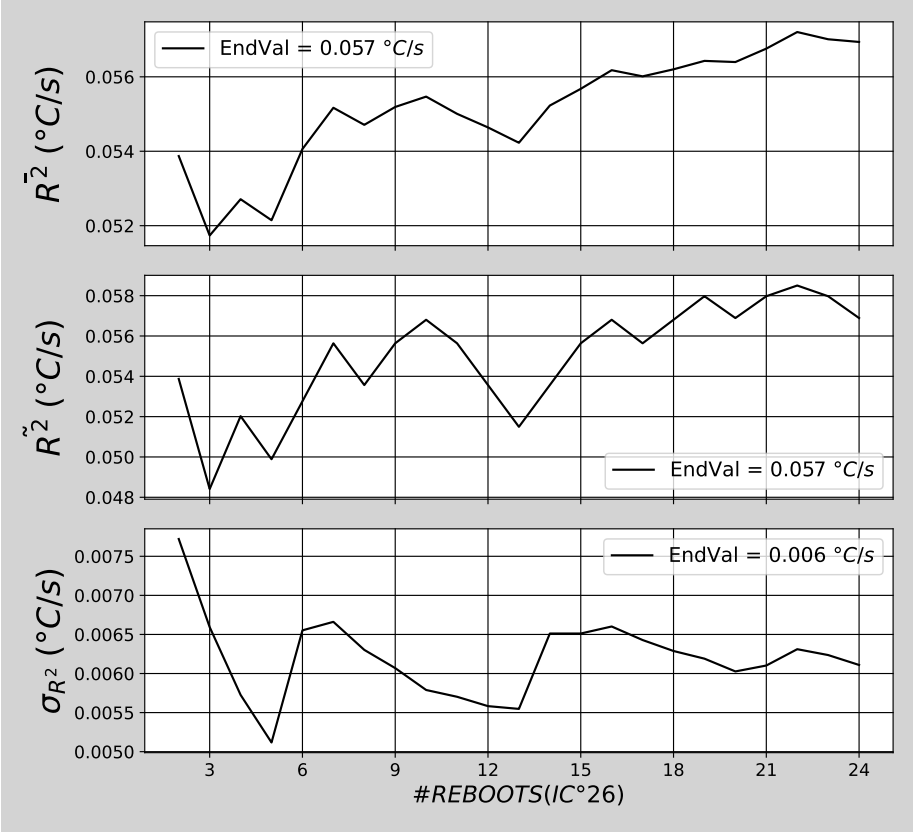
STM32 boot: IC25 → Closed





STM32 boot: IC26 → Closed





STM32 boot: summary

IC n°	$\bar{\beta}_0$ $(^\circ C/s)$	σ_{β_0} $(^\circ C/s)$	$\bar{R^2}$ $(^\circ C/s)$	σ_{R^2} $(^\circ C/s)$	Backside
25	0.931	0.229	0.011	0.005	Closed
3	1.405	0.145	0.06	0.015	Closed
12	1.819	0.204	0.18	0.085	Closed
6	2.183	0.191	0.08	0.012	Closed
2	2.503	0.322	0.174	0.146	Closed
26	2.97	0.16	0.057	0.006	Closed
1	3.433	0.159	0.093	0.08	Opened
9	3.965	0.167	0.336	0.021	Opened
10	4.341	0.193	0.144	0.1	Opened
7	4.567	0.137	0.278	0.023	Opened
8	4.843	0.222	0.232	0.086	Opened
4	6.351	0.149	0.437	0.078	Opened
11	6.539	0.237	0.385	0.096	Opened

STM32 boot: heatsink with 7 backside opened ICs

Open-air backside

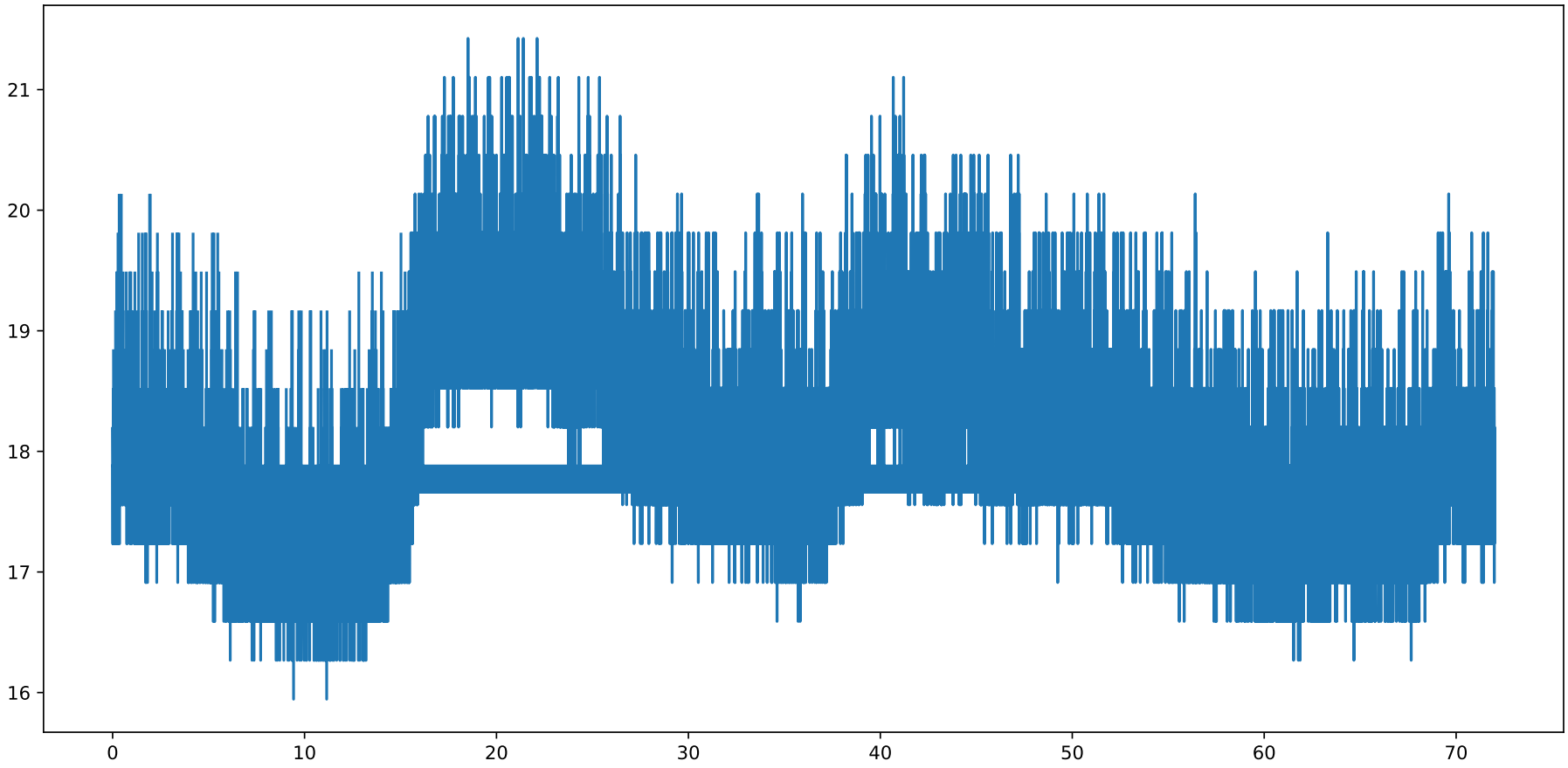
IC n°	$\bar{\beta}_0$ ($^\circ C/s$)	σ_{β_0} ($^\circ C/s$)
1	3.433	0.159
9	3.965	0.167
10	4.341	0.193
7	4.567	0.137
8	4.843	0.222
4	6.351	0.149
11	6.539	0.237

Heat-sunk backside

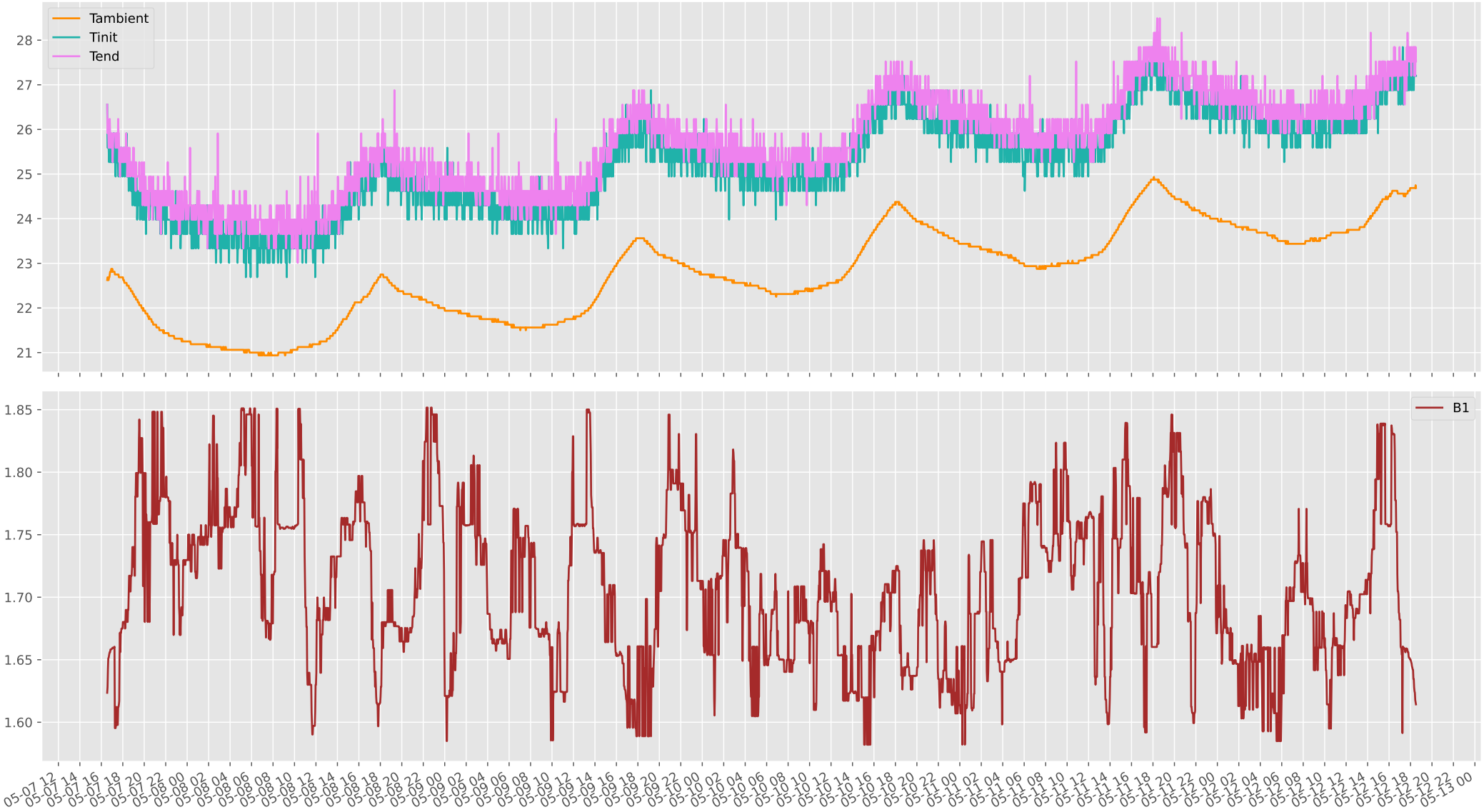
IC n°	$\bar{\beta}_0$ ($^\circ C/s$)	σ_{β_0} ($^\circ C/s$)
1	0.831	0.222
9	0.976	0.172
10	0.203	0.122
7	1.728	0.161
8	2.771	0.853
4	4.139	0.311
11	2.996	0.213

STM32 temperature over 72 hours

Beginning: 20:00

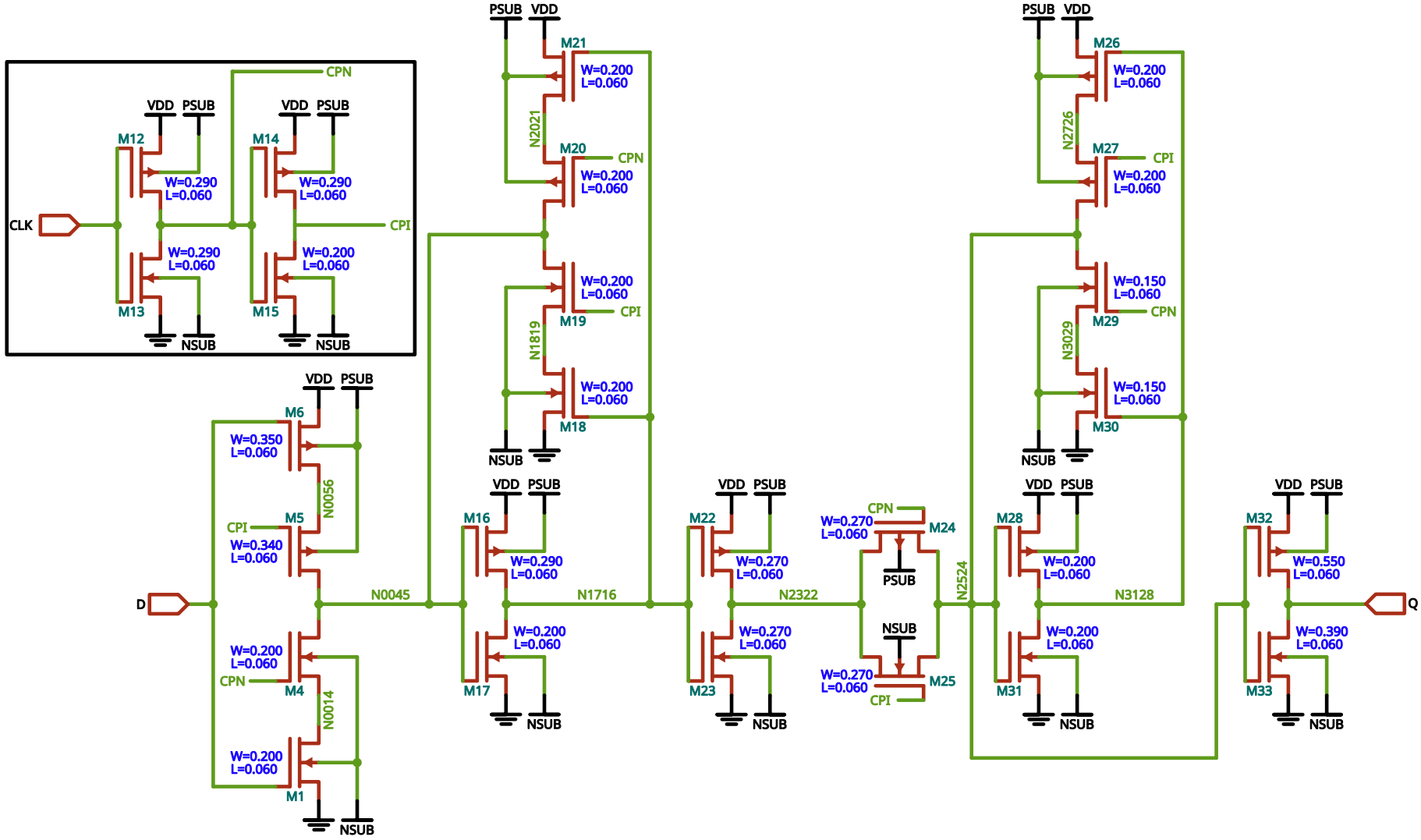


STM32 5 days experiment: Beginning around 16:00 May 7th

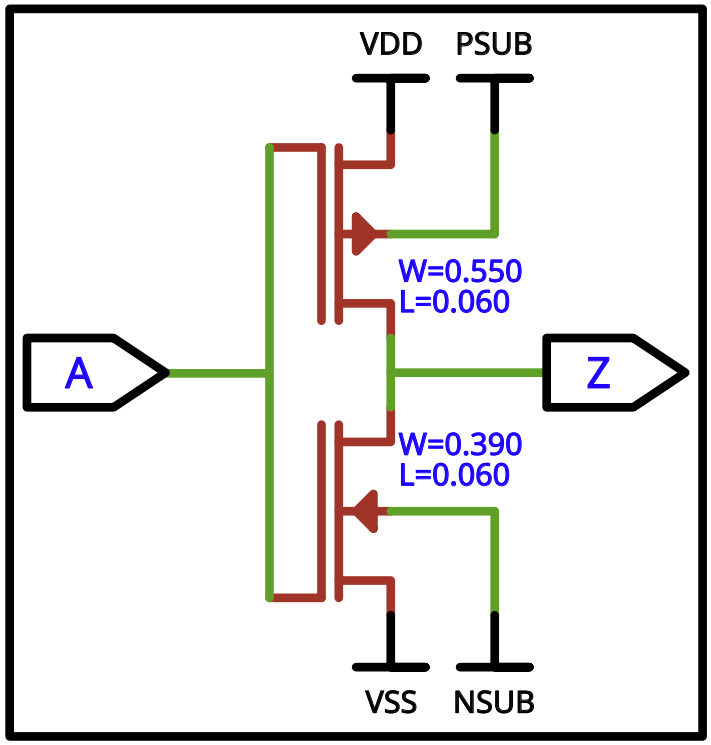


DFF logic path under BBI

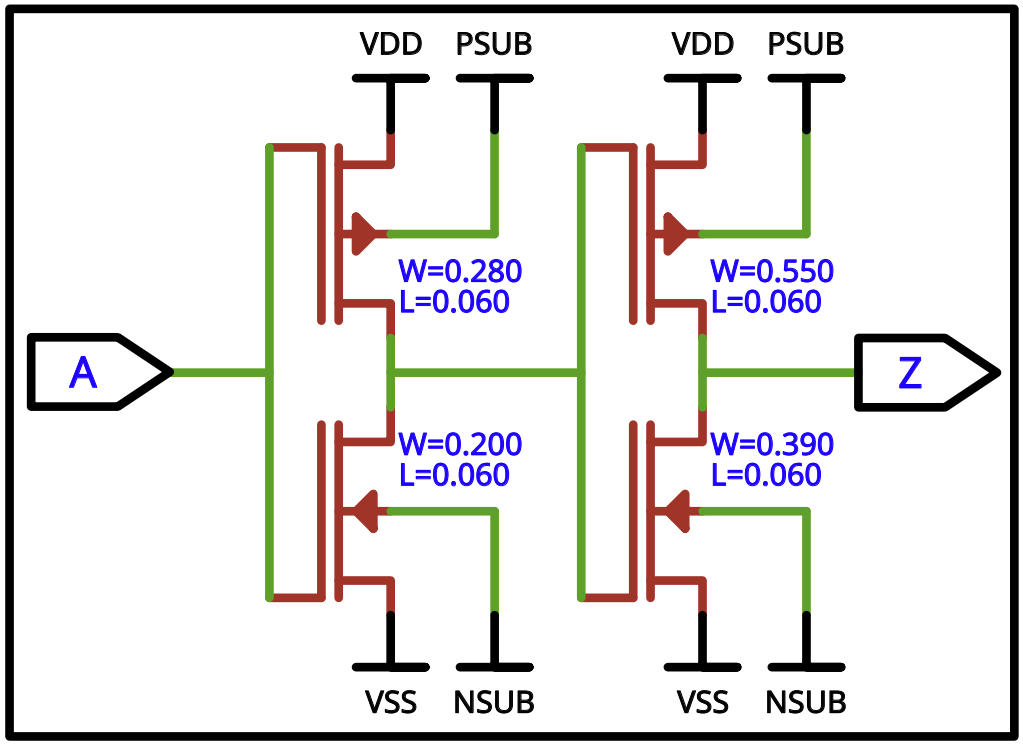
DFF schematic: CORE65GPSVT_HS65_GS_DFPQX4



Inverters and buffers schematics

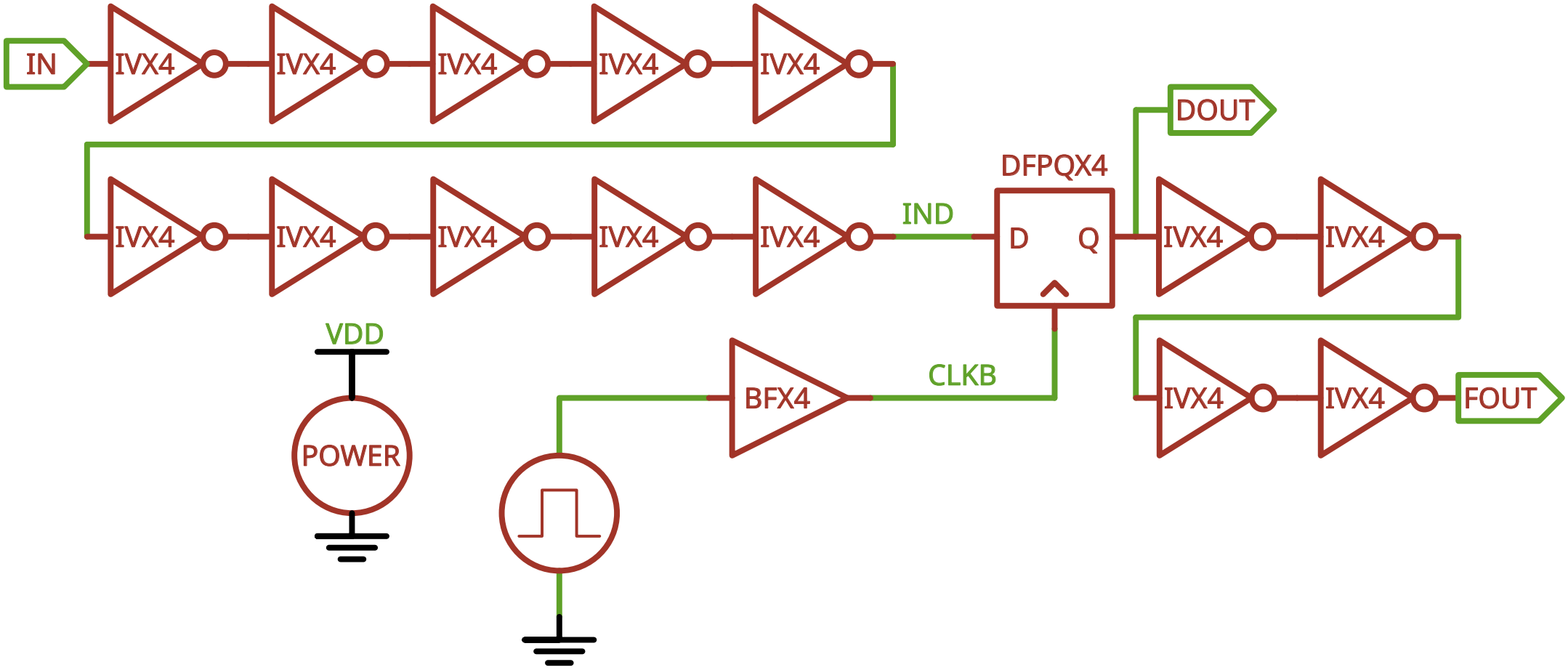


CORE65GPSVT_HS65_GS_IVX4

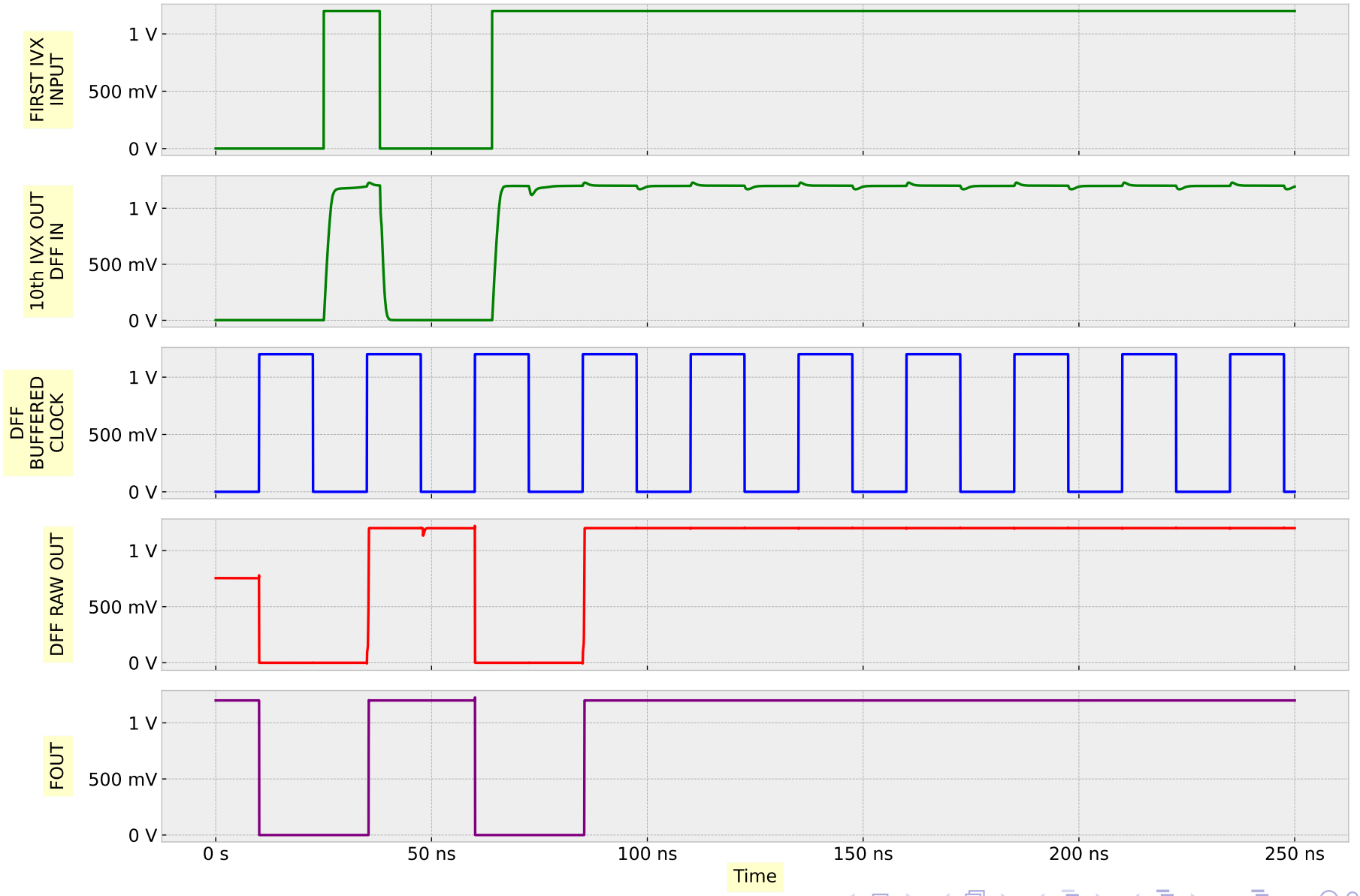


CORE65GPSVT_HS65_GS_BFX4

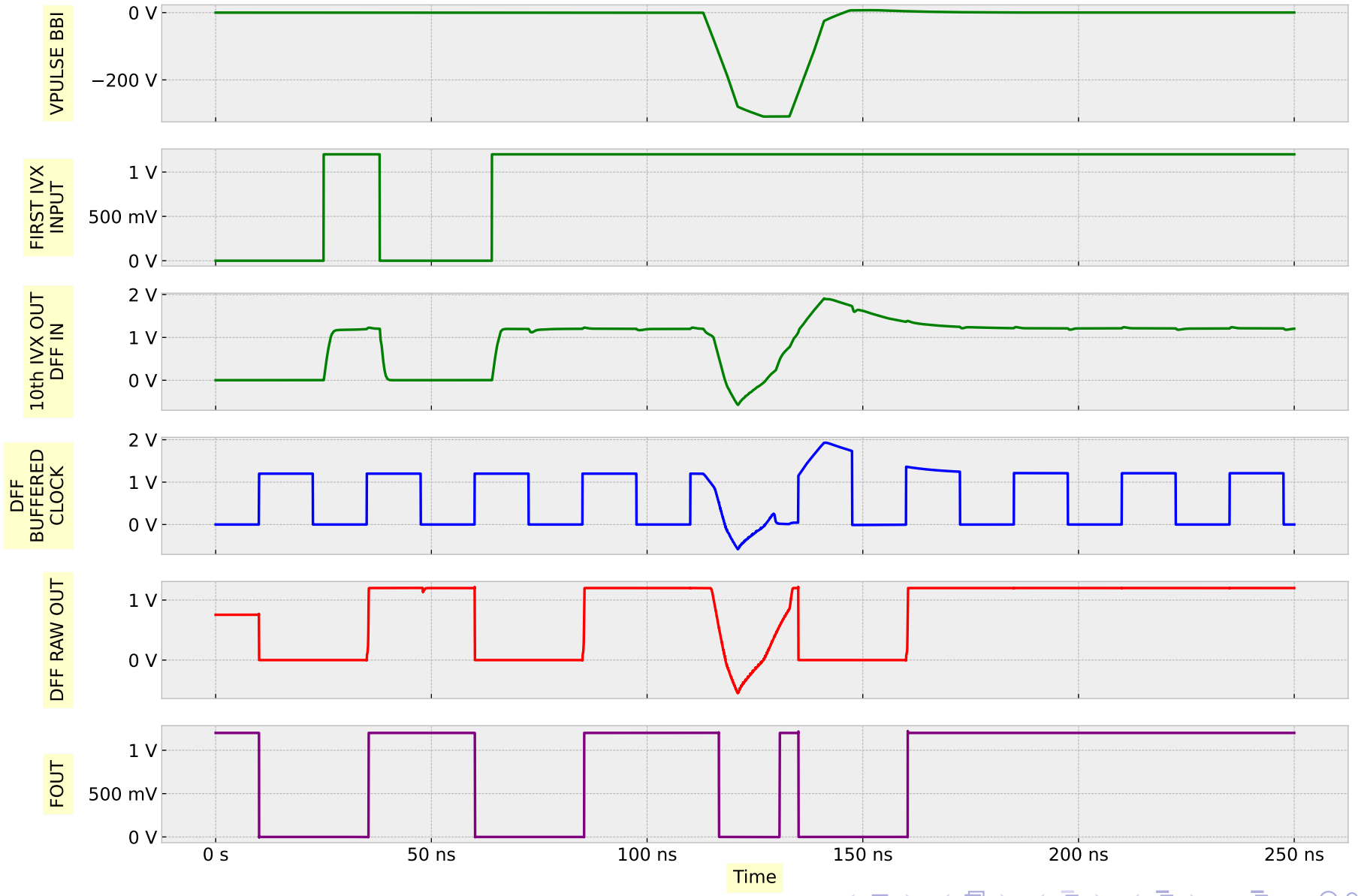
Simulated symbolic netlist



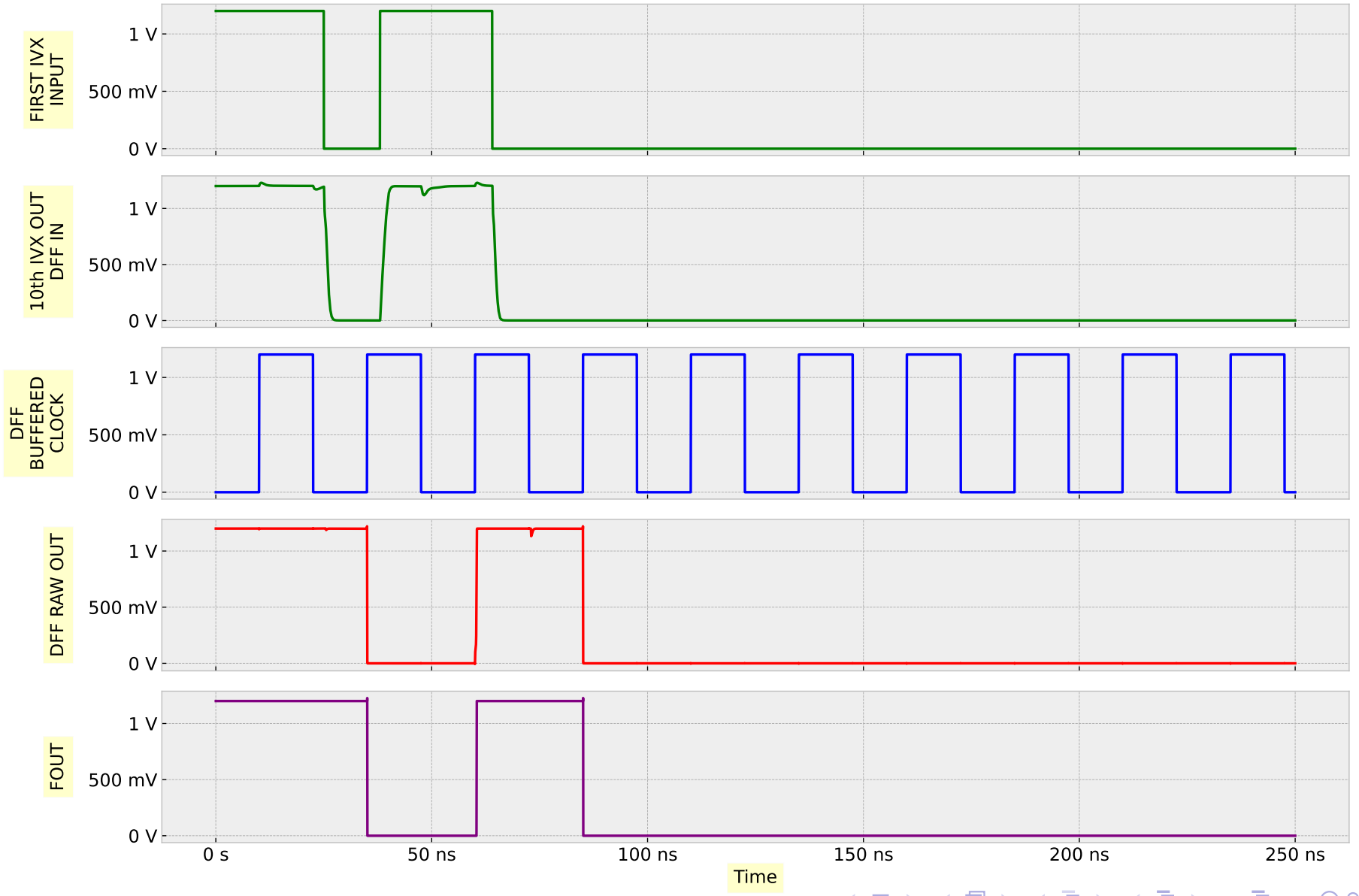
DFF simulation: IDLE NORMALLY HIGH



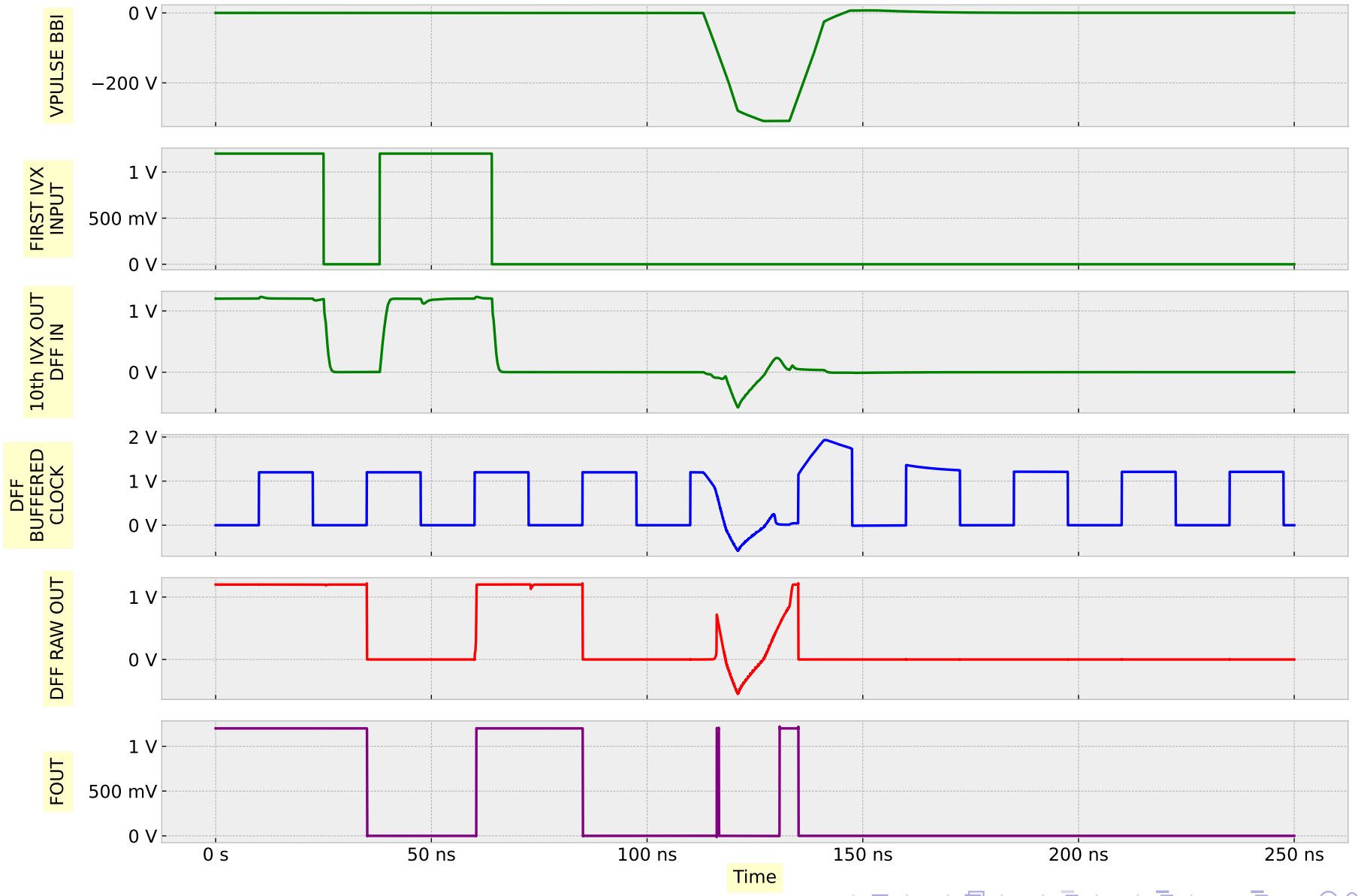
DFF simulation: BBI NORMALLY HIGH



DFF simulation: IDLE NORMALLY LOW



DFF simulation: BBI NORMALLY LOW



BLANK FRAME

NO CONTENT