

# FPGAs, HLS Tools & Runtime Systems

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# Overview

## FPGAs structure

- Look-Up Table

- Basic Logic Element

- Overview

## Optimization Using HLS tools

- Problem Description

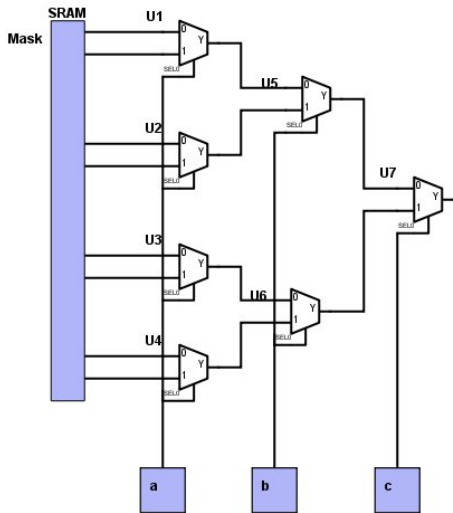
- Serial Version

- Opt1: Inner Loop Unrolling

- Pipeline

# FPGAs Structure

## LUT



- ▶ It is a **table** that determines what the output is for any given input
- ▶ A **state-less** interconnection of any number of gates (no feedback loops)
- ▶ Implemented *multiplexing* a combination of SRAM bits

Figure: 3 stages of 2x1 MUX

# FPGAs Structure

## LUT Example

$$y = (a + b) \cdot c$$

a	b	c	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

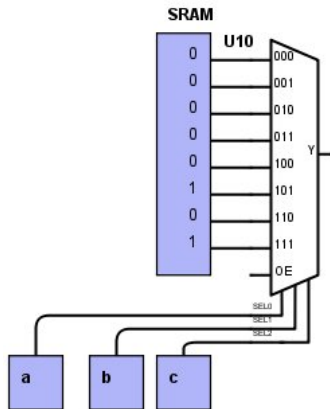


Figure:  $y = (a + b) \cdot c$

# FPGAs structure

## BLE

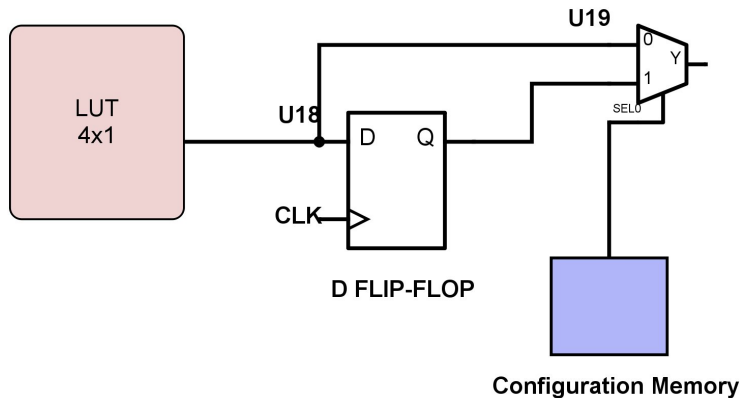


Figure: Basic Logic Element

# FPGAs structure

## Overview

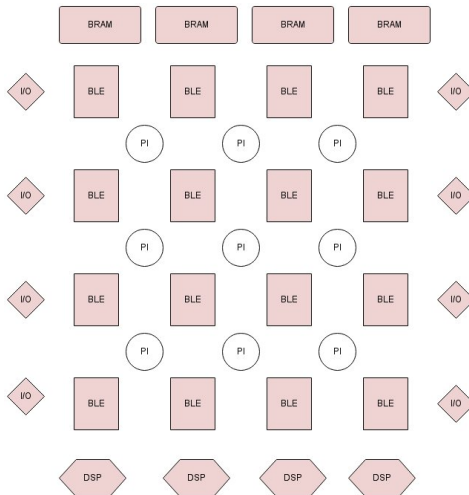


Figure: FPGAs Complete Overview

# Problem Description

## Matrix Multiplication

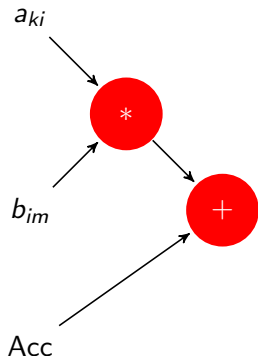
$$C = A * B$$

$$c_{ij} = \sum_{k=1}^n a_{ik} b_{kj}$$

$$\begin{array}{ccc|cccc} c_{11} & \dots & c_{1n} & a_{11} & a_{12} & \dots & a_{1n} \\ \vdots & & \vdots & \vdots & \vdots & & \vdots \\ \vdots & c_{km} & \vdots & a_{k1} & a_{k2} & \dots & a_{kn} \\ c_{n1} & \dots & c_{nn} & \vdots & \vdots & & \vdots \\ & & & a_{n1} & a_{n2} & \dots & a_{nn} \end{array} \quad \begin{array}{ccccc|ccccc} b_{11} & \dots & b_{1m} & \dots & b_{1n} \\ b_{21} & \dots & b_{2m} & \dots & b_{2n} \\ \vdots & & \vdots & & \vdots \\ b_{n1} & \dots & b_{nm} & \dots & b_{nn} \end{array}$$

# No Directives

$$c_{km} = a_{k1}b_{1m} + a_{k2}b_{2m} + \cdots + a_{kn}b_{nm}$$

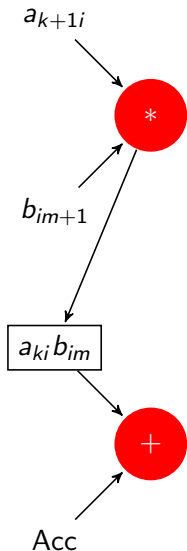


- ▶  $2n$  operations  $\forall$  element
- ▶  $n^2$  elements
- $\Rightarrow 2n^3$  operations
- ▶ 19MFLOPS on the tested platform



## Opt1: Sum Mul Overlapping

In the scope of this paper it is considered that the clock cycle is adjusted to the execution depth of the multiplication.



- ▶ Complete overlapping between Multiplication and addition
- ▶ 35MFLOPS on the given machine

# Pipeline

**Initiation Interval** is called the number of cycles between two new iterations.

In this case it is indicated by the time that the addition register is occupied.





