FPGAs, HLS Tools & Runtime Systems

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Overview

FPGAs Structure

LUT

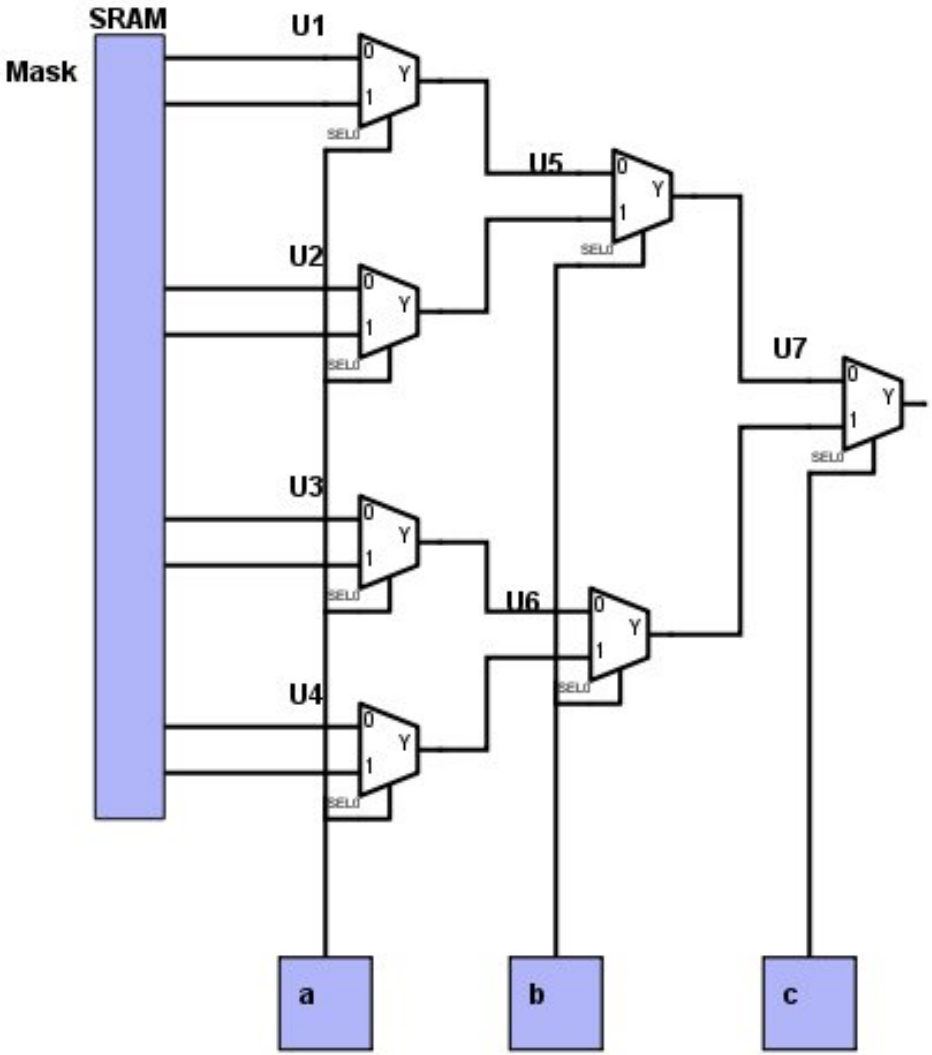

Figure: 3 stages of 2x1 MUX

- It is a table that ditermines what the output is for any given input
- A state-less interconnection of any number of gates (no feedback loops)
- Implemented *multiplexing* a combination of SRAM bits

FPGAs Structure

LUT Example

$$y = (a + b) \cdot c$$

a	b	c	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

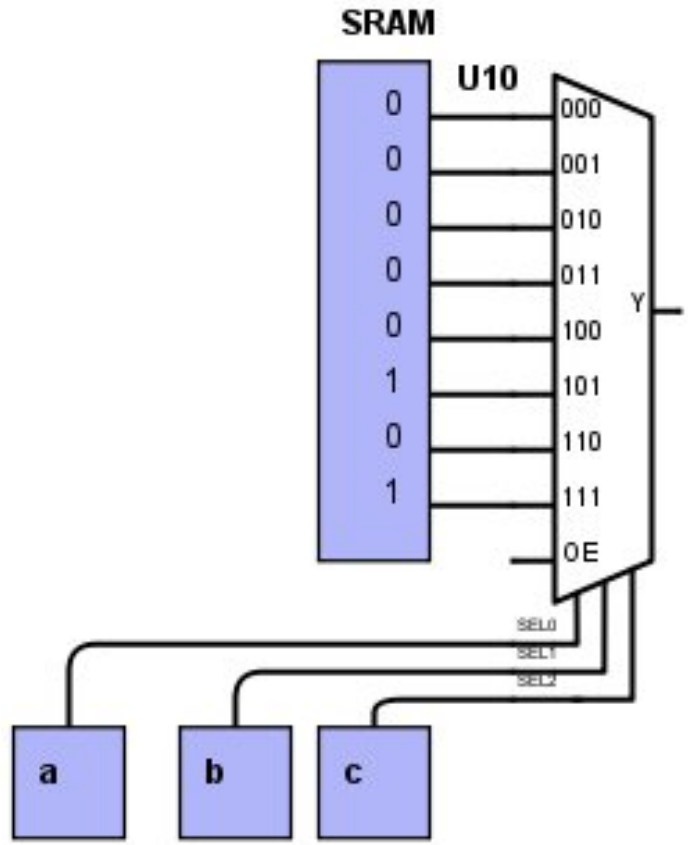

Figure: $y = (a + b) \cdot c$

FPGAs structure

BLE

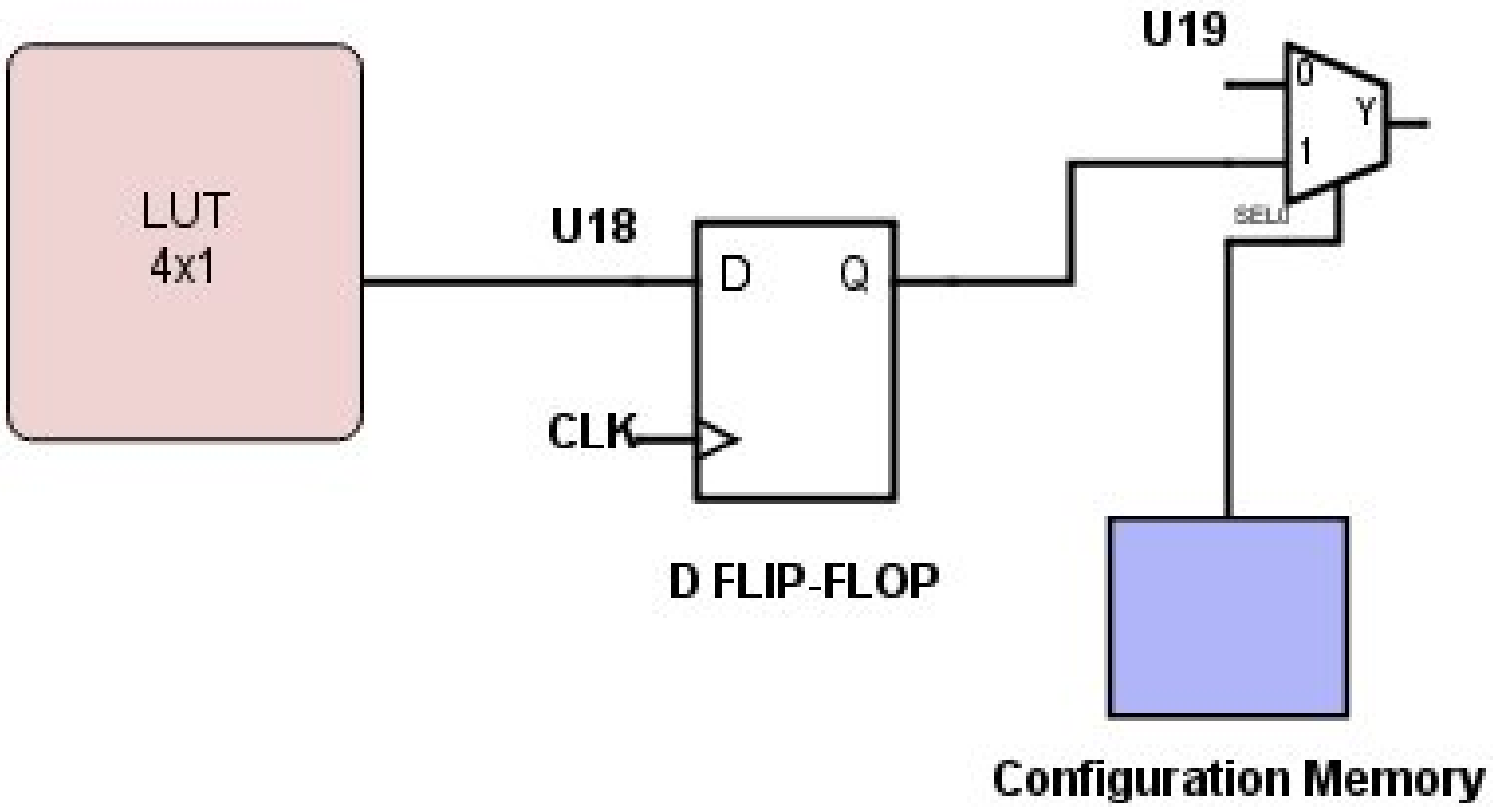

Figure: Basic Logic Element

FPGAs structure

Overview

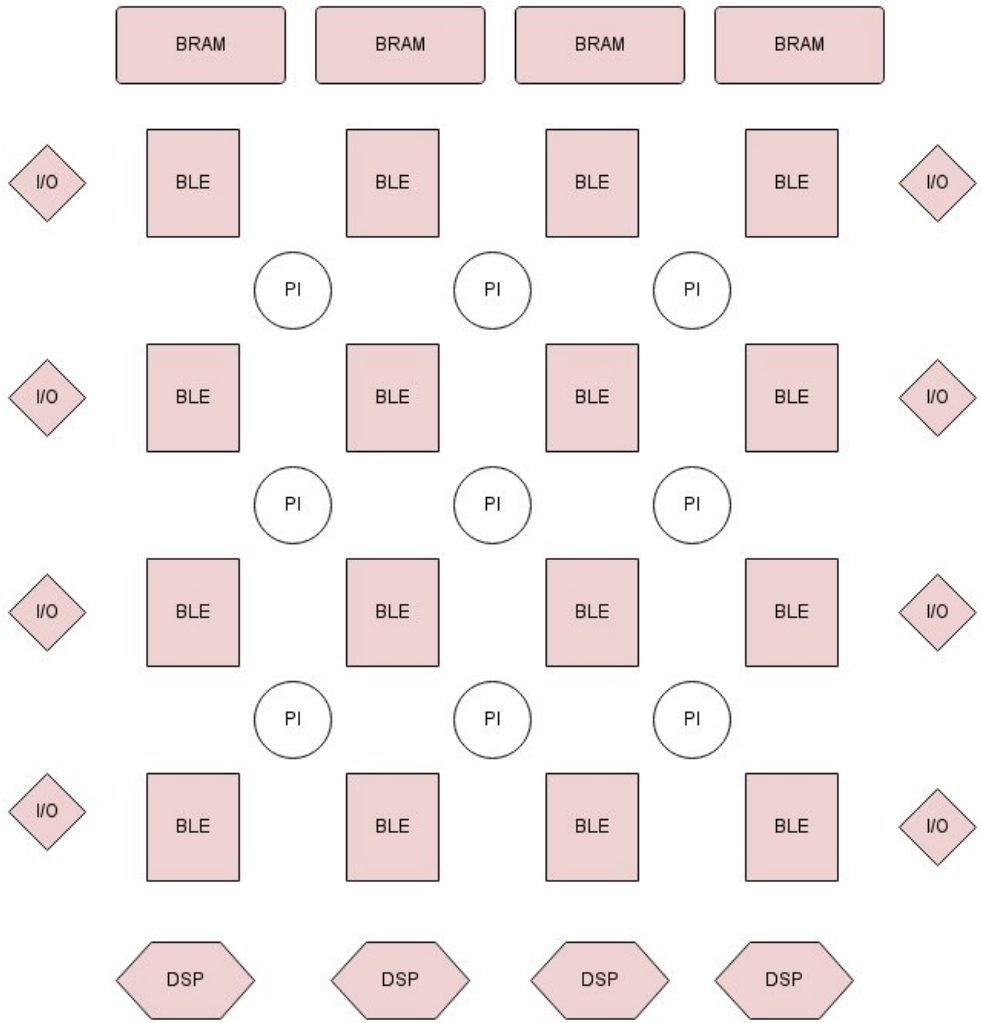

Figure: FPGAs Complete Overview