FPGAs, HLS Tools & Runtime Systems

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Overview

FPGAs structure

FPGAs Structure

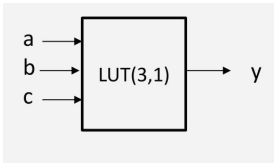

Figure: LUT

$$y = (a + b) \cdot c$$

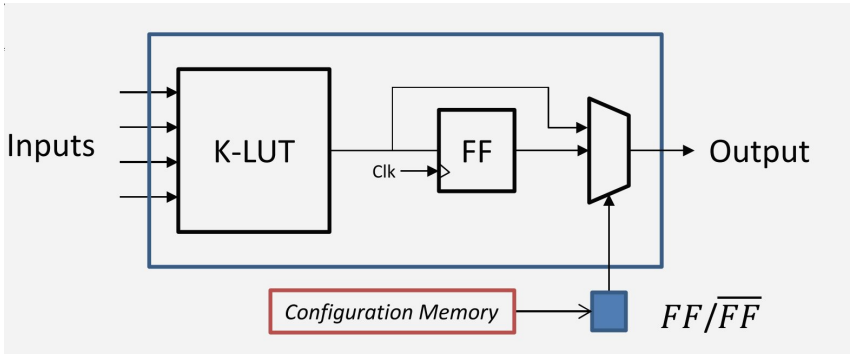

Figure: BLE

a	b	c	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

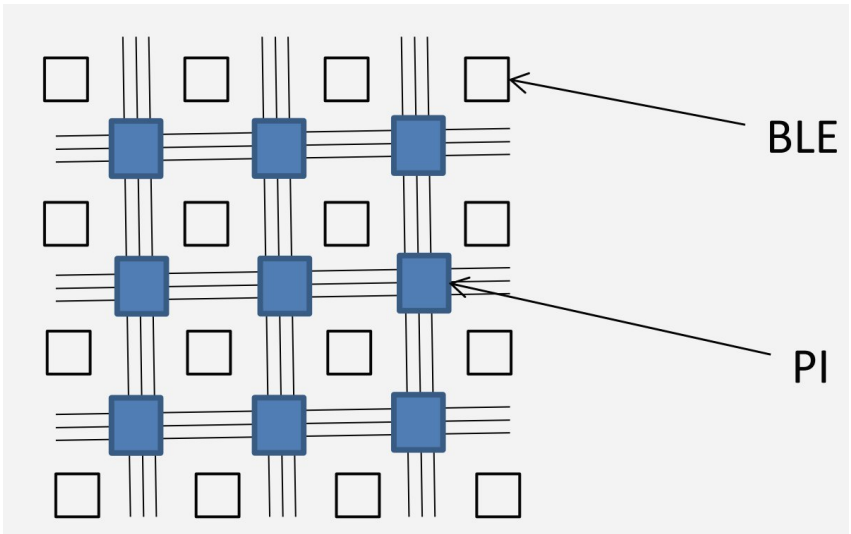

Figure: PI