

cellsim.uni

```
graph TD; Root[cellsim.uni] --- PPE[PPE]; Root --- SPE[SPE]; Root --- EIB[EIB.sim]; Root --- MM[Memory_multiport.sim]; Root --- DCP[default_configuration_parameters.h]; PPE --- Processor[Processor.sim]; PPE --- Cache[Cache.sim]; SPE --- spu[spu.sim]; SPE --- mfc[mfc.sim]; SPE --- ls[ls.sim];
```

PPE

Processor.sim

Cache.sim

SPE

spu.sim

mfc.sim

ls.sim

EIB.sim

Memory_multiport.sim

default_configuration_parameters.h