DEEPAK GANGADHARAN
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Research Interests

Scalable Design and Performance Analysis of IoT systems, Analysis and Scheduling of Real-Time Systems/Cyber-Physical Systems, Fault tolerant System Design

Education

- **PhD, Computer Science, National University of Singapore**
  Aug 2007 - Dec 2012
  - Topic: Quality-aware performance analysis for multimedia MPSoC platforms
- **BTech, Electrical and Communication Engineering, University of Kerala (India)**
  Oct 1998 - May 2002
  - Final Year Thesis: GTK-based implementation of remote command execution

Research Experience

- **Design of Infrastructure for Delivery of Update/Services to Connected Vehicles (Automotive IoT scenario)**
  - Developed an optimization strategy to derive optimal delivery of update/services to vehicles in motion via the edge infrastructure while considering objectives like bandwidth utilization, delivery time, etc.
  - Developed an incremental algorithm and a partitioned optimization approach to address the scalability issue in update/service delivery while considering multiple system objectives.
- **Timing Analysis for Deployment of Safety-Critical Applications on Automotive Platforms**
  - Developed specification framework and feasibility analysis tool for plug and play of automotive safety features
  - Proposed an end-to-end delay analysis technique for mixed critical applications on multiprocessor systems
  - Proposed a technique to schedule periodic tasks in a scheduling agnostic manner under data freshness constraint
- **Performance Analysis for Timing Predictability in Many-Core Systems**
  - Investigated methods to increase system utilization in many-core systems under timing constraints
  - Exploring run-time resource management techniques to achieve non functional properties in many-core systems
- **Automatic System Level Synthesis of Multi-ASIP platforms**

  - Team member of a European project **ASAM** that has the broad goal of developing tools for automatic synthesis of multi-ASIP architectures. Our group at DTU Informatics works on the specific objective of developing novel techniques for System level Platform Synthesis of multi-ASIP architectures.

- **Quality Driven Performance Analysis of Multimedia MPSoC Platforms**
  - Developed analytical models to analyze buffer and processing resource requirements in multimedia MPSoC Platforms with data loss using Network-Calculus based framework (**Work done during internship (Feb 2011 - April 2011) at Institute for Real-Time Computer Systems, Technical University of Munich chaired by Dr. Samarjit Chakraborty**)
  - Developed efficient prioritized data dropping scheme in multimedia streams to design resource efficient MPSoC platforms
  - Developed quality aware techniques for thermal management of video applications on MPSoC platforms
  - Investigated the impact of using Stochastic Network-Calculus based analysis framework towards the design of multimedia processing platforms

- **Efficient Test Case Classification Methodologies for Multimedia MPSoC Platforms**
  - Classification methods using novel multimedia workload models and performance model

- **Resource Efficient Mapping of Signal/Image Processing Algorithms to FPGAs/ASIC**
  - Reconfigurable area-efficient architectures for 2D convolvers
  - Study of Performance Characteristics of Parallel and Pipelined Implementations of FIR filters on FPGA

Teaching Experience

- **Instructor, IIIT Hyderabad**
  Spring 2020
  - Introduction to IoT

- **Teaching Assistant, School of Computer Engineering, Nanyang Technological University**
  Aug 2005 - April 2007
  - Digital Systems Lab

Professional Experience

- **Assistant Professor, IIIT Hyderabad**
  Sep 2019 - Now
  - Computer Systems Group

- **PostDoctoral Researcher, University of Pennsylvania**
  May 2015 - Aug 2019

  - Project: Plug and Play of Automotive Features and Connected Vehicles funded by Toyota ITC

- **PostDoctoral Researcher, University of Erlangen, Nuremberg**
  Sep 2013 - March 2015
  - Project: Invasive Computing
- **PostDoctoral Researcher, DTU Informatics, Technical University of Denmark**
  Jan 2012 - Jul 2013
  - Project: ASAM - Automatic Architecture Synthesis and Application Mapping
- **Research Assistant, School of Computer Engineering, Nanyang Technological University**
  Aug 2005 - April 2007
  - Project: Development of Reconfigurable Hardware Architectures for Selected Image/Signal Processing Algorithms
- **Senior Design Engineer, Conexant Systems Inc. (after acquiring Paxonet Communications Pvt. Ltd.**
  Aug 2004 - June 2005
  - Worked on RTL Design and Validation of various physical and data link layer protocols on ASICs and FPGAs
- **Design Engineer, Paxonet Communications Pvt. Ltd.**
  Aug 2002 - July 2004
  - Worked on RTL Design and Validation of various physical and data link layer protocols on ASICs and FPGAs

Publications

- JinHyun Kim, **Deepak Gangadharan**, Kyong Hoon Kim, Insik Shin and Insup Lee,"**Hierarchical Scheduling**,"*Book Chapter in Handbook of Real-Time Computing*, 2019
- Andreas Weichslgartner, Stefan Wildermann, **Deepak Gangadharan**, Michael Glass and Jürgen Teich, "**A Design-Time/Run-Time Application Mapping Methodology for Predictable Execution Time in MPSoCs**,"*ACM Transactions on Embedded Computing Systems (TECS)*, 2018
- **Deepak Gangadharan**, Oleg Sokolsky, Insup Lee, BaekGyu Kim, Chung-Wei Lin and Shinichi Shiraishi, "**Bandwidth Optimal Data/Service Delivery for Connected Vehicles via Edges**,"*In Proceedings of 11th IEEE Internation Conference on Cloud Computing (CLOUD)*, 2018
- Dagaen Golomb, **Deepak Gangadharan**, Sanjian Chen, Oleg Sokolsky and Insup Lee, "**Data Freshness Over-Engineering: Formulation and Results**,"*In Proceedings of 21st International Symposium on Real-Time Computing (ISORC)*, 2018 **(Best Paper Award)**
- JinHyun Kim, **Deepak Gangadharan**, Oleg Sokolsky, Axel Legay and Insup Lee, "**Extensible Energy Planning Framework for Preemptive Task**,"*In Proceedings of 20th International Symposium on Real-Time Computing (ISORC)*, 2017

- **Deepak Gangadharan**, JinHyun Kim, Oleg Sokolsky, BaekGyu Kim, Chung-Wei Lin, Shinichi Shiraishi and Insup Lee,"**Platform-based Plug and Play of Automotive Safety Features: Challenges and Directions**,"*In Proceedings of 22nd IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA), 2016*
- **Deepak Gangadharan**, Oleg Sokolsky, Insup Lee, BaekGyu Kim, Chung-Wei Lin, Shinichi Shiraishi, "**Platform-based Automotive Safety Features**,"*In SAE World Congress*, 2016
- Andreas Weichslgartner, **Deepak Gangadharan**, Stefan Wildermann, Michael Glass and Jürgen Teich, "**DAARM: Design-Time Application Analysis and Run-Time Mapping for Predictable Execution in Many-Core Systems**,"*In Proceedings of the 9th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, 2014
- **Deepak Gangadharan**, Ericles Sousa, Vahid Lari, Frank Hannig and Jürgen Teich, "**Application-driven Reconfiguration of Shared Resources for Timing Predictability of MPSoC Platforms**,"*In Proceedings of 48th Asilomar Conference on Signals, Systems and Computers*, 2014
- Ericles Sousa, **Deepak Gangadharan**, Frank Hannig and Jürgen Teich, "**Runtime Reconfigurable Bus Arbitration for Concurrent Applications on Heterogeneous MPSoC Architectures**,"*In Proceedings of the EUROMICRO Digital System Design Conference (DSD)*, 2014
- **Deepak Gangadharan**, Samarjit Chakraborty and Jürgen Teich,"**Quality-aware Video Decoding on Thermally-constrained MPSoC Platforms**, "*In Proceedings of the 25th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, 2014
- **Deepak Gangadharan**, Alexandru Tanase, Frank Hannig and Jürgen Teich,"**Timing Analysis of a Heterogeneous Architecture with Massively Parallel Processor Arrays**,"*DATE Workshop on Performance, Power and Predictability of Many-Core Embedded Systems (3PMCES)*, 2014
- Lech Jozwiak, Menno Lindwer, Rosilde Corvino, Paolo Meloni, Laura Micconi, Jan Madsen, Erkan Diken, **Deepak Gangadharan**, Roel Jordans et. al.,"**ASAM: Automatic Architecture Synthesis and Application Mapping**,"*Microprocessors and Microsystems - Embedded Hardware Design 37(8-C)*, 2013
- **Deepak Gangadharan**, Laura Micconi, Paul Pop and Jan Madsen,"**Multi-ASIP Platform Synthesis for Event-Triggered Applications with Cost/Performance Trade-offs**,"*In Proceedings of the 19th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA)*, 2013
- Laura Micconi, **Deepak Gangadharan**, Paul Pop and Jan Madsen,"**Multi-ASIP Platform Synthesis for Real-Time Applications**,"*In Proceedings of 8th IEEE International Symposium on Industrial Embedded Systems (SIES)*, 2013
- Balaji Raman, Ayoub Nouri, **Deepak Gangadharan**, Marius Bozga, Ananda Basu et. al.,"**Stochastic Modeling and Performance Analysis of Multimedia SoCs**,"*In Proceedings of International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS)*, 2013
- **Deepak Gangadharan**, Samarjit Chakraborty and Roger Zimmermann,"**Quality-Aware Media Scheduling on MPSoC Platforms**,"*In Proceedings of Design Automation and Test in Europe (DATE)*, 2013

- Lech Jozwiak, Menno Lindwer, Rosilde Corvino, Paolo Meloni, Laura Micconi, Jan Madsen, Erkan Diken, **Deepak Gangadharan**, Roel Jordans et. al.,"**ASAM: Automatic Architecture Synthesis and Application Mapping**,"*In Proceedings of the 15th Euromicro Conference on Digital System Design (DSD)*, 2012
- **Deepak Gangadharan**, Haiyang Ma, Samarjit Chakraborty and Roger Zimmermann,"**Video Quality-Driven Buffer Dimensioning in MPSoC Platforms via Prioritized Frame Drops**,"*In Proceedings of the 29th IEEE International Conference on Computer Design (ICCD)*, 2011
- Balaji Raman, Guillaume Quintin, Wei Tsang Ooi, **Deepak Gangadharan**, Jerome Milan and Samarjit Chakraborty, "**On Buffering with Stochastic Guarantees in Resource-Constrained Media Players**,"*In Proceedings of the 9th IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, 2011
- **Deepak Gangadharan**, Linh T.X. Phan, Samarjit Chakraborty, Roger Zimmermann and Insup Lee, "**Video Quality Driven Buffer Sizing via Frame Drops**,"*In Proceedings of the 17th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA)*, 2011
- **Deepak Gangadharan**, Samarjit Chakraborty, Roger Zimmermann,"**Fast Hybrid Simulation for Accurate Decoded Video Quality Assessment on MPSoC Platforms with Resource Constraints**,"*In Proceedings of the 16th Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2011
- **Deepak Gangadharan**, Samarjit Chakraborty, Roger Zimmermann,"**Fast model-based test case classification for performance analysis of multimedia MPSoC platforms**,"*In Proceedings of the 7th IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, 2009
- **G. Deepak**, R. Mahesh and A. Sluzek,"**Adaptable Area-Efficient Parallel Architecture for Grey and Color Image Convolvers**,"*In 8th International Symposium on Signals, Circuits and Systems (ISSCS)*, 2007
- **G. Deepak**, P. K. Meher and A. Sluzek,"**Performance Characteristics of Parallel and Pipelined Implementation of FIR Filters in FPGA Platform**,"*In 8th International Symposium on Signals, Circuits and Systems (ISSCS)*, 2007
- **G. Deepak**, R. Mahesh and A. Sluzek,"**Design of an Area-Efficient Multiplierless Processing Element For Fast Two Dimensional Image Convolution**,"*In 13th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2006

Student Mentoring

- **PhD**
  UPenn: Jan 2016 - Jan 2017
  - Dagaen Golomb - Topic: Data Freshness Formulation
- **Bachelor's**
  UPenn: Feb 2018 - May 2018
  - Miku Fujita - Topic: Scalable Data/Service Delivery to Connected Vehicles via Edges
  - Stephanie Tang - Topic: Vehicular Edge Computing Simulator

- **Dual Degree**
  IIIT Hyderabad
  - Akshaj Gupta - Topic: Scalable Data/Service Delivery to Connected Vehicles via Edges (Jan 2020-Now)
  - Joseph John Cherukara - Topic: Scalable Data/Service Delivery to Connected Vehicles via Edges (May 2020-Now)
  - Sridhar M - Topic: Data Freshness Formulation (May 2020-Now)

Honors and Awards

- Invited to NSF funded Early Career Researcher Workshop organized by Computing Community Consortium
- Best Paper Award at ISORC 2018
- Awarded Research Scholarship for Graduate Study by National University of Singapore.
- Awarded the prestigious National Talent Search Examination (NTSE) Scholarship from the National Council for Educational Research and Training (NCERT), India.

Professional Service

- Session Chair - IEEE Cloud 2018 Regular Paper Session
- Student Consortium Chair - IEEE BigMM 2020
- Program Committee - MOMAC 2016, IEEE Cloud Work-in-Progress 2018, IEEE BigMM 2020, IEEE MASS 2020
- Conference Reviewer - IEEE CLOUD 2018, RTSS 2017, EMSOFT 2017-2018, DAC 2016, DAC 2013-2014, DATE 2013-2017, RTAS 2014, ASAP 2014, CODES+ISSS 2014, SCOPES 2014, ESTIMedia 2014, MMSP 2011
- Expert Reviewer - EMSOFT 2014
- Journal Reviewer - VLSI Design, Journal of Multimedia, ACM TECS, IEEE TCAD, ACM Computing Surveys, IEEE Computer

Skills

- **Operating Systems:** Windows, Linux
- **Programming Languages:** Proficient in C, C++, VHDL, Verilog
- **Tools:** Matlab, CPlex, Simplescalar, Xilinx ISE, Leonardo Spectrum, Precision Synthesis, Modelsim and Synopsys

References

- Furnished upon request