EMI behavior of Copper Areas on Outer Layers of PCBs.

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ABSTRACT – **In the design of multilayer printed cicuit boards (PCBs), it is common that copper areas are introduced on the outer layers of the PCB as shown in figure 1. There are different reasons for the use of these "area–fills". Two of them are: an enhanced EMC–performance due to a reduced crosstalk, and secondly, to gain a uniformly coverage of the layer with copper to avoid an underetching of the traces.**
Nevertheless, PCB designers should consider that these area–fills have the potential to create serious EMC hazards. For a better understanding of these copper areas, several test structures were examined using a full wave field solver. Depending on the geometry, different resonating structures can be detected and explained. From these results, design guidelines are derived.

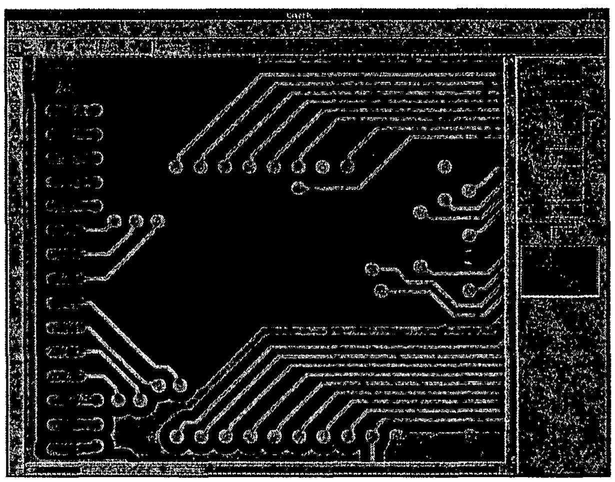

Figure 1: Typical copper filled area on a PCB

Introduction

Area–fills on outer layers of PCBs can have a significant impact on the radiation behavior of the complete design. Depending on the geometry and the connectivity to the reference potential (e.g. ground), a resonating structure can be formed by the copper areas. Within this contribution different structures are examined using the Method of Moment (MoM) [2] solver COMORAN [1]:

1. A floating copper area excited by an adjacent microstrip line, and
2. an area–fill connected with several vias on different locations to ground.

These configurations are examined concerning their spectral impedances and radiated electrical field strengths. The results are verified and explained using equivalent circuits representing the structure.

Geometrical setup and numerical results

Figure 2 shows the studied structure. This simulation model is chosen much simpler than the example shown in figure 1. From the results obtained using the simple model, the general behavior of copper areas can be understood and explained much easier as it is possible for more complicated, practical structures. The drawn conclusions are valid for practical configurations as well.

Floating copper areas

In the first case study, the shown vias are omitted, therefore the copper plane has floating potential. The structure is

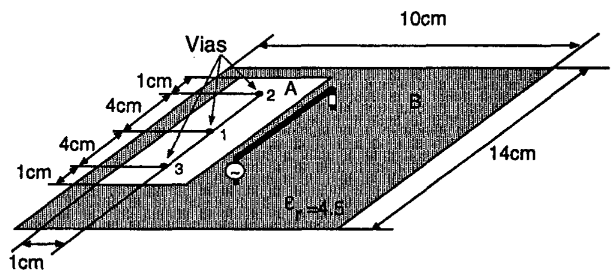

Figure 2: Microstrip line above a ground plane (B), close to an area–fill (A)

excited by a microstrip line, which is driven by a voltage source placed at one end of the trace and is loaded by a 360 Ω resistor. The distance between signal trace and the floating plane A is twice the distance between the planes of $d = 1$ mm. Therefore, the signal behavior of the trace is almost not affected by the neighbored plane A. But due to the capacitive coupling, a current distribution is generated within the floating copper area. This current distribution becomes resonant when the edge length of the plane l is equal to the half wavelength of the exciting signal

$$l = \lambda/2 = c_0/2f\sqrt{\varepsilon_r} \quad , \tag{1}$$

where c_0 is the free space velocity of light.
In the given case of a 10 cm long edge, the resonant frequency results in $f_0 = 707$ MHz. In figure 3, where the real part of the current distribution on the area–fill is indicated by arrows, the halfwave resonance can clearly be seen.

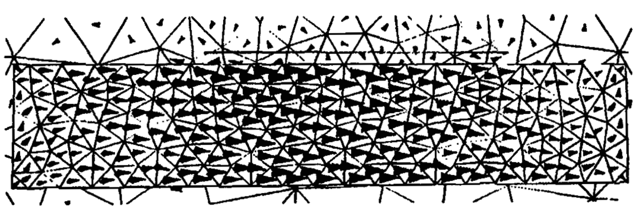

Figure 3: Real part of the current distribution on the floating plane

This resonating behavior must have a strong impact on the radiated electrical field, since the resonating structure acts as a dipol antenna. To proove this, the electrical field strength $\vec{E}$ is computed on a sphere in 3 meter distance from the center of the reference plane. The maximum value on the sphere is compared to a reference case without area–fill in figure 4 within a frequency range up to 1 GHz. The ratio of both cases (= difference in dB) is as well shown by the solid line[1].

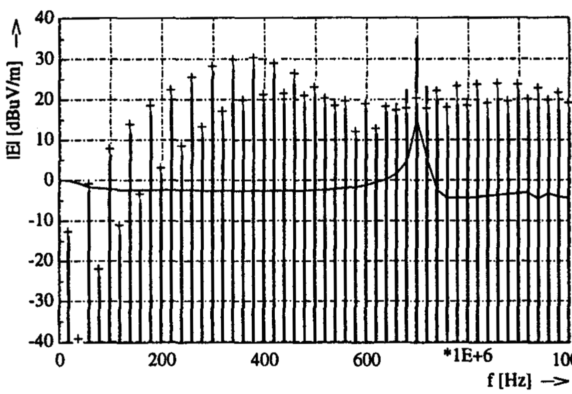

Figure 4: Radiated electrical field strength @ 3m distance (ǁǁ): with floating plane A; (+): no plane A; (—) difference in dB

Both cases show almost the same behavior, except in the frequency range around 700 MHz, where the floating plane is in $\lambda/2$–resonance. Here, the radiated electrical field strength is drastically increased (up to 16 dB more!), due to the dipol behavior of the floating plane.

[1]The absolute values are depending on the exciting signal and are not of interest here.

Grounded area fills

In order to avoid this antenna behavior of area–fills, they have to be connected to the reference plane by vias. The following examinations show the impact of different numbers of vias between plane A and B as depicted in figure 2.

Analog to the floating case, the electrical field strength is computed for three different numbers of connecting vias. The first connecting via is placed at position "1" in figure 2, the second is added at position "2", and finally, the third one at position "3".
The results are shown in figure 5, where the ratios of the electrical field strength relative to the case without area–fill are plotted vs. frequency.

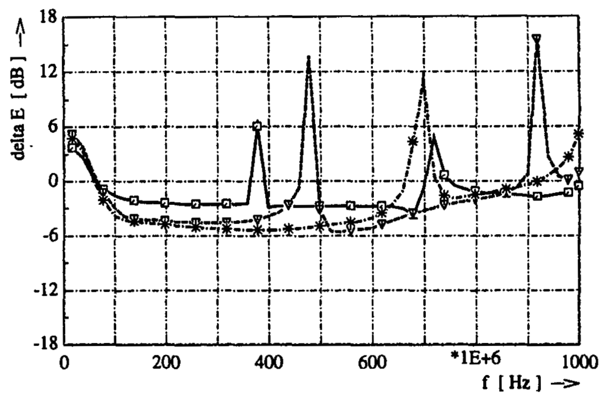

Figure 5: Ratio of the electrical field strength (ΔE in dB) to the reference case without plane A (□):1 via; (▽): 2 vias; (∗): 3 vias

Quite remarkable are the distinct peaks at several frequencies, which are indicating an increased radiation level up to 18 dB! Examining these results more detailed, the $\lambda/2$–resonance around 700 MHz can still be observed for the 1–via case but with reduced amplitude. A larger peak occurs at 380 MHz, which can only be caused by the connecting via. By adding more vias, this additional peak is shifted to higher frequencies.

In order to gain more insight in the behavior of the connected area–fill structure, a slightly different configuration is examined: a voltage source is placed between area–fill and reference plane at postion "1" in figure 2. The impedance $Z(f)$ of the structure seen by this source can now be computed. The formerly used excitation – the microstrip line – is omitted for this computation.

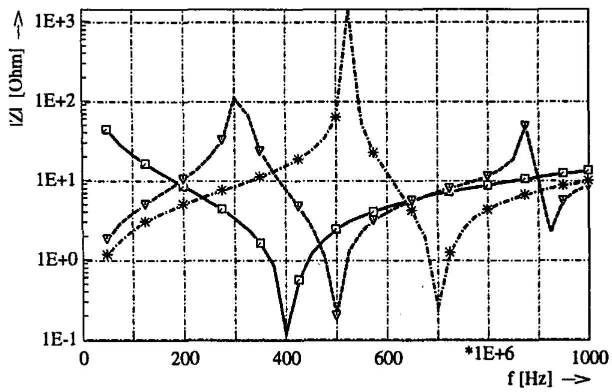

Figure 6: Impedance $|Z|$ vs. frequency
($\square$):1 via; (∇): 2 vias; ($*$): 3 vias

Due to the inductive behavior of the connecting vias, a resonating LC-circuit is created now, whereby the capacitor is formed by the interplane capacitance between plane A and B. The resonance frequency of this circuit can be approximated within the quasi-statical frequency range by

$$f_0 = 1/(2\pi\sqrt{LC}) \quad \text{with} \tag{2}$$
$$C = \varepsilon_0\varepsilon_r A/d \tag{3}$$

and $L' = 1.85$ nH/mm for a single via[2]. Since the resonance frequency f_0 is already exceeding the quasi-statical frequency range, equation 2 can only be used to clearify the structural behavior and not to compute the exact value of the resonance frequency. For this purpose, the numerical solution is suited better.

In order to see the impact of the number of the connecting vias, the impedance $|Z(f)|$ is plotted in figure 6 for three different cases: one connecting via up to 3 vias. By introducing more vias, the resonance frequency is shifted towards higher frequencies, because the circuit inductance is decreased by the "parallel" vias.

The peak values of the radiated electrical field strength shown in figure 5 are related to the local minima of the impedance $|Z|$. In these cases, the LC-circuit is in resonance and the currents magnitude increases drasticly, leading to a high level of radiation.

Using practical excitation signals (e.g. a trapezoidal clock signal), whose spectral power contribution becomes smaller at higher frequencies (-40 dB/decade [4, 3]), the shift of resonance frequencies towards higher values by adding more vias can help to reduce the amplitude of the radiated electrical field strength.

[2]The value for this via was derived from an additional COMORAN computation

Via placement strategies

Within the quasi-statical frequency range, the positioning of the vias will not affect the resonance frequencies of the above described LC-circuits. At higher frequencies, there will be an impact from the local arrangement of the connecting vias. Figure 7 shows the studied via configurations on the area-fill. The reference plane remains unchanged in all cases.

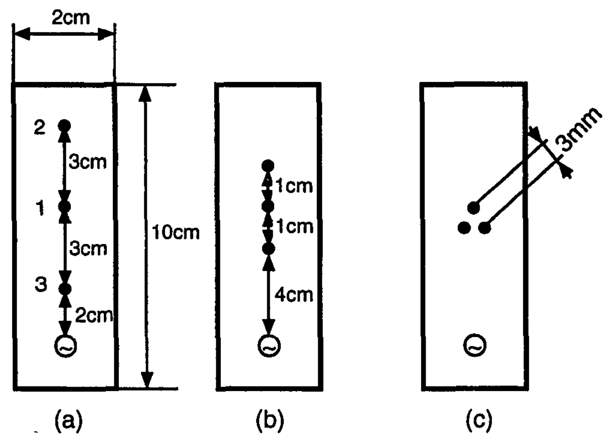

Figure 7: Studied via placement cases:
(a) wide distributed; (b): narrow distributed;
(c): grouped

Again, the input impedance Z(f) seen by the exciting voltage source is computed using COMORAN for the three studied cases. The results are plotted in figure 8. As expected, the impedance shows only small deviations within a frequency range up to 400 MHz between the three cases.

Within the high frequency range, the peak frequencies are shifted to smaller frequencies with decreasing distance of the vias, due to an increased mutual inductance of the vias. Furthermore, higher order resonances occur in the studied frequency range.

These results are supporting the well known design guideline: "spread vias all over the area-fill in a distance of 1 in". The via inductance can be kept as low as possible, which shifts the resonance frequencies to higher regions in the spectrum.

On the other hand, up to now, there is no positive effect visible due to the area-fills. In the best case, the generated resonances can be shifted to a frequency range, where the exciting signal energy is already very small and therefore, the bad influence on the EMI-behavior can be neglected.

In the following final section, one potential advantage of the use of area-fills is studied.

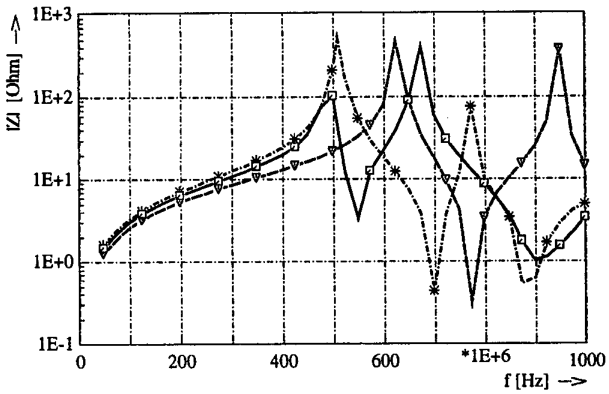

Figure 8: Impedance $|Z|$ depending on the via placement: (∇): 3 vias wide distributed; ($*$): 3 vias narrow distributed; ($\square$):3 vias grouped at the center;

Impact on the power bus

Because lumped decoupling capacitors are not efficient enough at higher frequencies above some hundred megahertz, the interplane capacitance between GND and POWER layers is used to provide a low impedance of the power supply system.

Area-fills may increase the capacitance of the power bus, and therefore reducing its impedance. Figure 9 shows two possible cross-sections of the PCBs power bus. In the right case, the area-fill is connected to the lower reference plane. The area-fill adds some capacitance with respect to the neighbored reference plane of opposite potential. The left case shows the area-fill connected to the directly neighbored plane. Therefore, no additional capacitance is build up here, since both neighbored planes have the same potential.

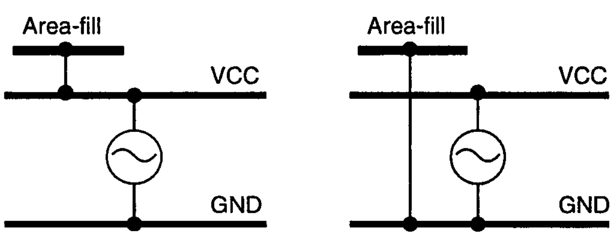

Figure 9: Two possible connections of area-fills to the power supply system

These considerations of "capacitance" are only valid in the quasi-statical frequency range. In order to show the impact on the impedance for higher frequencies as well, the previous simulation model is extended by an additional reference plane directly below plane "B" in a distance of 1 mm.

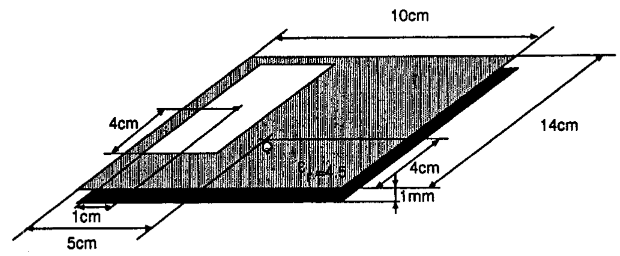

Figure 10: Extended configuration with 2 reference plane and area-fill

The input impedance of the two configurations sketched in figure 9 is computed. The excitation is placed on a via between the two reference planes at the source position of the first studied configuration (figure 2). The area-fill is connected by a via in the center of the area-fill, as shown in figure 10.

In figure 11 the input impedance $|Z|$ seen by the exciting source is plotted vs. frequency for the two different layer stack-ups. Additionally, the impedance is plotted for the two potential planes only, as a reference.

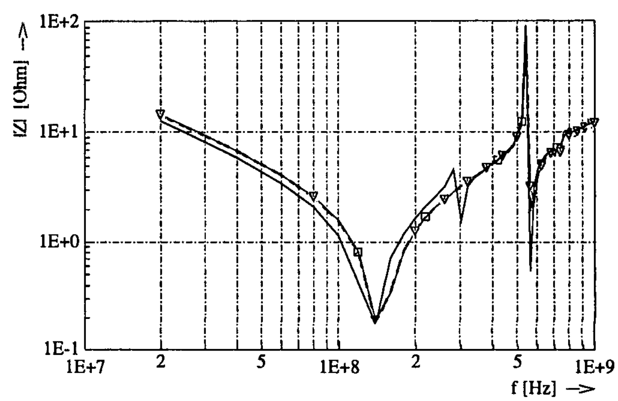

Figure 11: Input Impedance $|Z|$ of the power supply system ($\square$): no area-fill; (∇): left case, (_): rigth case

The large peak frequency at 540 MHz in figure 11 results from the planes halfwave resonance, where the longer edge (l=14cm) becomes resonant as shown in figure 12. The maximum value indicated by the white color, is reached in the proximity of the voltage source. Besides this peak value, a resonating current distribution can be observed with its maximum at the center of the resonating edge and minimal values at the borders.

Because of the location of the feeding point in 4 cm distance from the edge, the resonating length is virtually shortened, leading to a slightly higher resonant frequency as derived from equation (1). Since this resonance is not affected by the area-fill, all three curves in figure 11 show the same behavior here.

Figure 12: Magnitude of the current distribution on the reference planes @ 540 MHz

In a frequency range up to 150 MHz, the area–fill can decrease the impedance of the power bus from 14Ω down to 12Ω accordingly to its additional capacitance, if connected correctly. From equation (3), the capacitance of the two reference planes can be determined to 558 pF, resulting in an impedance of 14Ω at $f = 20$ MHz. From the reduced impedance value, the additional capacitance can be derived to be 76 pF, which can also be verified by equation (2).

This effect vanishes if the area–fill is connected directly to the neighbored plane. Both curves in figure 11, the □–marked and the reference curve ($\bigtriangledown$), are almost identical over the whole frequency range.

Around 300 MHz, an additional resonance frequency can be observed in the solid line of figure 11. Considering an equivalent circuit of the structure (shown in figure 13, this resonance can be explained as a parallel LC–resonance circuit, build up by the two capacitors, connected by the inductor of the via.

The pole frequency of this circuit can be derived analytically

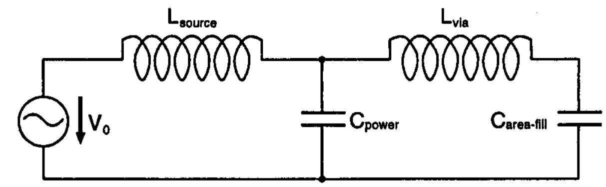

Figure 13: Equivalent circuit of the power bus configuration with area–fill

from the input impedance of the circuit:

$$f_0 = \frac{1}{2\pi} \cdot \sqrt{\frac{C_{power} + C_{area-fill}}{C_{power} \cdot C_{area-fill} \cdot L_{via}}} \quad \text{with} \quad (4)$$

$$C_{power} = 558 \text{ pF}$$
$$C_{area-fill} = 76 \text{ pF}$$
$$L_{via} = 3.7 \text{ nH}$$

With the given values, equation (4) results in a resonance frequency of 320 MHz, which is in good correlation to the simulation result shown in figure 11.

Adding more vias will reduce the circuit inductance, as described already above. Therefore, the resonance frequency will be increased. The impact on the power bus impedance is show in figure 14. All three cases have almost the same impedance $Z(f)$, except the resonance frequency of the parallel LC–circuits.

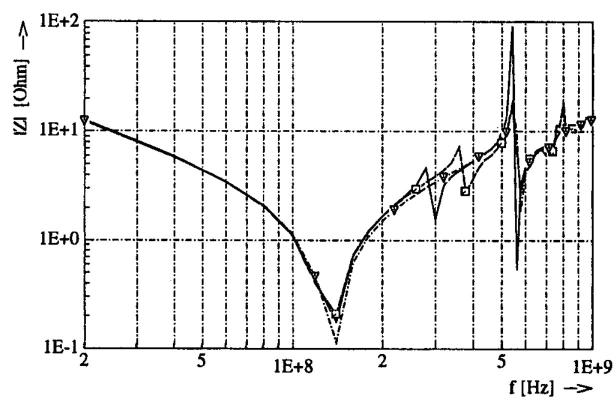

Figure 14: Input Impedance $|Z|$ of the power supply system (—): 1 via; (□): 2 vias; ($\bigtriangledown$): 3 vias

Extrapolating from these case studies to a practical PCB with several (hundreds of) area–fills with different sizes and shapes, a quite complex system of parallel LC–circuits is formed by the area–fills. Every new LC–circuit will generate an additional resonance frequency, which can cause not only extrem impedance values, but also high radiation levels at these frequencies.

Conclusion

Floating copper areas, or area–fills, on outer layer of PCBs can act as very effective dipole antennas when the exciting signal frequency comes close to the resonant frequency of these planes. If their largest extend is very small, their resonant frequencies are accordingly high and may be out of the interesting frequency range. Nevertheless, it is preferable not to have any floating planes on the PCB.

Grounded copper areas are acting as resonant circuits. Their resonant frequency is determined by the capacitance of the copper area to the reference plane and the inductance of the connecting vias. By introducing a large number of vias, the inductance is decreased and therefore, the resonance frequency can be out of the interesting frequency range, again. But too many vias can also create additional problems, e.g. by blocking routing paths on other layers and increasing production costs.

As shown in the last part of this contribution, the idea of using area–fills in order to enhance the power bus impedance can also generate problems due to additional resonances. Wrong connected area–fills do not even contribute to the capacitance of the power supply system.

From the EMI point of view, area–fills on outer layers of PCBs have to be avoided, whenever it is possible.

References

[1] Bücker, Markus. Enhanced Numerical Integration Technique. *IEEE 1999 International Symposium on Electromagnetic Compatibility, Seattle, Washington, USA*, pages 328–333, August 2–6 1999.

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[3] Ott, Henry W. *Noise Reduction Techniques in Electronic Systems.* John Wiley & Sons, INC, New York, Chichester, Brisbane, Toronto, Singapore., 1988.

[4] C.R. Paul. *Introduction to Electromagnetic Compatibility.* John Wiley & Sons, INC., 1992.