Schematic: SAMA5D2B-XULT

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11	Flash & Audio & LED
12	Ethernet_10/100M
13	SD & eMMC
14	EDBG
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Revision History

DATE	REVISION	DESCRIPTION
22 Sep 2015	SAMA5D2-XULT RevA-150922	Official Release
17 Mar 2016	SAMA5D2B-XULT RevB-160316	Official Release
10 Jul 2017	SAMA5D2C-XULT RevC-170710	Official Release

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A	RevA	XinJQ	22-Sep-15	XXX	XX-XXX-XX
A	INIT EDIT	XinJQ	21-May-15	XXX	XX-XXX-XX

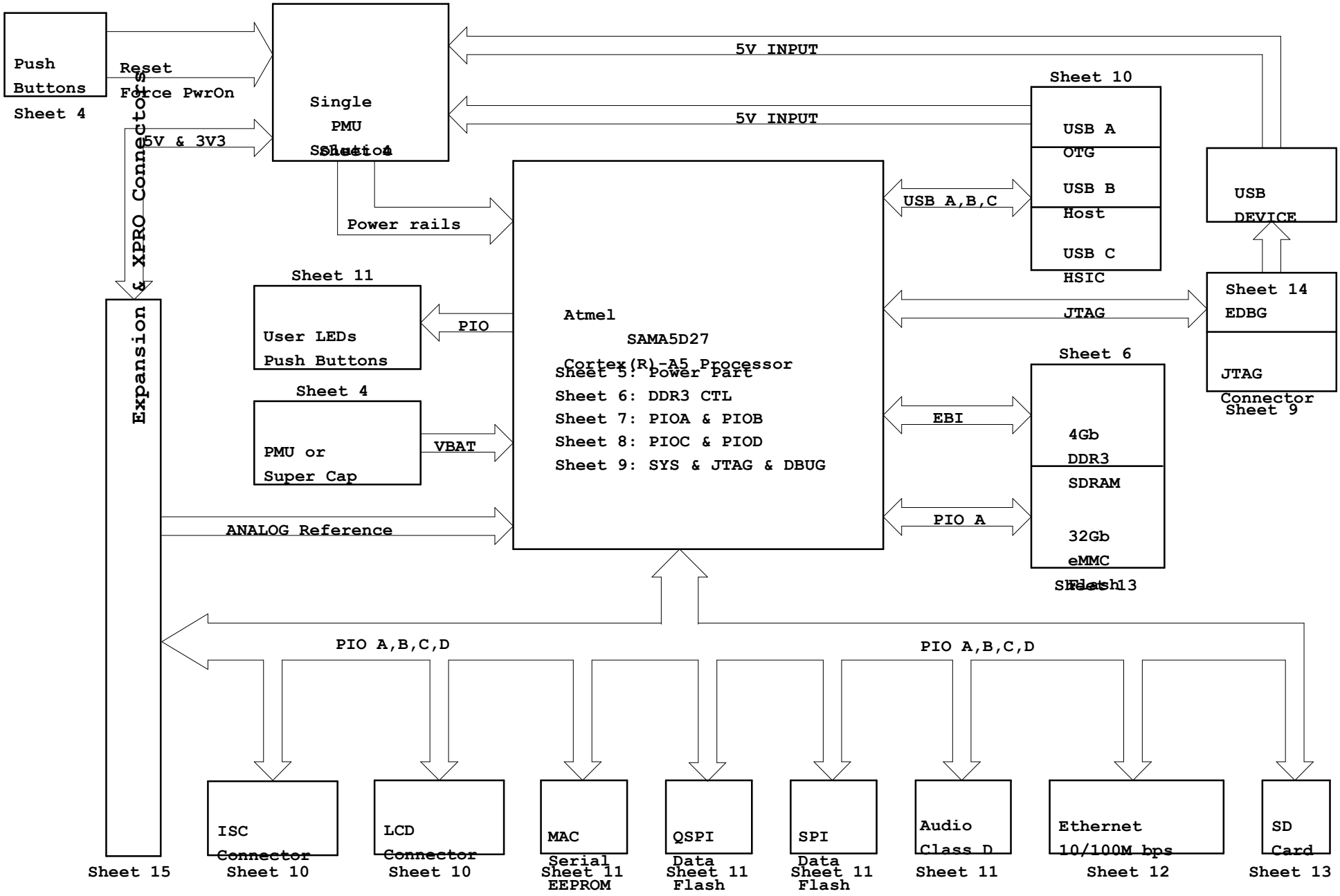
SAMA5D2C-XULT

Title & Revision History

SCALE 1/1

REV C

SHEET 1/12



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SAMA5D2C-XULT
Block Diagram
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PIO Muxing & Jumper setting

LCD	
ID_SYS	1
GND	2
NC	3
NC	4
LCDDAT2	5
LCDDAT3	6
GND	7
LCDDAT4	8
LCDDAT5	9
LCDDAT6	10
LCDDAT7	11
GND	12
NC	13
NC	14
LCDDAT10	15
LCDDAT11	16
GND	17
LCDDAT12	18
LCDDAT13	19
LCDDAT14	20
LCDDAT15	21
GND	22
NC	23
NC	24
LCDDAT18	25
LCDDAT19	26
GND	27
LCDDAT20	28
LCDDAT21	29
LCDDAT22	30
LCDDAT23	31
GND	32
LCDPCK	33
LCDVSYNC	34
LCDHSYNC	35
LCDDEN	36
SPI1_SPCK/AD0_XP	37
SPI1_MOSI/AD1_XM	38
SPI1_MISO/AD2_YP	39
SPI1_NPCS0/AD3_YM	40
LCDDISP	41
TWD1	42
TWCK1	43
IRQ1	44
IRQ2	45
LCDPWM	46
NRST	47
VCC	48
VCC	49
GND	50

PIOA	USAGE	PIOA	USAGE	PIOB	USAGE	PIOB	USAGE	PIOC	USAGE
PA0	SDHC0_CK	PA16	SPI0_MISO/EXP	PB0	LED_BLUE/LCD_ID	PB16	ETH_GRXDV	PC0	ISC_D6/EXP/XPRO
PA1	SDHC0_CMD	PA17	SPI0_CS0/EXP	PB1	CLASSD_R0	PB17	ETH_GRXER	PC1	ISC_D7/SPI1_SPCK/EXP
PA2	SDHC0_DAT0	PA18	SDHC1_DAT0/EXP	PB2	CLASSD_R1	PB18	ETH_GRX0	PC2	ISC_D8/SPI1_MOSI/EXP
PA3	SDHC0_DAT1	PA19	SDHC1_DAT1/EXP	PB3	CLASSD_R2	PB19	ETH_GRX1	PC3	ISC_D9/SPI1_MISO/EXP
PA4	SDHC0_DAT2	PA20	SDHC1_DAT2/EXP	PB4	CLASSD_R3	PB20	ETH_GTX0/EXP	PC4	ISC_PCK/SPI1_NPCS0/EXP
PA5	SDHC0_DAT3	PA21	SDHC1_DAT3/EXP/XPRO	PB5	LED_GREEN/EXP/XPRO	PB21	ETH_GTX1/EXP	PC5	ISC_VSYNC/EXP
PA6	SDHC0_DAT4	PA22	SDHC1_CK/QSPI0_SCK/EXP	PB6	LED_RED/EXP/XPRO	PB22	ETH_GMDC/EXP	PC6	ISC_HSYNC/EXP
PA7	SDHC0_DAT5	PA23	QSPI0_CS/EXP/XPRO	PB7	LCD_IRQ1	PB23	ETH_GMDIO/EXP	PC7	ISC_MCK/EXP
PA8	SDHC0_DAT6	PA24	QSPI0_IO0/EXP/XPRO	PB8	LCD_IRQ2	PB24	ISC_D10/EXP	PC8	PMIC_LBO/EXP
PA9	SDHC0_DAT7	PA25	QSPI0_IO1/EXP	PB9	USER_PB/EXP/XPRO	PB25	ISC_D11/EXP	PC9	ETH_INT
PA10	SDHC0_RSTN	PA26	QSPI0_IO2/EXP	PB10	USBB_EN5V/EXP/XPRO	PB26	ISC_D0/EXP	PC10	LCD_DAT2/EXP
PA11	SDHC0_VDDSEL	PA27	QSPI0_IO3	PB11	ISC_RST/EXP	PB27	ISC_D1/EXP	PC11	LCD_DAT3/EXP
PA12	PMIC_CHGLEV	PA28	SDHC1_CMD	PB12	ISC_PWD/EXP	PB28	ISC_D2/EXP/XPRO	PC12	LCD_DAT4
PA13	SDHC0_CD	PA29	USBB_OVCUR	PB13	PMIC_IRQ	PB29	ISC_D3/EXP/XPRO	PC13	LCD_DAT5
PA14	SPI0_SPCK/EXP	PA30	SDHC1_CD	PB14	ETH_GTXCK	PB30	ISC_D4/EXP	PC14	LCD_DAT6
PA15	SPI0_MOSI/EXP	PA31	USBA_VBUS Detection	PB15	ETH_GTXEN	PB31	ISC_D5/EXP/XPRO	PC15	LCD_DAT7

PIOC	USAGE	PIOD	USAGE	PIOD	USAGE
PC16	LCD_DAT10	PD0	LCD_PCK	PD16	JTAG_TDO
PC17	LCD_DAT11	PD1	LCD_DEN	PD17	JTAG_TMS
PC18	LCD_DAT12	PD2	DBGU_URXD1	PD18	XPRO
PC19	LCD_DAT13	PD3	DBGU_UTXD1	PD19	LCD_XP/EXP
PC20	LCD_DAT14	PD4	LCD/EEP/ISC/EXP_TWD1	PD20	LCD_XM/EXP
PC21	LCD_DAT15	PD5	LCD/EEP/ISC/EXP_TWCK1	PD21	LCD_YP/PMIC_TWD0/EXP
PC22	LCD_DAT18	PD6	EXP	PD22	LCD_YM/PMIC_TWCK0/EXP
PC23	LCD_DAT19	PD7	XPRO	PD23	EXP
PC24	LCD_DAT20	PD8	XPRO	PD24	EXP
PC25	LCD_DAT21	PD9	XPRO	PD25	EXP/XPRO
PC26	LCD_DAT22/EXP	PD10	XPRO	PD26	EXP/XPRO
PC27	LCD_DAT23/EXP	PD11	XPRO	PD27	EXP/XPRO
PC28	LCD_PWM	PD12	EXP/XPRO	PD28	EXP/XPRO
PC29	LCD_DISP	PD13	EXP/XPRO	PD29	EXP/XPRO
PC30	LCD_VSYNC	PD14	JTAG_TCK	PD30	EXP
PC31	LCD_HSYNC	PD15	JTAG_TDI	PD31	EXP

JUMPER DESCRIPTION		
PART	DEFAULT	FUNCTION
JP1	OPEN	Disable EDBG
JP2	OPEN	Disable Debug
JP3	CLOSE	I VDD_3V3_LP Measurement
JP4	CLOSE	I VDDCORE Measurement
JP5	CLOSE	I VDDISC+VDDIOP0/1/2 Measurement
JP6	CLOSE	I VDDBU Measurement
JP7	CLOSE	I VDDIODDR_MPU Measurement
JP8	CLOSE	I VDD_5V_IN Measurement
JP9	OPEN	Disable CS of SPI&QSPI&eMMC Memory

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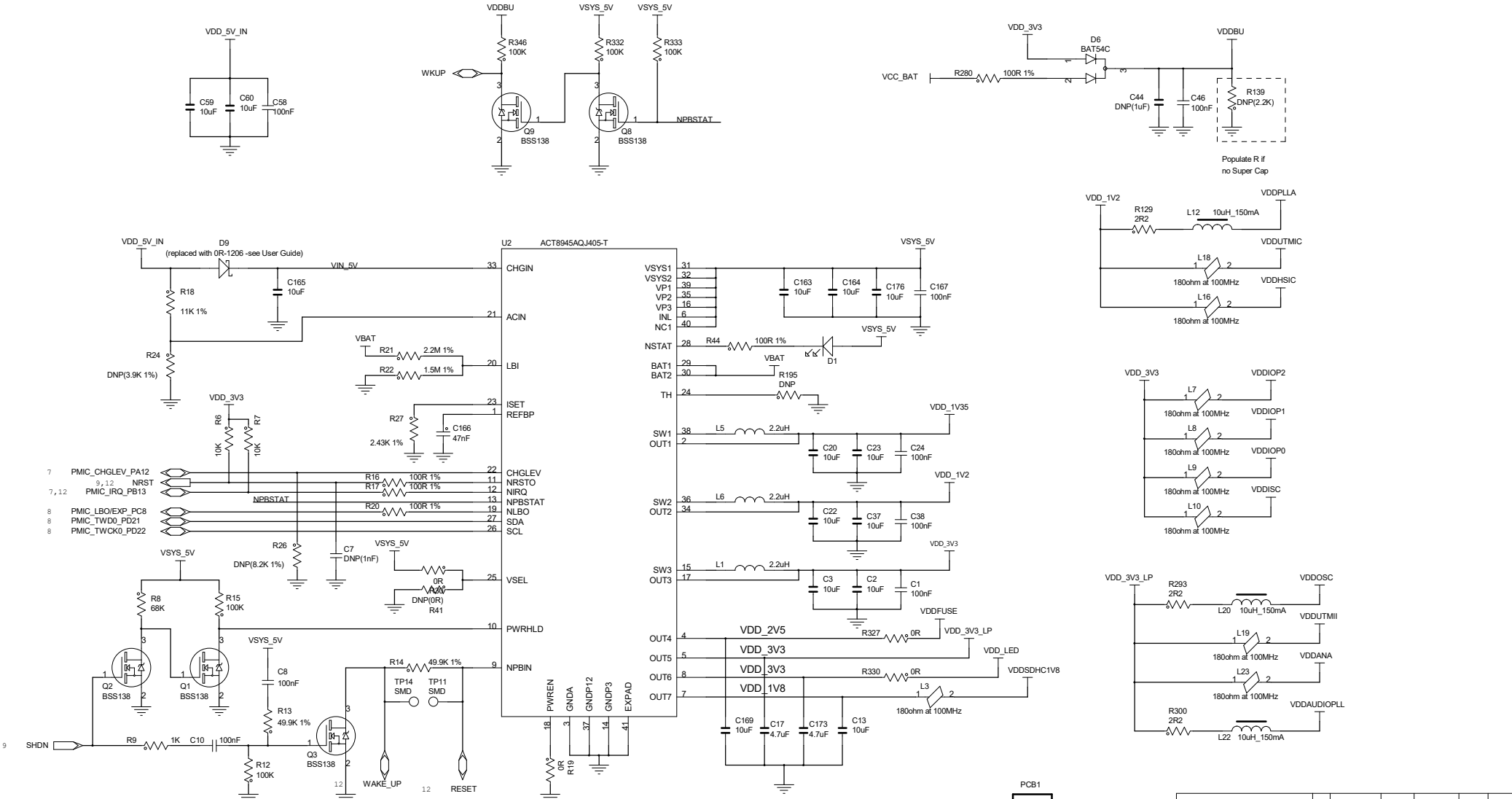
SAMA5D2C-XULT

PIO Muxing

SCALE 1/1

REV. C

SHEET 3/12



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SAMA5D2C-XULT

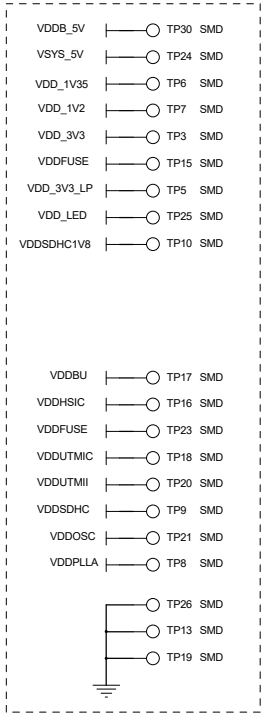
Power Supply

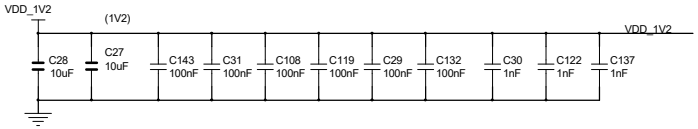
SCALE 1/1

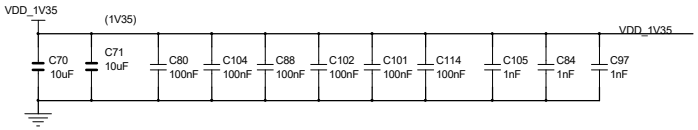
REV. C

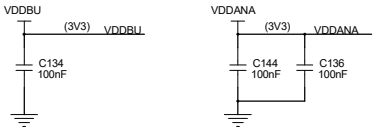
SHEET 4/12

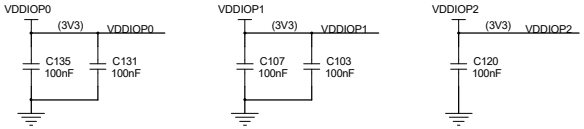
POWER TEST POINTS

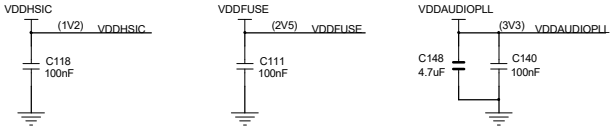


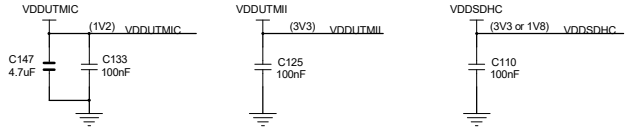


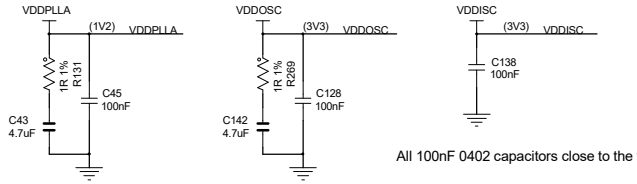




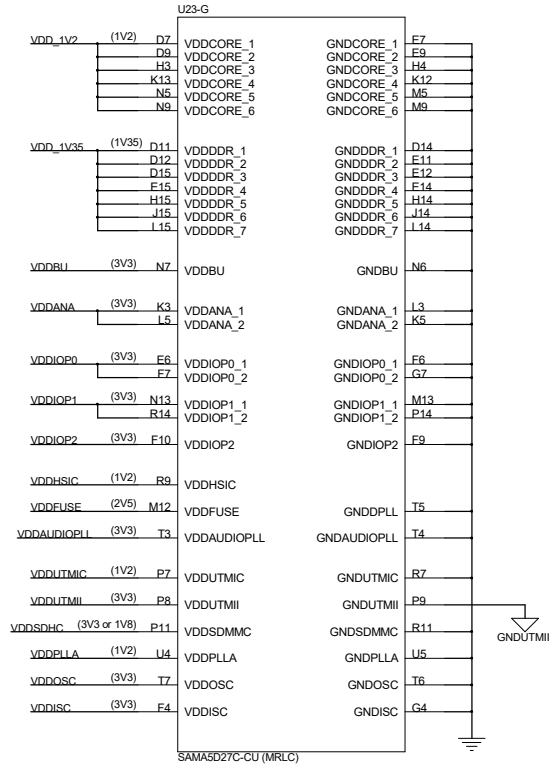


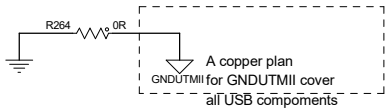






All 100nF 0402 capacitors close to the the Pin of VDD***.





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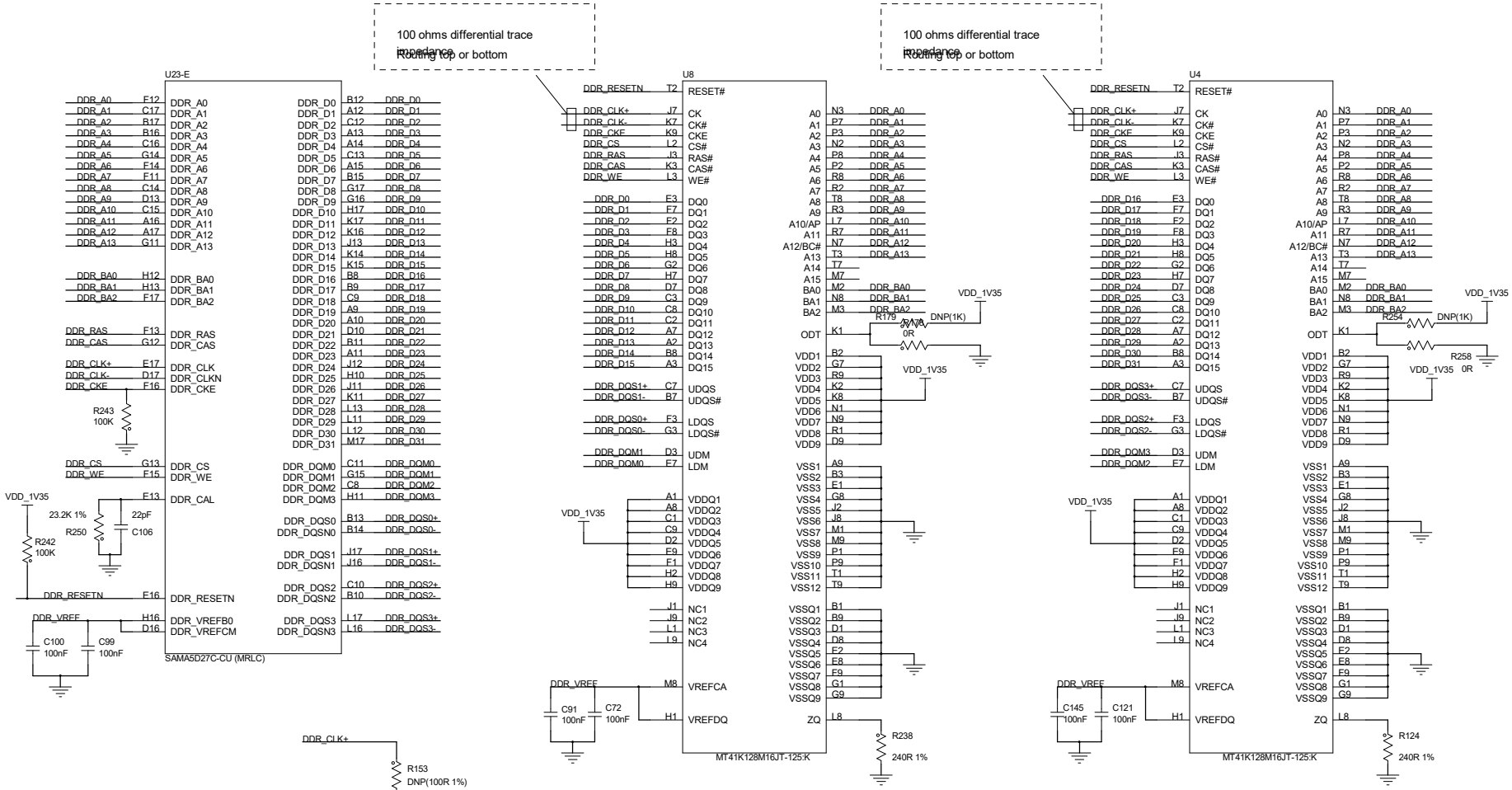
SAMA5D2C-XULT

SAMA5D27- Power

SCALE 1/1

REV. C

SHEET 5/12



Keep nets as short as possible, therefore, DDR devices have to be placed close as possible of SAMA5D27
The layout DDR should use controlled impedance traces of ZO= 50ohm characteristic impedance.

Address, control and data traces may not exceed 1.3 inches (33.0 mm).
Address, control and data traces must be length-matched to within 0.1 inch (2.54mm).
Address, control and data traces must match the data group trace lengths to within 0.25 inches (6.35mm).

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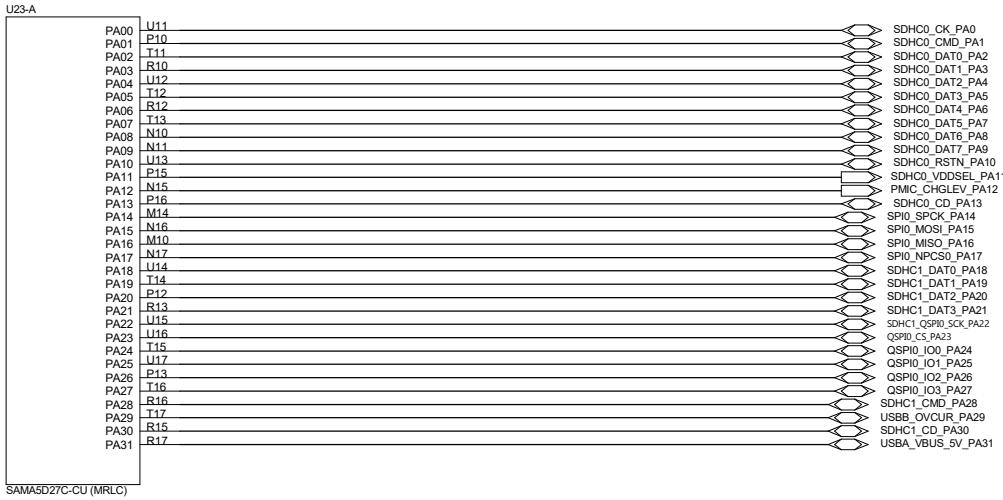
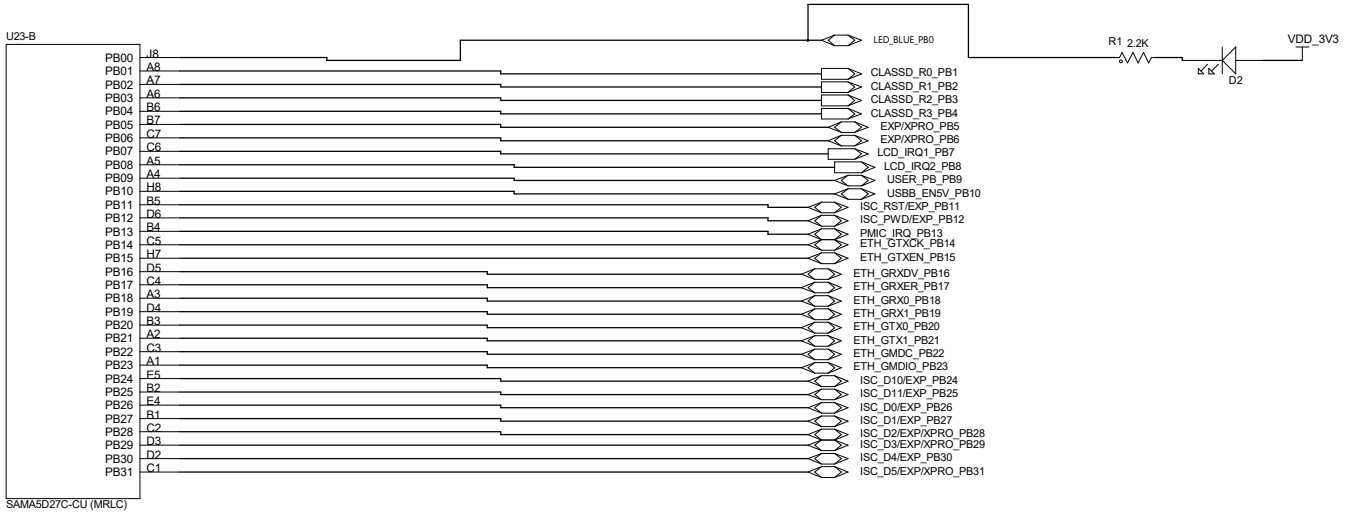
SAMA5D2C-XULT
SAMA5D27- DDR3
SCALE 1/1
REV. c
SHEET 6/12





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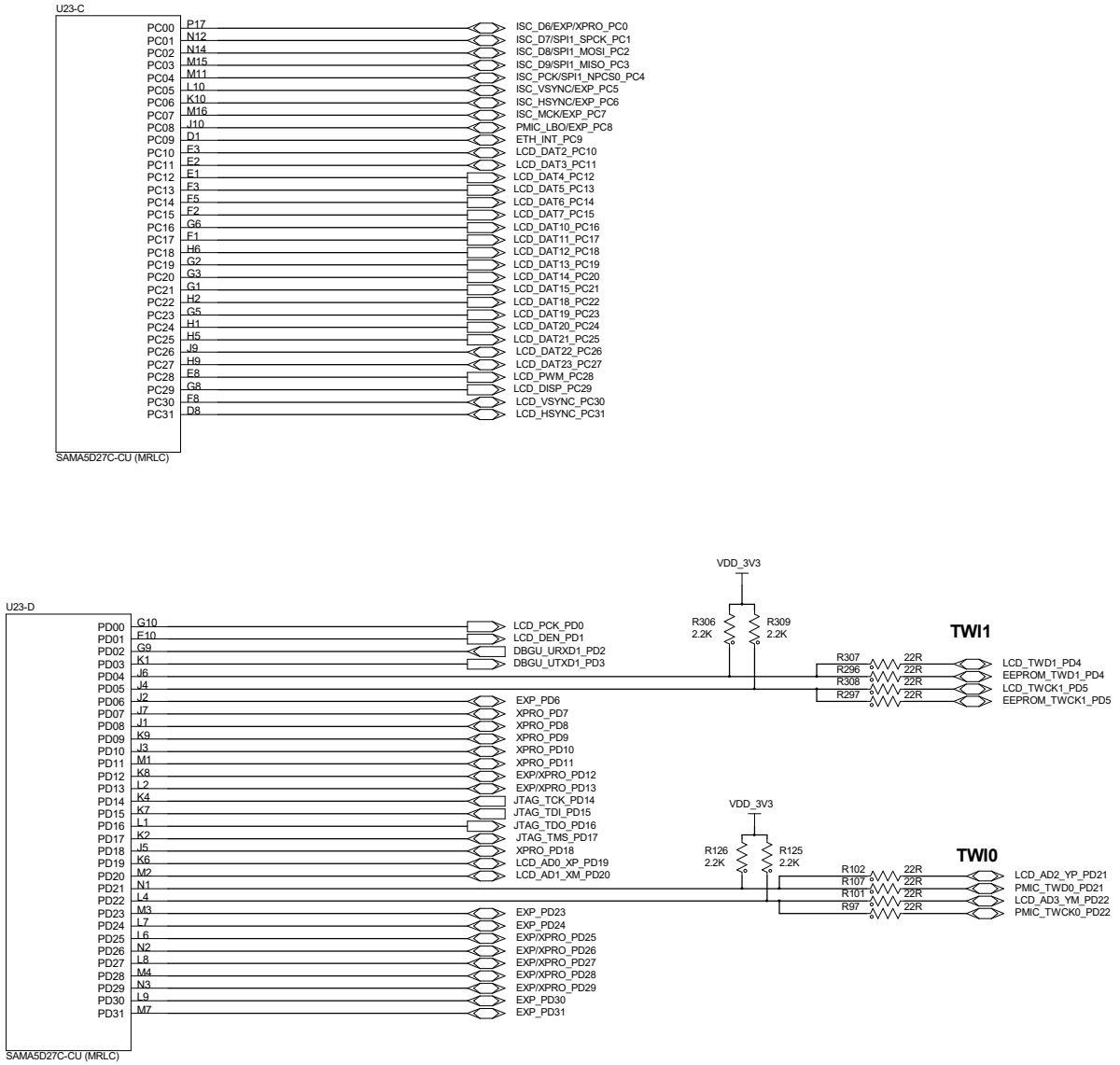
SAMA5D2C-XULT

SAMA5D27- PIOA & PIOB

SCALE 1/1

REV. C

SHEET 7/12



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SAMA5D2C-XULT

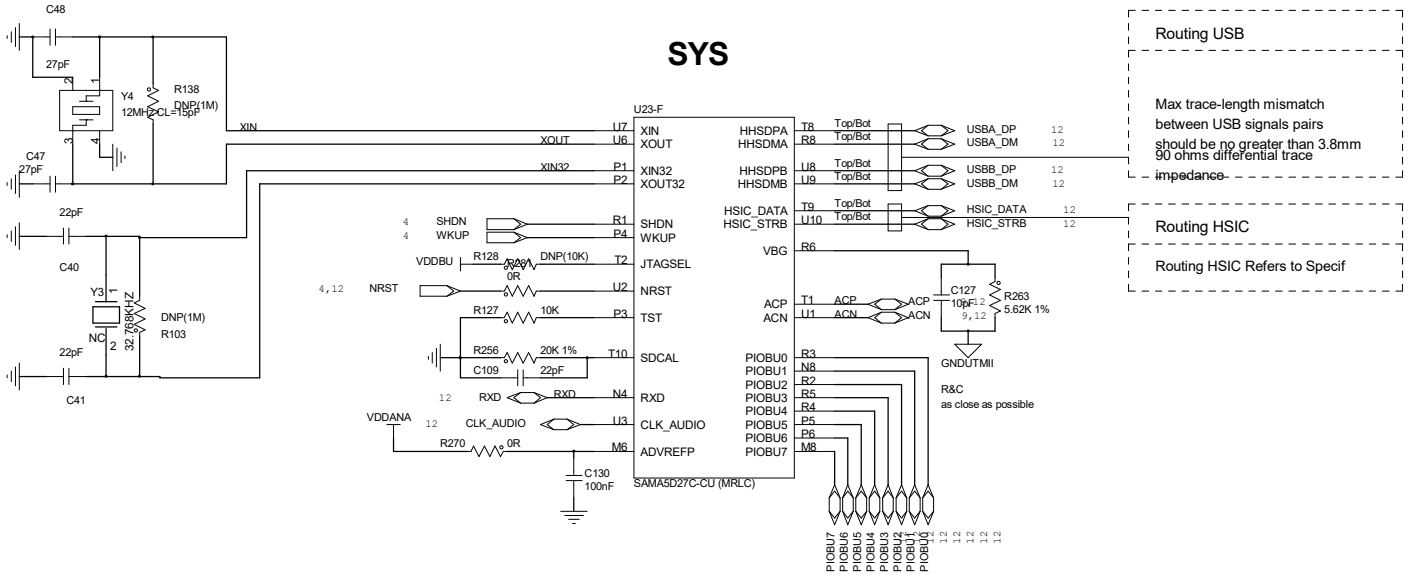
SAMA5D27- PIOC & PIOD

SCALE 1/1

REV. C

SHEET 8/12

SYS

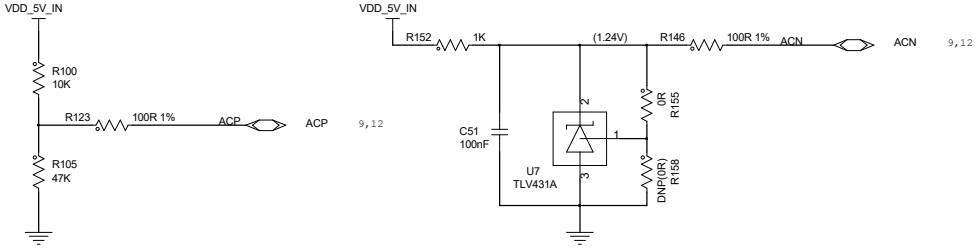


Routing USB

Max trace-length mismatch between USB signals pairs should be no greater than 3.8mm
90 ohms differential trace impedance

Routing HSIC

Routing HSIC Refers to Specif



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SAMA5D2C-XULT

SAMA5D27- SYS & JTAG & DBUG

SCALE 1/1

REV. C

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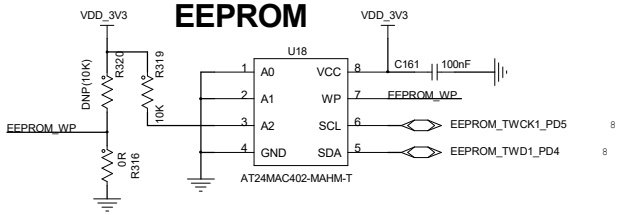
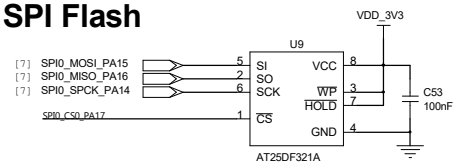
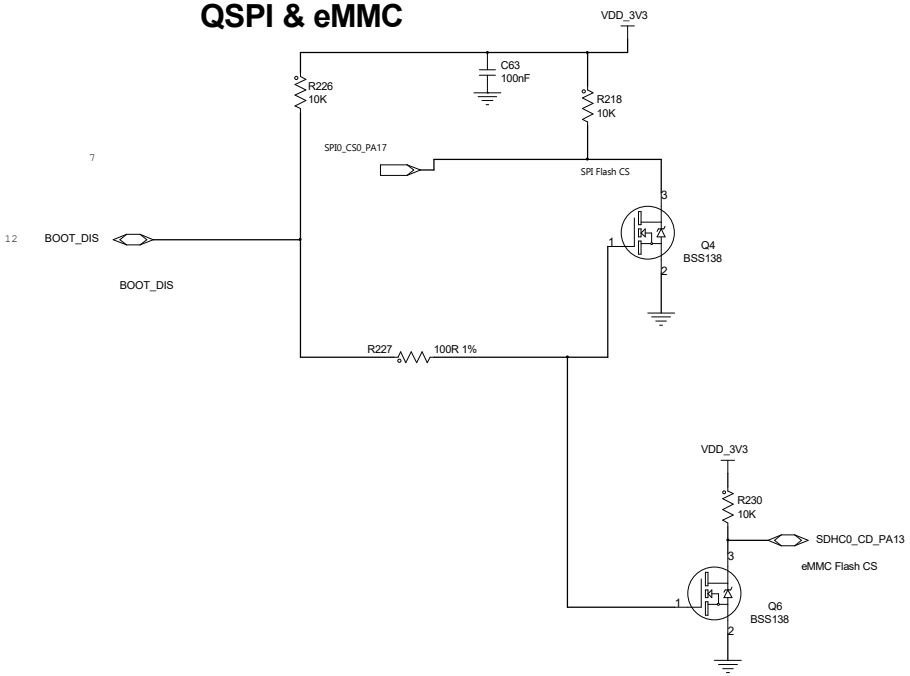
EEPROM



SPI Flash



QSPI & eMMC



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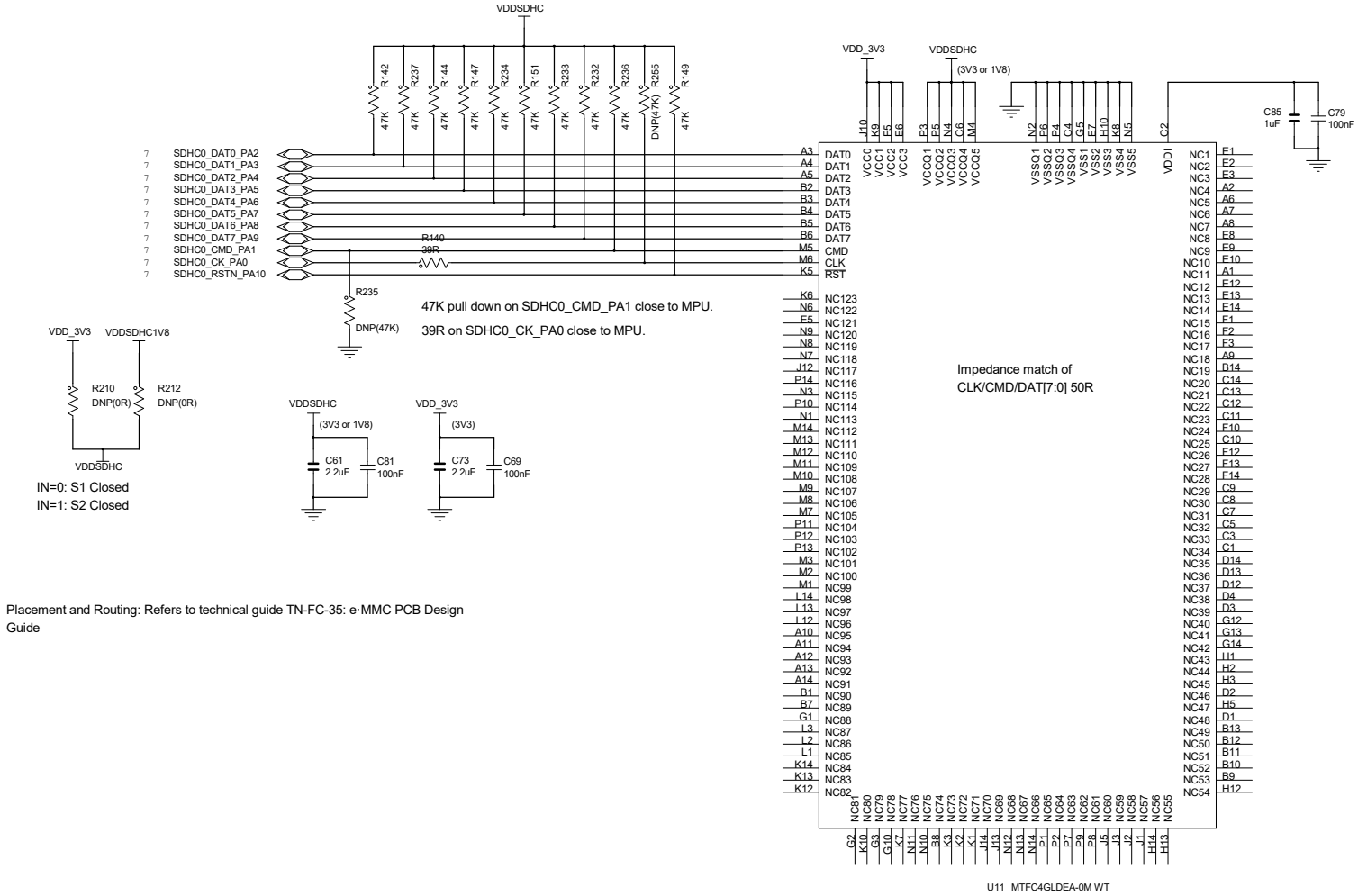
SAMA5D2C-XULT

Flash & Audio & LED

SCALE 1/1

REV. C

SHEET 10/12



Placement and Routing: Refers to technical guide TN-FC-35: e·MMC PCB Design Guide

eMMC - SDHC0

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SAMA5D2C-XULT

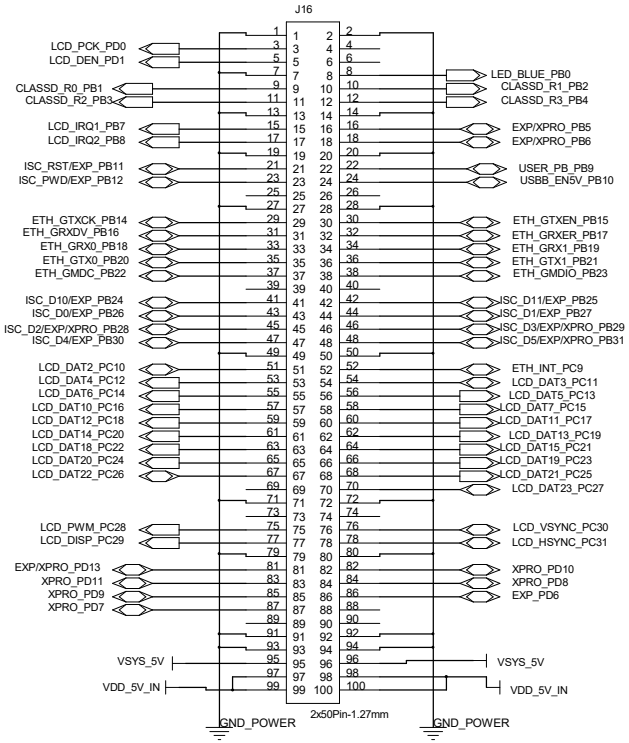
SD & eMMC

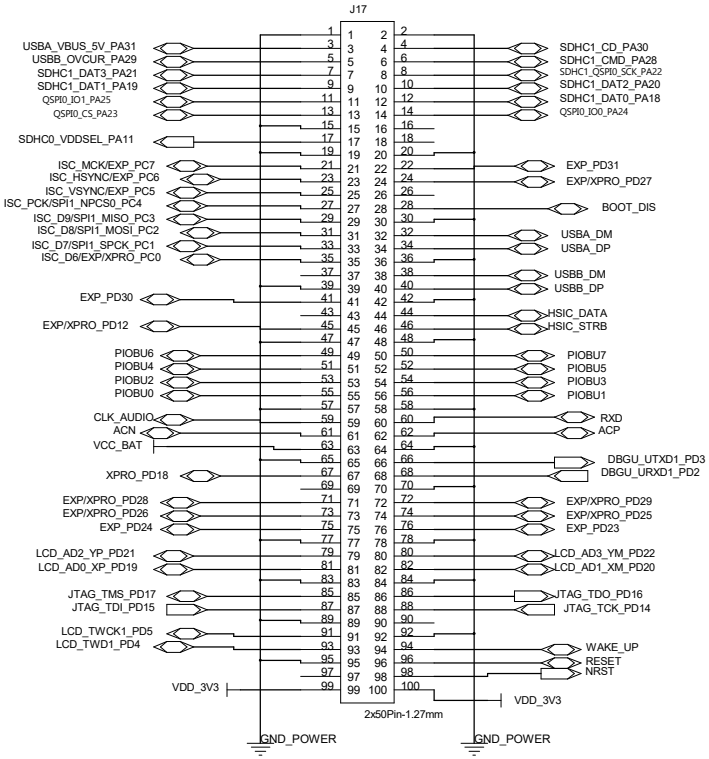
SCALE 1/1

REV. C

SHEET 11/12

Boards Connectors





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SAMA5D2C-XULT

Expansion & XPRO Connectors

SCALE 1/1

REV. C

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